MOTOROLA

HIGH SPEED CMOS INTEGRATED CIRCUITS

This book presents technical data for the broad line of High-Speed Logic integrated circuits. Complete specifications are provided in the form of data sheets. In addition, a comprehensive Function Selector Guide and a Design Considerations chapter have been included to familiarize the user with these new logic circuits.

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ALPHANUMERIC INDEX

Function Selector Guide

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BUFFERS/INVERTERS

1

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC04	Hex Inverter	LS04	*4069	LS/CMOS	14
HCT04	Hex Inverter with LSTTL-Compatible Inputs	LS04	*4069	LS/CMOS	14
HCU04	Hex Unbuffered Inverter	*LS04	4069	LS/CMOS	14
HC14	Hex Schmitt-Trigger Inverter	LS14	4584	LS/CMOS	14
HC125	Quad 3-State Noninverting Buffer	LS125		LS	14
HC126	Quad 3-State Noninverting Buffer	LS126		LS	14
HC240	Octal 3-State Inverting Buffer/Line Driver/Line Receiver	LS240		LS	20
HCT240	Octal 3-State Inverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	LS240		LS	20
HC241	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver	LS241		LS	20
HCT241	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	LS241		LS	20
HC242	Quad 3-State Inverting Bus Transceiver	LS242		LS	14
HC243	Quad 3-State Noninverting Bus Transceiver	LS243		LS	14
HC244	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver	LS244		LS	20
HCT244	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	LS244		LS	20
HC245	Octal 3-State Noninverting Bus Transceiver	LS245		LS	20
HCT245	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS245		LS	20
HC365	Hex 3-State Noninverting Buffer with Common Enables	LS365A		LS	16
HC366	Hex 3-State Inverting Buffer with Common Enables	LS366A		LS	16
HC367	Hex 3-State Noninverting Buffer with Separate 2-Bit and 4-Bit Sections	LS367A	*4503	LS/CMOS	16
HC368	Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections	LS368A		LS	16
HC540	Octal 3-State Inverting Buffer/Line Driver/Line Receiver	LS540		LS	20
HC541	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver	LS541		LS	20
HC640	Octal 3-State Inverting Bus Transceiver	LS640		LS	20
HCT640	Octal 3-State Inverting Bus Transceiver with LSTTL-Compatible Inputs	LS640		LS	20
HC643	Octal 3-State Inverting and Noninverting Bus Transceiver	LS643		LS	20
HCT643	Octal 3-State Inverting and Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS643		LS	20
HC4049	Hex Inverting Buffer/Logic-Level Down Converter		4049	CMOS	16
HC4050	Hex Noninverting Buffer/Logic-Level Down Converter		4050	CMOS	16

*Suggested alternative

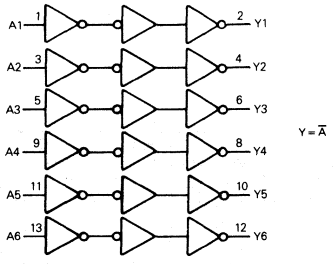
BUFFERS

Device	HC 04	HCT 04	HCU 04	HC 14	HC 125	HC 126	HC 240	HCT 240	HC 241	HCT 241	HC 242	HC 243	HC 244	HCT 244
# Pins	14	14	14	14	14	14	20	20	20	20	14	14	20	20
Quad Device					•	•					•	•		
Hex Device	•	•	•	•										
Octal Device							•	•	•	•			•	•
Noninverting Outputs					•	•			•	•		•	•	•
Inverting Outputs	•	•	•	•			•	•			•			
Single Stage (unbuffered)			•											
Schmitt Trigger				•										
3-State Outputs					•	•	•	•	•	•	•	•	•	•
Common Output Enables								•	•	•	•	•	•	•
Active-Low Output Enables					•		••	••	•	•	•	•	••	••
Active-High Output Enables						•			•	•	•	•		
Separate 4-Bit Sections							•	•	•	•			•	•
Separate 2-Bit and 4-Bit Sections														
Transceiver											•	•		
Direction Control														
Logic-Level Down Converter														
LSTTL-Compatible Inputs		•						•		•				•

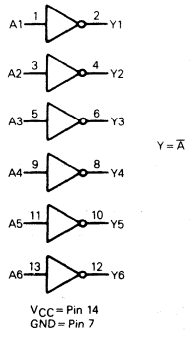
Device	HC 245	HCT 245	HC 365	HC 366	HC 367	HC 368	HC 540	HC 541	HC 640	HCT 640	HC 643	HCT 643	HC 4049	HC 4050
# Pins	20	20	16	16	16	16	20	20	20	20	20	20	16	16
Quad Device														
Hex Device			•	•	•	•							•	•
Octal Device	•	•					•	•	•	•	•	•		
Noninverting Outputs	•	•	•		•			•			•	•		•
Inverting Outputs				•		•	•		•	•	•	•	•	
Single Stage (unbuffered)														
Schmitt Trigger														
3-State Outputs	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Common Output Enables	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Active-Low Output Enables	•	•	••	••	••	••	••	••	•	•	•	•		
Active-High Output Enables														
Separate 4-Bit Sections														
Separate 2-Bit and 4-Bit Sections					•	•								
Transceiver	•	•							•	•	•	•		
Direction Control	•	•							•	•	•	•		
Logic-Level Down Converter													•	•
LSTTL-Compatible Inputs		•								•		•		

BUFFERS/INVERTERS (Continued)

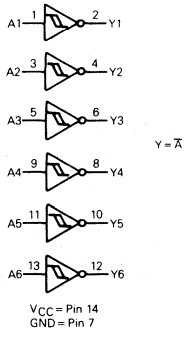
HC04
HCT04



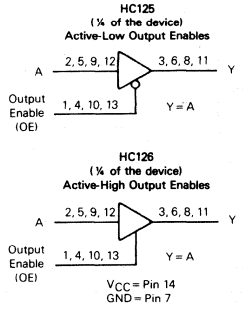
HCU04



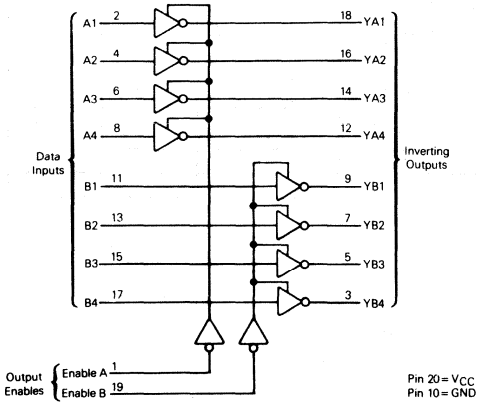
HC14



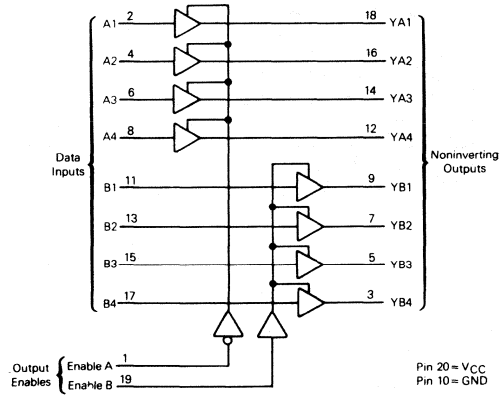
HC125
HC126



HC240
HCT240

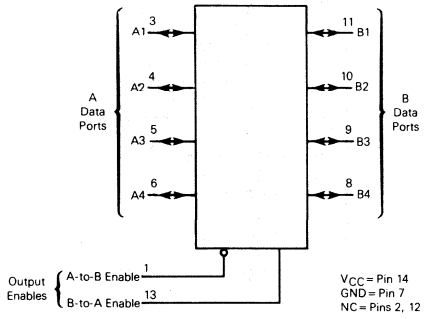


HC241
HCT241

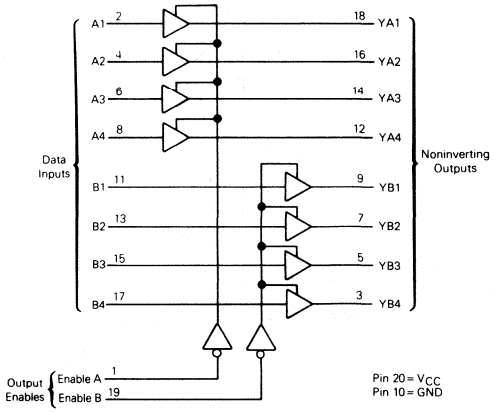


BUFFERS/INVERTERS (Continued)

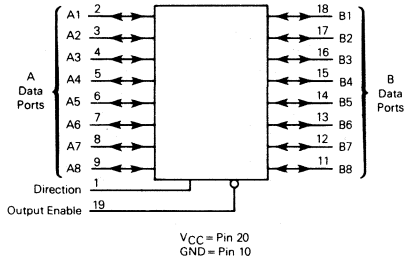
HC242
HC243



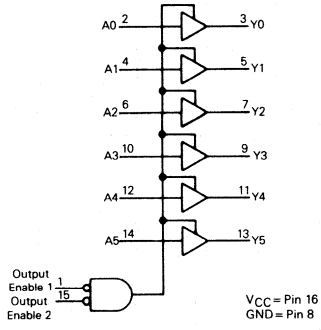
HC244
HCT244



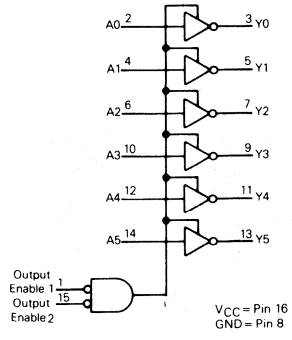
HC245
HCT245



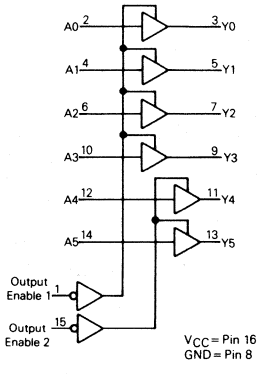
HC365



HC366



HC367



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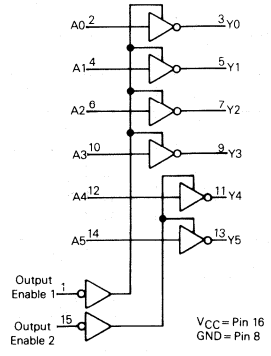
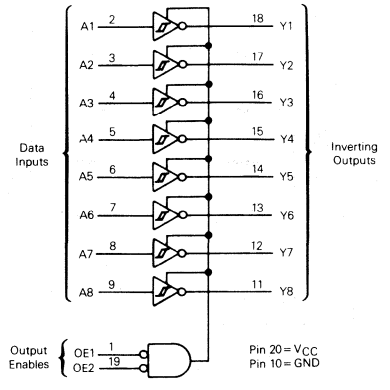
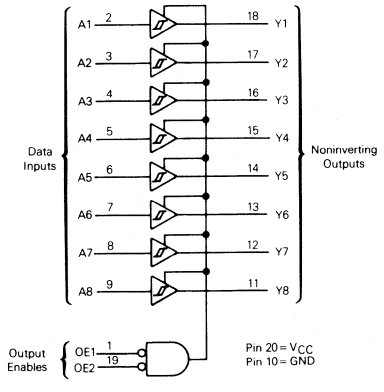
HC368



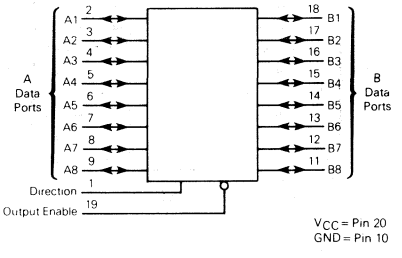
HC540



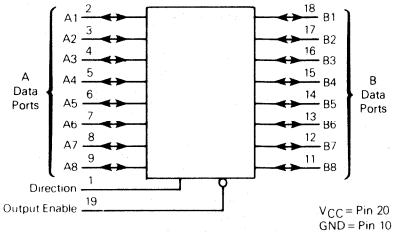
HC541



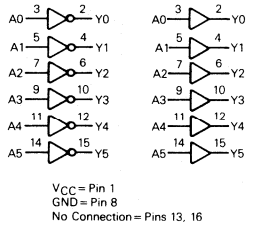
HC640
HCT640



HC643
HCT643



HC4049
HC4050



GATES

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC00	Quad 2-Input NAND Gate	LS00	4011	LS	14
HCT00	Quad-2 Input NAND Gate with LSTTL-Compatible Inputs	LS00	4011	LS	14
HC02	Quad 2-Input NOR Gate	LS02	4001	LS	14
HC03	Quad 2-Input NAND Gate with Open-Drain Outputs	LS03	*4011	LS	14
HC08	Quad 2-Input AND Gate	LS08	4081	LS	14
HC10	Triple 3-Input NAND Gate	LS10	4023	LS	14
HC11	Triple 3-Input AND Gate	LS11	4073	LS	14
HC20	Dual 4-Input NAND Gate	LS20	4012	LS	14
HC27	Triple 3-Input NOR Gate	LS27	4025	LS	14
HC30	8-Input NAND Gate	LS30	4068	LS	14
HC32	Quad 2-Input OR Gate	LS32	4071	LS	14
HC51	2-Wide, 2-Input/2-Wide, 3-Input AND-OR-INVERT Gates	LS51	*4506	LS	14
☆HC58	2-Wide, 2-Input/2-Wide, 3-Input AND-OR Gates	*LS51	*4506		14
HC86	Quad 2-Input Exclusive OR Gate	LS86	4070	LS	14
HC132	Quad 2-Input Schmitt-Trigger NAND Gate	LS132	4093	LS	14
HC133	13-Input NAND Gate	LS133		LS	16
HC266	Quad 2-Input Exclusive NOR Gate	*LS266	4077	LS/CMOS	14
HC4002	Dual 4-Input NOR Gate	*LS25	4002	CMOS	14
HC4075	Triple 3-Input OR Gate		4075	CMOS	14
HC4078	8-Input NOR/OR Gate		4078	CMOS	14

*Suggested alternative

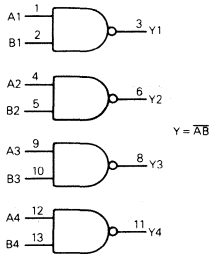
☆High-Speed CMOS design only

Device	HC 00	HCT 00	HC 02	HC 03	HC 08	HC 10	HC 11	HC 20	HC 27	HC 30
#Pins	14	14	14	14	14	14	14	14	14	14
Single Device										•
Dual Device								•		
Triple Device						•	•		•	
Quad Device	•	•	•	•	•					
NAND	•	•		•		•		•		•
NOR			•						•	
AND					•		•			
OR										
Exclusive OR										
Exclusive NOR										
AND-OR-INVERT										
AND-OR										
2-Input	•	•	•	•	•					
3-Input						•	•		•	
4-Input								•		
8-Input										•
13-Input										
Schmitt Trigger Inputs										
LSTTL-Compatible Inputs		•								
Open-Drain Outputs				•						

Device	HC 32	HC 51	HC 58	HC 86	HC 132	HC 133	HC 266	HC 4002	HC 4075	HC 4078
#Pins	14	14	14	14	14	16	14	14	14	14
Single Device		•	•			•				•
Dual Device								•		
Triple Device									•	
Quad Device	•			•	•		•			
NAND					•	•				
NOR								•		•
AND										
OR	•								•	
Exclusive OR				•						
Exclusive NOR							•			
AND-OR-INVERT		•								
AND-OR			•							
2-Input	•	•	•	•	•		•			
3-Input		•	•						•	
4-Input								•		
8-Input										•
13-Input						•				
Schmitt Trigger Inputs					•					
LSTTL-Compatible Inputs										
Open-Drain Outputs										

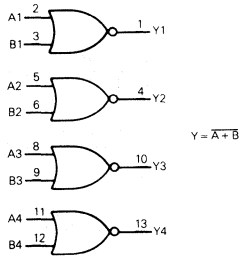
GATES (Continued)

HC00
HCT00



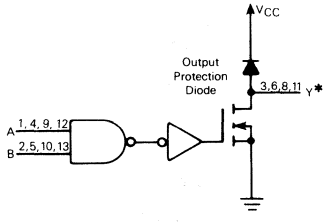
V_{CC} = Pin 14
GND = Pin 7

HC02



V_{CC} = Pin 14
GND = Pin 7

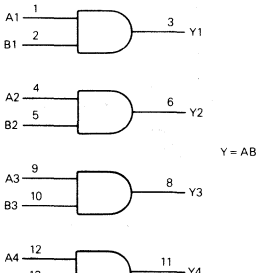
HC03



V_{CC} = Pin 14
GND = Pin 7

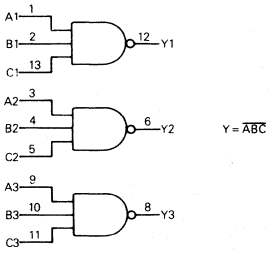
*Denotes open-drain outputs.

HC08

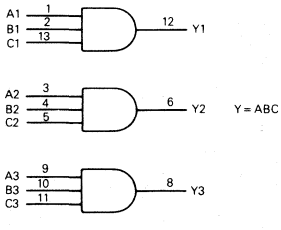


V_{CC} = Pin 14
GND = Pin 7

HC10



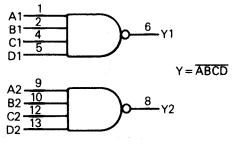
HC11



V_{CC} = Pin 14
GND = Pin 7

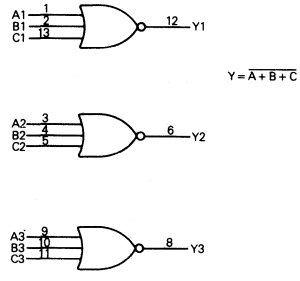
GATES (Continued)

HC20



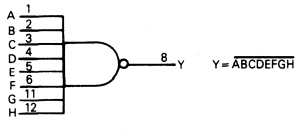
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 3, 11

HC27



V_{CC} = Pin 14
GND = Pin 7

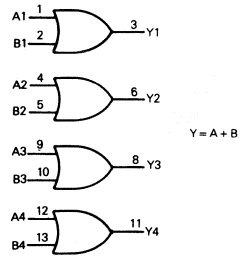
HC30



Pins 9, 10, 13 = no connection

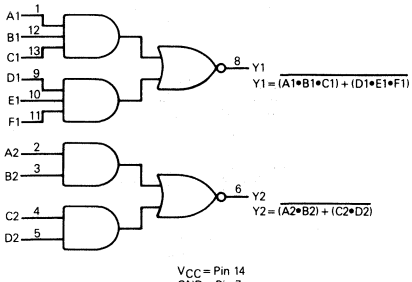
V_{CC} = Pin 14
GND = Pin 7

HC32



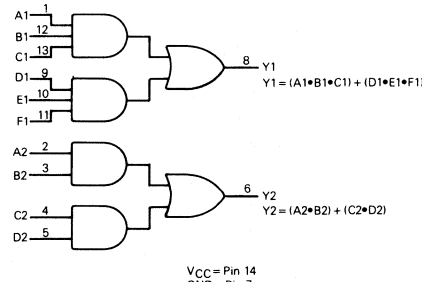
V_{CC} = Pin 14
GND = Pin 7

HC51



V_{CC} = Pin 14
GND = Pin 7

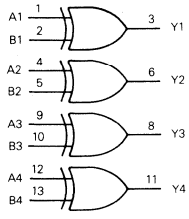
HC58



V_{CC} = Pin 14
GND = Pin 7

GATES (Continued)

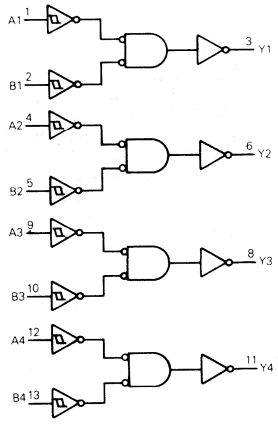
HC86



$Y = A \oplus B = \overline{A}B + A\overline{B}$

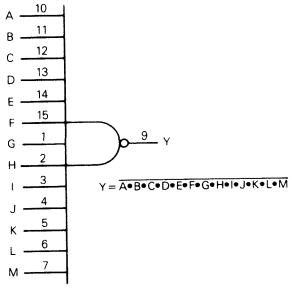
V_{CC} = Pin 14
GND = Pin 7

HC132



$Y = \overline{AB}$

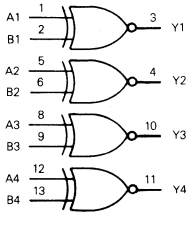
HC133



$Y = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H \bullet I \bullet J \bullet K \bullet L \bullet M}$

V_{CC} = Pin 16
GND = Pin 8

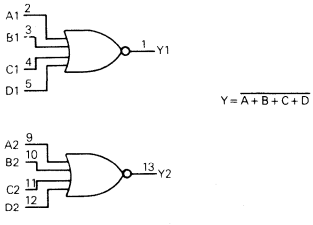
HC266



$Y = \overline{A \oplus B} = AB + \overline{A}\overline{B}$

V_{CC} = Pin 14
GND = Pin 7

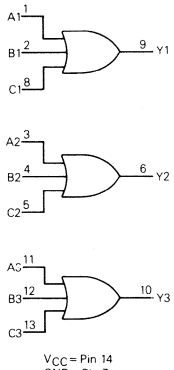
HC4002



$Y = \overline{A + B + C + D}$

V_{CC} = Pin 14
GND = Pin 7
No Connection = Pins 6, 8

HC4075

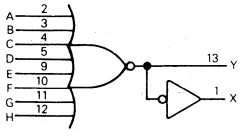


$Y = A + B + C$

V_{CC} = Pin 14
GND = Pin 7

GATES (Continued)

HC4078



$Y = \overline{A + B + C + D + E + F + G + H}$

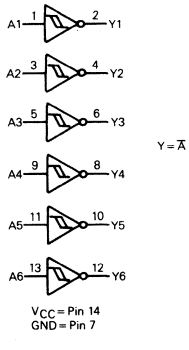
$X = A + B + C + D + E + F + G + H$

V_{CC} = Pin 14
GND = Pin 7
No Connection = Pins 6, 8

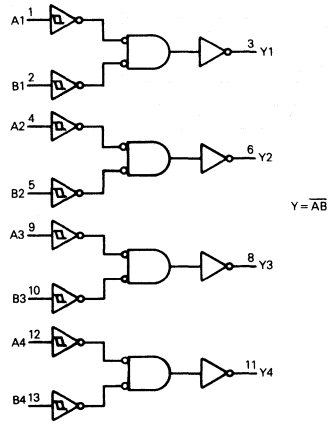
SCHMITT TRIGGERS

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC14	Hex Schmitt-Trigger Inverter	LS14	4584	LS/CMOS	14
HC132	Quad 2-Input Schmitt-Trigger NAND Gate	LS132	4093	LS	14

HC14



HC132



BUS TRANSCEIVERS

1

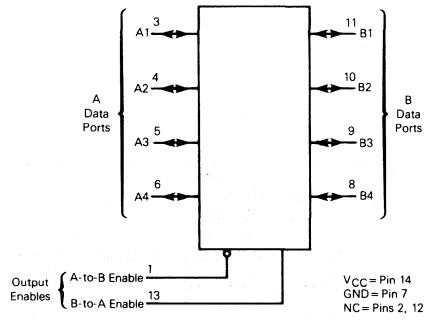
Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC242	Quad 3-State Inverting Bus Transceiver	LS242		LS	14
HC243	Quad 3-State Noninverting Bus Transceiver	LS243		LS	14
HC245	Octal 3-State Noninverting Bus Transceiver	LS245		LS	20
HCT245	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS245		LS	20
HC640	Octal 3-State Inverting Bus Transceiver	LS640		LS	20
HCT640	Octal 3-State Inverting Bus Transceiver with LSTTL-Compatible Inputs	LS640		LS	20
HC643	Octal 3-State Inverting and Noninverting Bus Transceiver	LS643		LS	20
HCT643	Octal 3-State Inverting and Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS643		LS	20
HC646	Octal 3-State Noninverting Bus Transceiver and D-Type Flip-Flop	LS646		LS	24
HC648	Octal 3-State Inverting Bus Transceiver and D-Type Flip-Flop	LS648		LS	24

Device	HC 242	HC 243	HC 245	HCT 245	HC 640	HCT 640	HC 643	HCT 643	HC 646	HC 648
#Pins	14	14	20	20	20	20	20	20	24	24
Quad Device	•	•								
Octal Device			•	•	•	•	•	•	•	•
Buffer	•	•	•	•	•	•	•	•		
Storage Capability									•	•
Inverting Output	•				•	•	•	•	•	
Noninverting Output		•	•	•			•	•		•
Common Output Enables	•	•	•	•	•	•	•	•	•	•
Active-Low Output Enable	•	•	•	•	•	•	•	•	•	•
Active-High Output Enable	•	•								
Direction Control			•	•	•	•	•	•	•	•
LSTTL-Compatible Inputs				•		•		•		

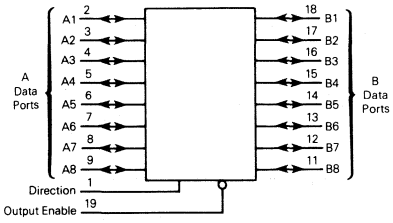
BUS TRANSCEIVERS (Continued)

HC242
HC243

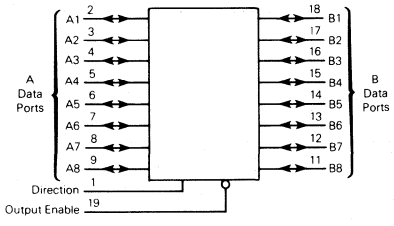
HC242 — Inverting Outputs
HC243 — Noninverting Outputs



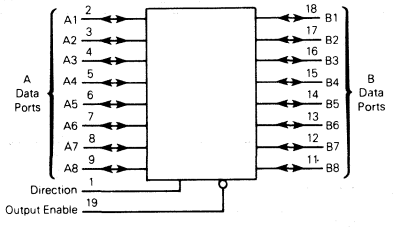
HC245
HCT245



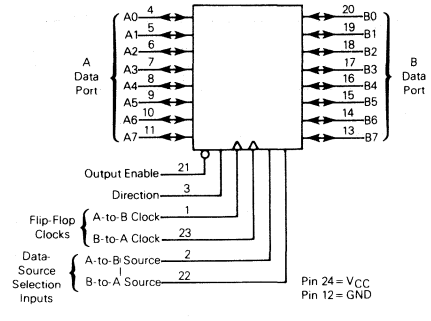
HC640
HCT640



HC643
HCT643



HC646
HC648



LATCHES

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC75	Dual 2-Bit Transparent Latch	LS75	*4042	LS	16
HC259	8-Bit Addressable Latch/1-of-8 Decoder	LS259	*4099	LS	16
HC373	Octal 3-State Noninverting D-Type Transparent Latch	LS373, LS573		LS373	20
HCT373	Octal 3-State Noninverting D-Type Transparent Latch with LSTTL-Compatible Inputs	LS373, LS573		LS373	20
HC533	Octal 3-State Inverting D-Type Transparent Latch	LS533		LS	20
HC563	Octal 3-State Inverting D-Type Transparent Latch	LS533			20
HC573	Octal 3-State Noninverting D-Type Transparent Latch	LS373, LS573		LS573	20

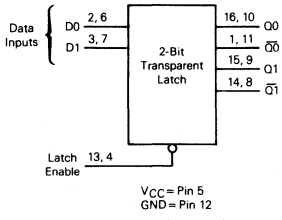
* Suggested alternative

Device	HC 75	HC 259	HC 373	HCT 373	HC 533	HC 563	HC 573
#Pins	16	16	20	20	20	20	20
Single Device		•					
Dual Device	•						
Octal Device			•	•	•	•	•
1-Bit			•	•	•	•	•
2-Bit	•						
8-Bit		•					
Transparent	•	•	•	•	•	•	•
Addressable		•					
Noninverting Outputs	•	•	•	•			•
Inverting Outputs	•				•	•	
Common Latch Enable			•	•	•	•	•
Active-Low Latch Enable	•	•	•	•	•	•	•
Active-Low Reset		•					
3-State Outputs			•	•	•	•	•
Common Output Enable; Active-Low			•	•	•	•	•
LSTTL-Compatible Inputs				•			

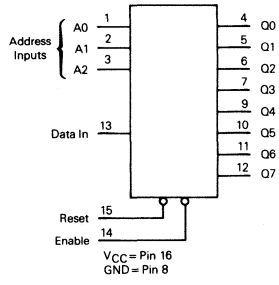
These devices are identical in function and are different in pinout only: HC373 and HC573
HC533 and HC563

LATCHES (Continued)

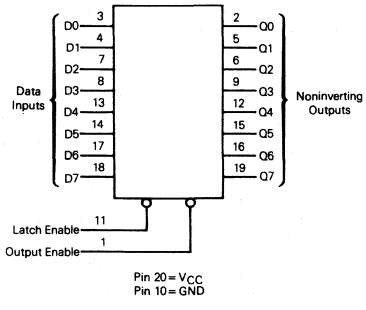
HC75



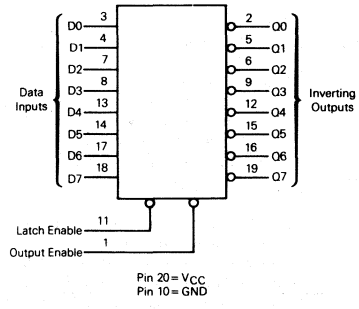
HC259



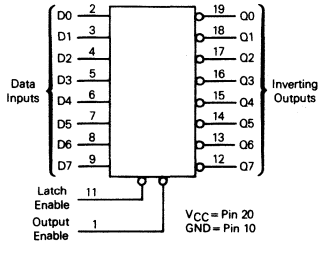
HC373
HCT373



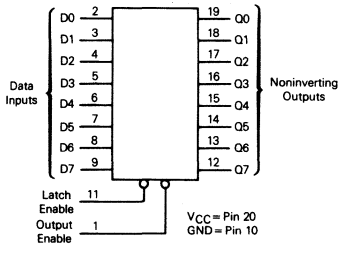
HC533



HC563



HC573



FLIP-FLOPS

1

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC73	Dual J-K Flip-Flop with Reset	LS73A, LS107A	*4027	LS73A	14
HC74	Dual D-Type Flip-Flop with Set and Reset	LS74A	4013	LS	14
HC76	Dual J-K Flip-Flop with Set and Reset	LS76A, LS112A	*4027	LS76A	16
HC107	Dual J-K Flip-Flop with Reset	LS73A, LS107A	*4027	LS107A	14
HC109	Dual J-$\overline{K}$ Flip-Flop with Set and Reset	LS109A	*4027	LS	16
HC112	Dual J-K Flip-Flop with Set and Reset	LS76A, LS112A	*4027	LS112A	16
HC113	Dual J-K Flip-Flop with Set	LS113A	*4027	LS	14
HC173	Quad 3-State D-Type Flip-Flop with Common Clock and Reset	LS173A	4076	LS/CMOS	16
HC174	Hex D-Type Flip-Flop with Common Clock and Reset	LS174	4174	LS/CMOS	16
HC175	Quad D-Type Flip-Flop with Common Clock and Reset	LS175	4175	LS/CMOS	16
HC273	Octal D-Type Flip-Flop with Common Clock and Reset	LS273		LS	20
HC374	Octal 3-State Noninverting D-Type Flip-Flop	LS374, LS574		LS374	20
HCT374	Octal 3-State Noninverting D-Type Flip-Flop with LSTTL-Compatible Inputs	LS374, LS574		LS374	20
HC534	Octal 3-State Inverting D-Type Flip-Flop	LS534		LS	20
HC564	Octal 3-State Inverting D-Type Flip-Flop	LS534			20
HC574	Octal 3-State Noninverting D-Type Flip-Flop	LS374, LS574		LS574	20
HC646	Octal 3-State Noninverting Bus Transceiver and D-Type Flip-Flop	LS646		LS	24
HC648	Octal 3-State Inverting Bus Transceiver and D-Type Flip-Flop	LS648		LS	24

* Suggested alternative

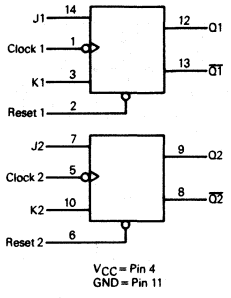
Device	HC 73	HC 74	HC 76	HC 107	HC 109	HC 112	HC 113	HC 173	HC 174
#Pins	14	14	16	14	16	16	14	16	16
Type	J-K	D	J-K	J-K	J-$\overline{K}$	J-K	J-K	D	D
Dual Device	•	•	•	•	•	•	•		
Quad Device								•	
Hex Device									•
Octal Device									
Common Clock								•	•
Negative-Transition Clocking	•		•	•		•	•		
Postive-Transition Clocking		•			•			•	•
Common, Active-Low Data Enables								••	
Noninverting Outputs	•	•	•	•	•	•	•	•	•
Inverting Outputs	•	•	•	•	•	•	•		
3-State Outputs								•	
Common, Active-Low Output Enables								••	
Common Reset								•	•
Active-Low Reset	•	•	•	•	•	•			•
Active-High Reset								•	
Active-Low Set		•	•		•	•	•		
Transceiver									
Direction Control									
LSTTL-Compatible Inputs									

Device	HC 175	HC 273	HC 374	HCT 374	HC 534	HC 564	HC 574	HC 646	HC 648
#Pins	16	20	20	20	20	20	20	24	24
Type	D	D	D	D	D	D	D	D	D
Dual Device									
Quad Device	•								
Hex Device									
Octal Device		•	•	•	•	•	•	•	•
Common Clock	•	•	•	•	•	•	•	•	•
Negative-Transition Clocking									
Positive-Transition Clocking	•	•	•	•	•	•	•	•	•
Common, Active-Low Data Enables									
Noninverting Outputs	•	•	•	•			•	•	
Inverting Outputs	•				•	•			•
3-State Outputs			•	•	•	•	•	•	•
Common, Active-Low Output Enables			•	•	•	•	•	•	•
Common Reset	•	•							
Active-Low Reset	•	•							
Active-High Reset									
Active-Low Set									
Transceiver								•	•
Direction Control								•	•
LSTTL-Compatible Inputs				•					

These devices are identical in function and are different in pinout only: HC73 and HC107
HC76 and HC112
HC374 and HC574
HC534 and HC564

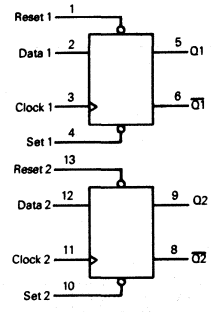
FLIP-FLOPS (Continued)

HC73



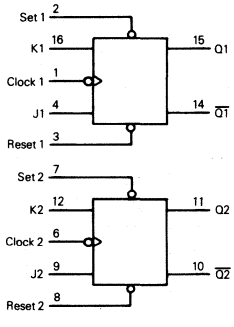
V_{CC} = Pin 4
GND = Pin 11

HC74



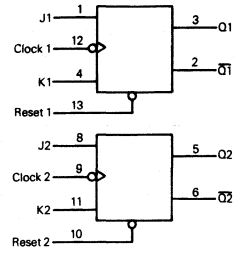
V_{CC} = Pin 14
GND = Pin 7

HC76



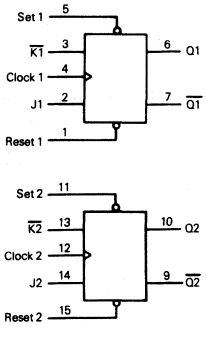
V_{CC} = Pin 5
GND = Pin 13

HC107



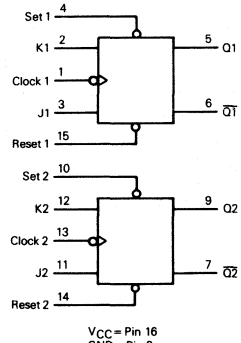
V_{CC} = Pin 14
GND = Pin 7

HC109



V_{CC} = Pin 16
GND = Pin 8

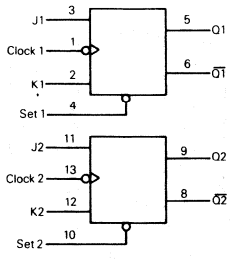
HC112



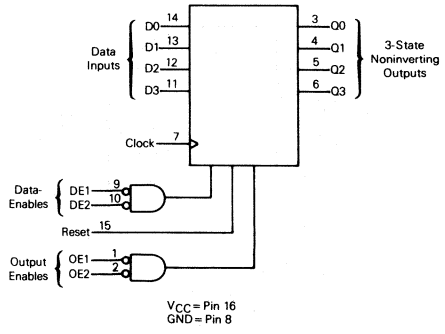
V_{CC} = Pin 16
GND = Pin 8

FLIP-FLOPS (Continued)

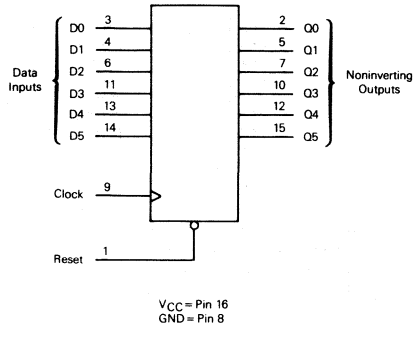
HC113



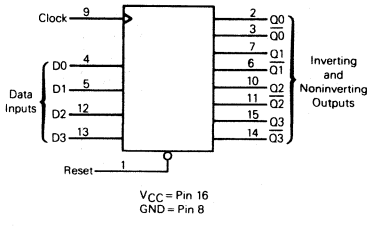
HC173



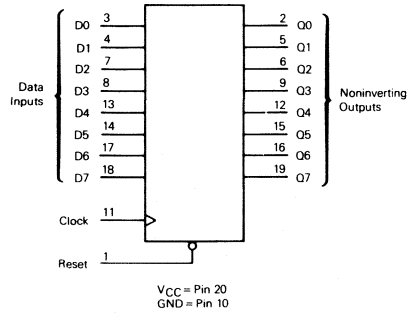
HC174



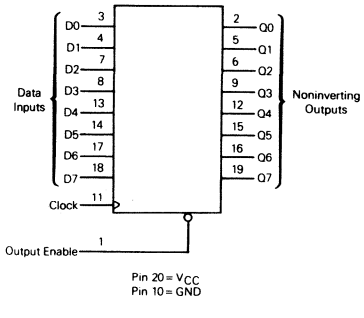
HC175



HC273

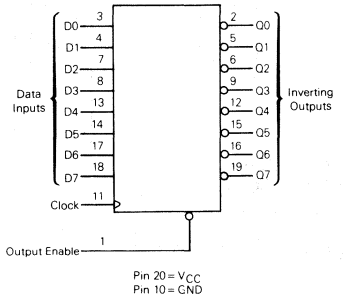


HC374
HCT374

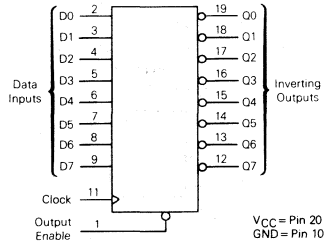


FLIP-FLOPS (Continued)

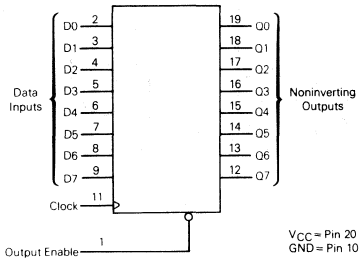
HC534



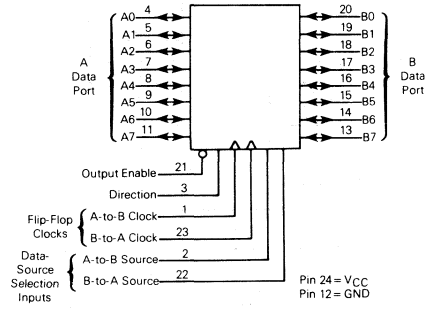
HC564



HC574



HC646
HC648



DIGITAL DATA SELECTORS/MULTIPLEXERS

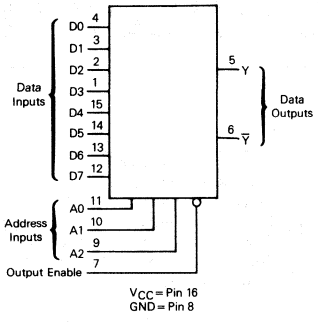
Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC151	8-Input Data Selector/Multiplexer	LS151	*4512	LS	16
HC153	Dual 4-Input Data Selector/Multiplexer	LS153	4539	LS/CMOS	16
HC157	Quad 2-Input Noninverting Data Selector/Multiplexer	LS157	*4519	LS	16
HC158	Quad 2-Input Inverting Data Selector/Multiplexer	LS158	*4519	LS	16
HC251	8-Input Data Selector/Multiplexer with 3-State Outputs	LS251	*4512	LS	16
HC253	Dual 4-Input Data Selector/Multiplexer with 3-State Outputs	LS253	*4539	LS/CMOS	16
HC257	Quad 2-Input Data Selector/Multiplexer with 3-State Outputs	LS257	*4519	LS	16
HC298	Quad 2-Input Data Selector/Multiplexer with Output Latch	LS298		LS	16
HC354	8-Input Data Selector/Multiplexer with Data and Address Latches and with 3-State Outputs	LS354, *LS356	*4512	LS354	20
HC356	8-Input Data Selector/Multiplexer with Data and Address Latches and with 3-State Outputs	*LS354, LS356	*4512	LS356	20

*Suggested alternative

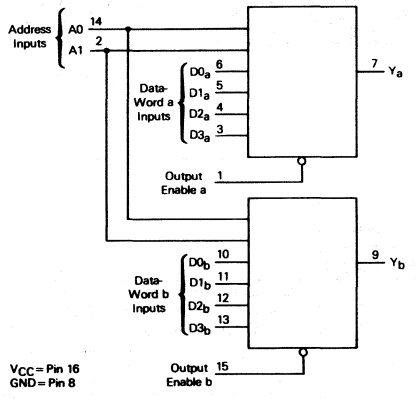
Device	HC 151	HC 153	HC 157	HC 158	HC 251	HC 253	HC 257	HC 298	HC 354	HC 356
#Pins	16	16	16	16	16	16	16	16	20	20
Description	One of 8 inputs is selected	One of 4 inputs is selected	One of two 4-bit words is selected	One of two 4-bit words is selected	One of 8 inputs is selected	One of 4 inputs is selected	One of two 4-bit words is selected	One of two 4-bit words is selected	One of 8 inputs is selected	One of 8 inputs is selected
Single Device	•				•				•	•
Dual Device		•				•				
Quad Device			•	•			•	•		
Data Latch with Active-Low Latch Enable									•	•
Common Address		•	•	•		•	•	•		
1-Bit Binary Address			•	•			•	•		
2-Bit Binary Address		•				•				
3-Bit Binary Address	•				•				•	•
Address Latch (Transparent)									•	
Address Latch (Non-transparent)										•
Active-Low Address Latch Enable									•	•
Output Latch with Active-Low Latch Clock								•		
Noninverting Output	•	•	•		•	•	•	•	•	•
Inverting Output	•			•	•				•	•
3-State Outputs					•	•	•		•	•
Common Output Enable			•	•			•			
Active-High Output Enable									•	•
Active-Low Output Enable	•	•	•	•	•	•	•		••	••

DIGITAL DATA SELECTORS/MULTIPLEXERS (Continued)

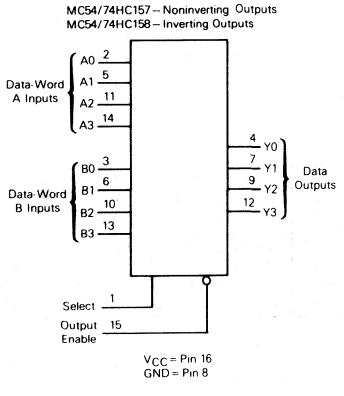
HC151



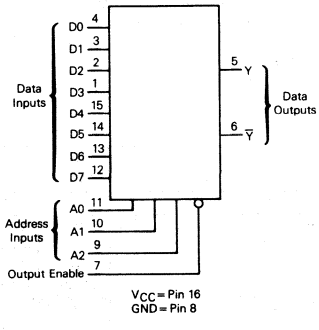
HC153



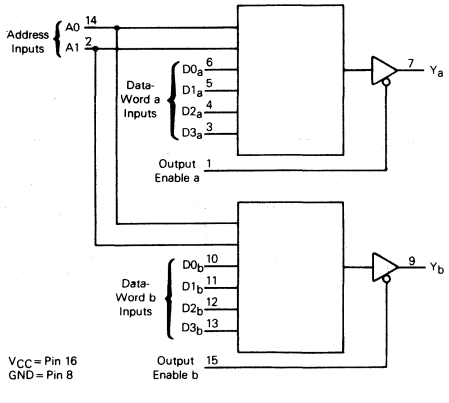
HC157
HC158



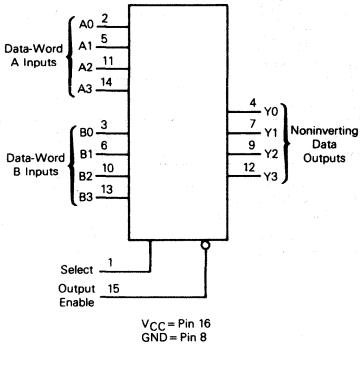
HC251



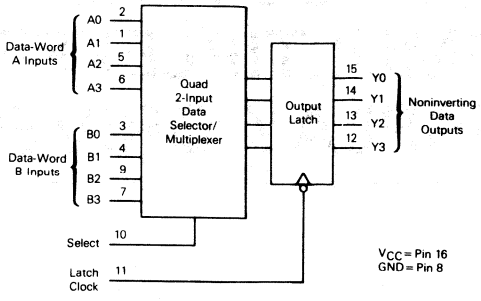
HC253



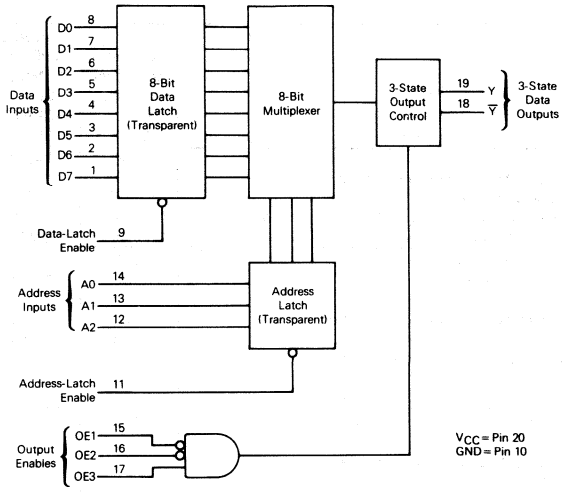
HC257



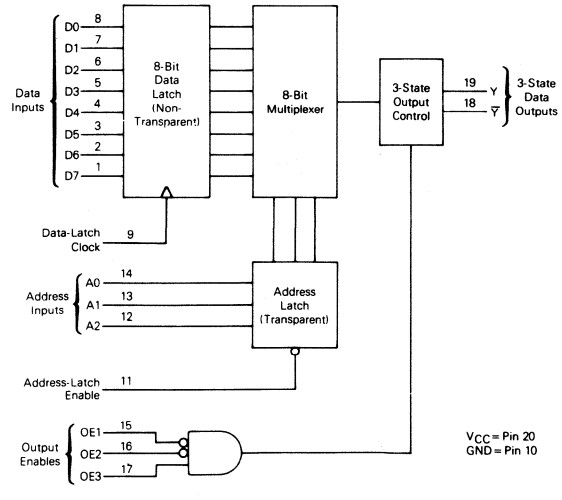
HC298



HC354



HC356



DECODERS/ DEMULTIPLEXERS/ DISPLAY DRIVERS

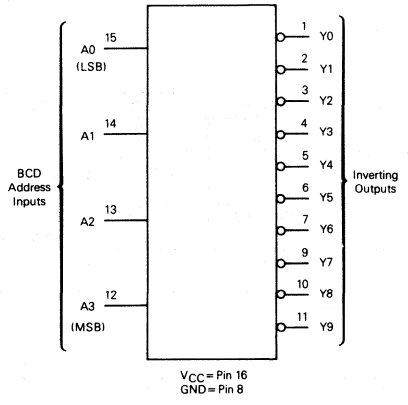
Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC42	1-of-10 Decoder	LS42	*4028	LS	16
HC137	1-of-8 Decoder/Demultiplexer with Address Latch	LS137	*4028	LS	16
HC138	1-of-8 Decoder/Demultiplexer	LS138	*4028	LS	16
HCT138	1-of-8 Decoder/Demultiplexer with LSTTL-Compatible Inputs	LS138	*4028	LS	16
HC139	Dual 1-of-4 Decoder/Demultiplexer	LS139	4556	LS/CMOS	16
HC147	Decimal-to-BCD Priority Encoder	LS147		LS	16
HC154	1-of-16 Decoder/Demultiplexer	LS154, *LS159	*4515	LS154	24
HC237	1-of-8 Decoder/Demultiplexer with Address Latch	*LS137	*4028	LS	16
HC259	8-Bit Addressable Latch/1-of-8 Decoder	LS259	*4099	LS	16
HC4511	BCD-to-Seven-Segment Latch/Decoder/Display Driver	*LS47, *LS48, *LS49	4511	CMOS	16
HC4514	1-of-16 Decoder/Demultiplexer with Address Latch	*LS154, *LS159	4514, *4515	LS/CMOS	24
HC4543	BCD-to-Seven-Segment Latch/Decoder/Display Driver for Liquid-Crystal Displays	*LS47, *LS48, *LS49	4543	CMOS	16

* Suggested alternative

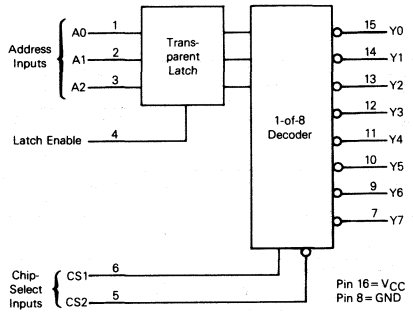
Device	HC42	HC137	HC138	HCT138	HC139	HC147
#Pins	16	16	16	16	16	16
Input Description	BCD Address	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address	2-Bit Binary Address	Any Combination of 9 Inputs
Output Description	One of 10	One of 8	One of 8	One of 8	One of 4	BCD Address of Highest Input
Single Device Dual Device	•	•	•	•	• •	•
Address Input Latch Active-High Latch Enable Active-Low Latch Enable		• •				
Active-Low Inputs						•
Active-Low Outputs Active-High Outputs	•	•	•	•	•	•
Active-Low Output Enable Active-High Output Enable		• •	•• •	•• •	•	
Active-Low Reset						
Active-Low Blanking Input						
Active-Low Lamp-Test Input						
Phase Input (for LCD's)						
LSTTL-Compatible Inputs				•		

Device	HC154	HC237	HC259	HC4511	HC4514	HC4543
# Pins	24	16	16	16	24	16
Input Description	4-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address	BCD Data	4-Bit Binary Address	BCD Data
Output Description	One of 16	One of 8	One of 8	7-Segment Display	One of 16	7-Segment Display
Single Device Dual Device	•	•	•	•	•	•
Address Input Latch Active-High Latch Enable Active-Low Latch Enable		• •		• •	• •	• •
Active-Low Inputs						
Active-Low Outputs Active-High Outputs	• 	 •	 •	 •	 •	 •
Active-Low Output Enable Active-High Output Enable	•• 	• •	•		•	
Active-Low Reset			•			
Active-Low Blanking Input				•		•
Active-Low Lamp-Test Input				•		
Phase Input (for LCD's)						•
LSTTL-Compatible Inputs						

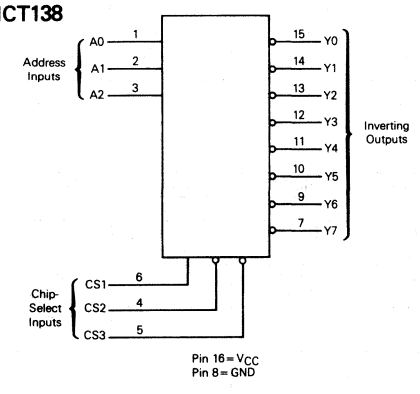
HC42



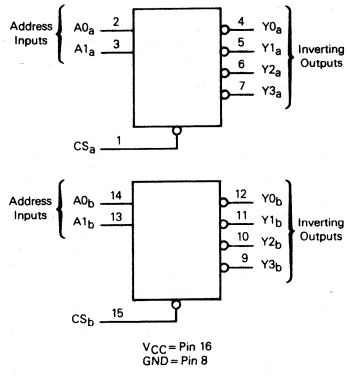
HC137



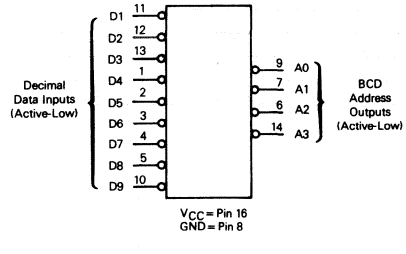
HC138
HCT138



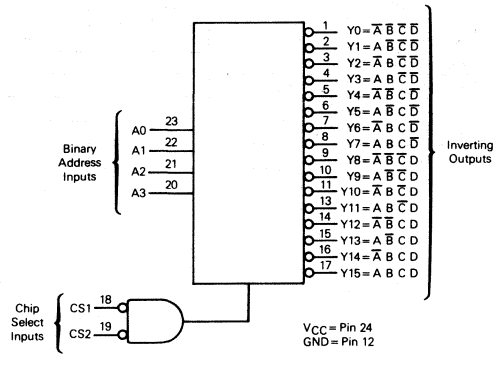
HC139



HC147

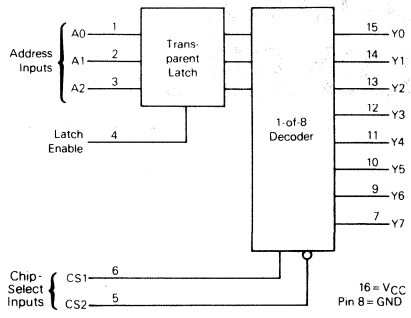


HC154

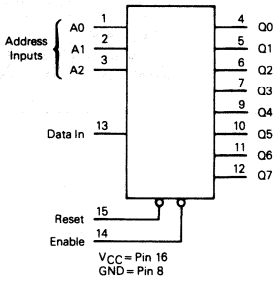


DECODERS/DEMULTIPLEXERS/DISPLAY DRIVERS (CONTINUED)

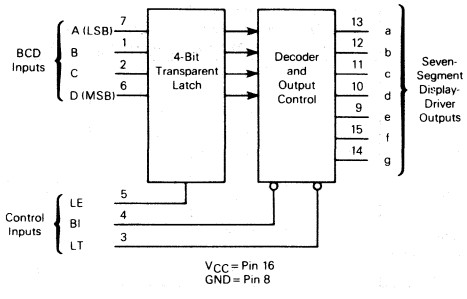
HC237



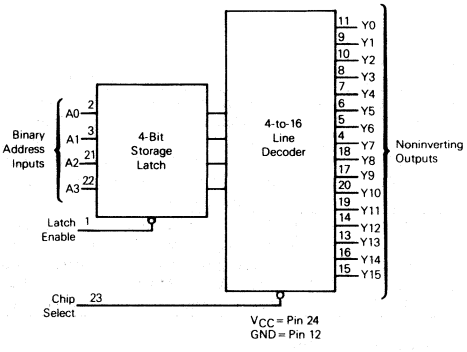
HC259



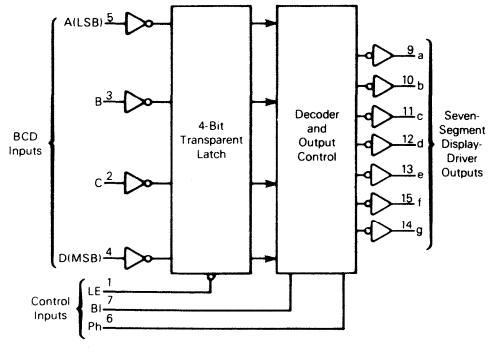
HC4511



HC4514



HC4543



ANALOG SWITCHES/ MULTIPLEXERS/ DEMULTIPLEXERS

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC4016	Quad Analog Switch/Multiplexer/Demultiplexer		4016,4066	CMOS	14
HC4051	8-Channel Analog Multiplexer/Demultiplexer		4051	CMOS	16
HC4052	Dual 4-Channel Analog Multiplexer/Demultiplexer		4052	CMOS	16
HC4053	Triple 2-Channel Analog Multiplexer/Demultiplexer		4053	CMOS	16
HC4066	Quad Analog Switch/Multiplexer/Demultiplexer with Enhanced On-Resistance Linearity		4066,4016	CMOS	14
☆HC4316	Quad Analog Switch/Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies		*4016		16
☆HC4351	8-Channel Analog Multiplexer/Demultiplexer with Address Latch		*4051		18
☆HC4352	Dual 4-Channel Analog Multiplexer/Demultiplexer with Address Latch		*4052		18
☆HC4353	Triple 2-Channel Analog Multiplexer/Demultiplexer with Address Latch		*4053		18

*Suggested alternative

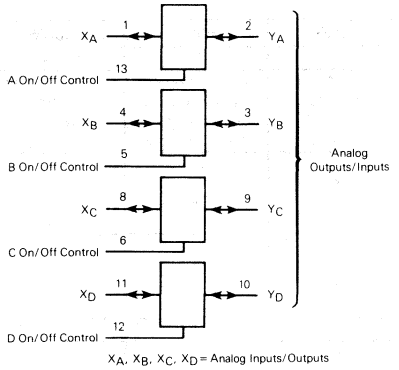
☆High-Speed CMOS design only

Device	HC4016	HC4051	HC4052	HC4053	HC4066
#Pins	14	16	16	16	14
Description	4 Independently Controlled Switches	A 3-Bit Address Selects One of 8 Switches	A 2-Bit Address Selects One of 4 Switches	A 3-Bit Address Selects Varying Combinations of the 6 Switches	4 Independently Controlled Switches
Single Device		•			
Dual Device			•		
Triple Device				•	
Quad Device	•				•
1-to-1 Multiplexing	•				•
2-to-1 Multiplexing				•	
4-to-1 Multiplexing			•		
8-to-1 Multiplexing		•			
Active-High ON/OFF Control	•				•
Common Address Inputs			•	•	
2-Bit Binary Address			•		
3-Bit Binary Address		•		•	
Address Latch with Active-Low Latch Enable					
Common Switch Enable		•	•	•	
Active-Low Enable		•	•	•	
Active-High Enable					
Separate Analog and Control Reference Power Supplies		•	•	•	
Switched tubs (for R_{ON} and Prop. Delay Improvement)					•

Device	HC4316	HC4351	HC4352	HC4353
#Pins	16	18	18	18
Description	4 Independently Controlled Switches. (Has a separate Analog Lower Power Supply)	A 3-Bit Address Selects One of 8 Switches. (Has an Address Latch)	A 2-Bit Address Selects One of 4 Switches. (Has an Address Latch)	A 3-Bit Address Selects Varying Combinations of the 6 Switches. (Has an Address Latch)
Single Device		•		
Dual Device			•	
Triple Device				•
Quad Device	•			
1-to-1 Multiplexing	•			
2-to-1 Multiplexing				•
4-to-1 Multiplexing			•	
8-to-1 Multiplexing		•		
Active-High ON/OFF Control	•			
Common Address Inputs			•	•
2-Bit Binary Address			•	
3-Bit Binary Address		•		•
Address Latch with Active-Low Latch Enable		•	•	•
Common Switch Enable	•	••	••	••
Active-Low Enable	•	•	•	•
Active-High Enable		•	•	•
Separate Analog and Control Reference Power Supplies	•	•	•	•
Switched tubs (for R_{ON} and Prop. Delay Improvement)				

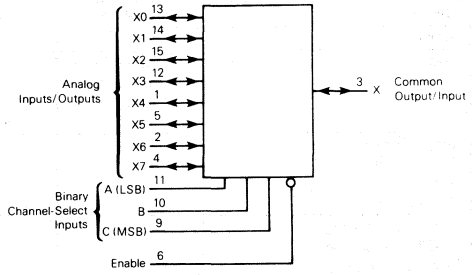
ANALOG SWITCHES/MULTIPLEXERS/DEMULTIPLEXERS (CONTINUED)

HC4016



X_A, X_B, X_C, X_D = Analog Inputs/Outputs
V_{CC} = Pin 14
GND = Pin 7

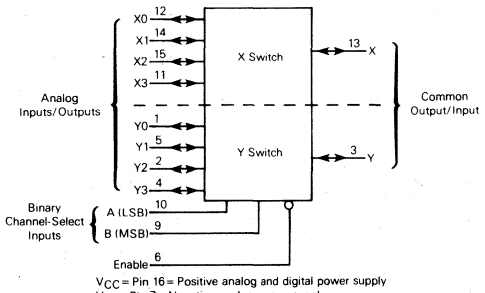
HC4051



V_{CC} = Pin 16 = Positive analog and digital power supply
V_{EE} = Pin 7 = Negative analog power supply
GND = Pin 8 = Negative digital power supply

NOTE: Control inputs are referenced to GND. Analog inputs/outputs are referenced to V_{EE}. V_{EE} must be ≤ GND.

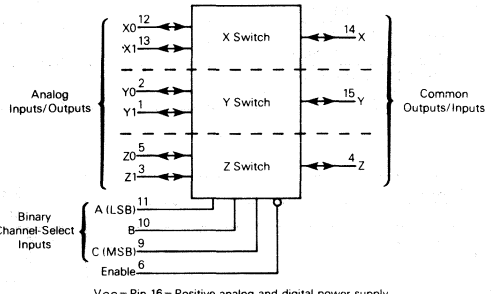
HC4052



V_{CC} = Pin 16 = Positive analog and digital power supply
V_{EE} = Pin 7 = Negative analog power supply
GND = Pin 8 = Negative digital power supply

NOTE: Control inputs are referenced to GND. Analog inputs/outputs are referenced to V_{EE}. V_{EE} must be ≤ GND.

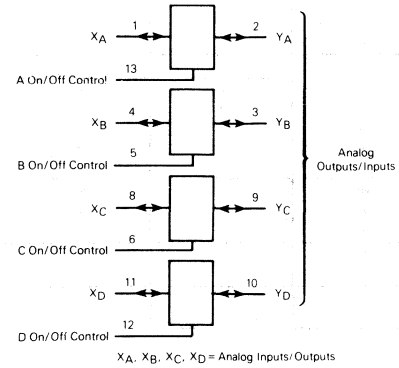
HC4053



V_{CC} = Pin 16 = Positive analog and digital power supply
V_{EE} = Pin 7 = Negative analog power supply
GND = Pin 8 = Negative digital power supply

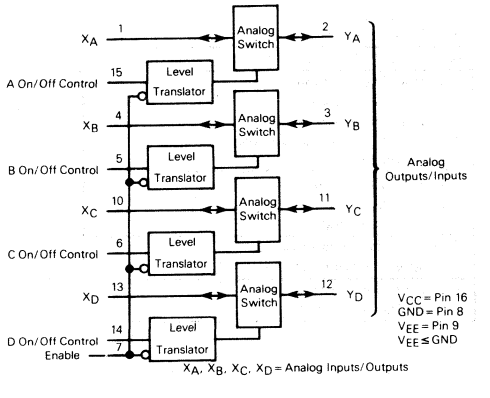
NOTE: Control inputs are referenced to GND. Analog inputs/outputs are referenced to V_{EE}. V_{EE} must be ≤ GND.

HC4066



X_A, X_B, X_C, X_D = Analog Inputs/Outputs
V_{CC} = Pin 14
GND = Pin 7

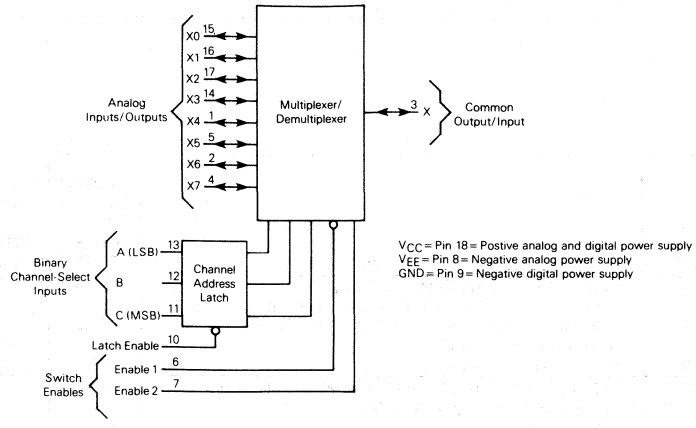
HC4316



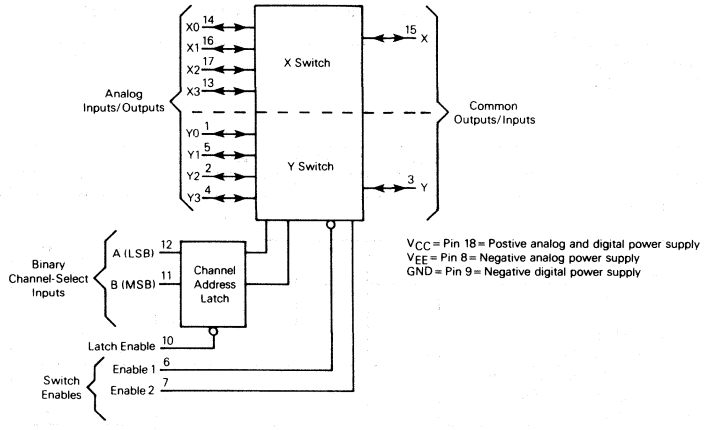
V_{CC} = Pin 16
GND = Pin 8
V_{EE} = Pin 9
V_{EE} ≤ GND

X_A, X_B, X_C, X_D = Analog Inputs/Outputs

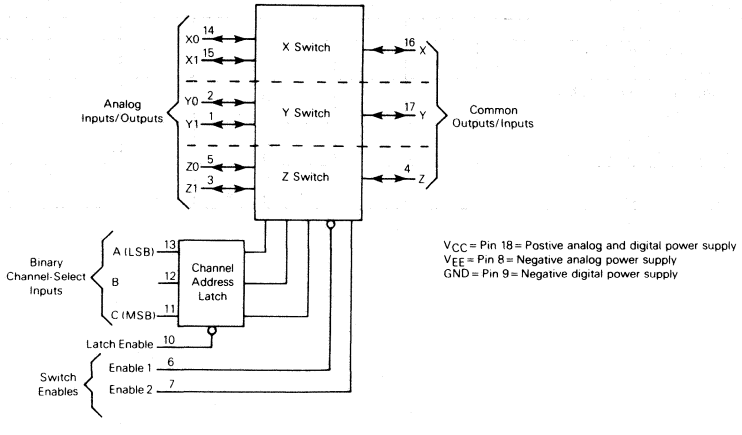
HC4351



HC4352



HC4353



NOTE: Control inputs are referenced to GND. Analog inputs/outputs are referenced to V_{EE}. V_{EE} must be $\leq$ GND.

SHIFT REGISTERS

1

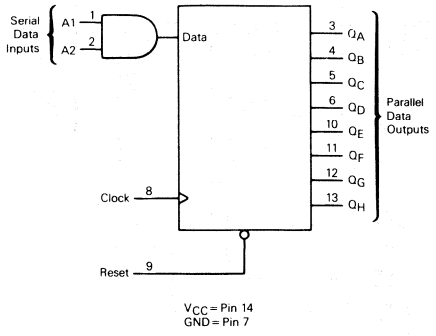
Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC164	8-Bit Serial-Input/Parallel-Output Shift Register	LS164	*4034	LS	14
HC165	8-Bit Serial- or Parallel-Input/Serial-Output Shift Register	LS165	*4021	LS	16
HC166	8-Bit Serial- or Parallel-Input/Serial-Output Shift Register with Reset	LS166	*4021	LS	16
HC194	4-Bit Bidirectional Universal Shift Register	LS194A	4194	LS/CMOS	16
HC195	4-Bit Universal Shift Register	LS195A	*4035	LS	16
HC299	8-Bit Bidirectional Universal Shift Register with 3-State Parallel Outputs	LS299		LS	20
☆HC589	8-Bit Serial- or Parallel-Input/Serial-Output Shift Register with 3-State Output	*LS597			16
HC595	8-Bit Serial-Input/Serial- or Parallel-Output Shift Register with Latched 3-State Outputs	LS595	*4034	LS	16
HC597	8-Bit Serial- or Parallel-Input/Serial-Output Shift Register with Input Latch	LS597		LS	16

*Suggested alternative
☆High-Speed CMOS design only

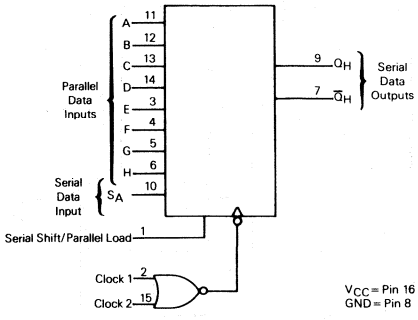
Device	HC164	HC165	HC166	HC194	HC195	HC299	HC589	HC595	HC597
#Pins	14	16	16	16	16	20	16	16	16
4-Bit Register				•	•				
8-Bit Register	•	•	•			•	•	•	•
Serial Data Input	•	•	•	•	•	••	•	•	•
Parallel Data Inputs		•	•	•	•	•	•		•
Serial Output Only		•	•				•		•
Parallel Outputs	•			•	•	•		•	
Inverting Output		•			•				
Noninverting Output	•	•	•	•	•	•	•	•	•
Serial Shift/Parallel Load Control		•	•	•	•	•	•		•
Shifts One Direction Only	•	•	•		•		•	•	•
Shifts Both Directions				•		•			
Positive-Transition Clocking	•	•	•	•	•	•	•	•	•
Active-High Clock Enable		•	•						
Input Data Enable	•								
Data Latch with Active-High Latch Clock							•		•
Output Latch with Active-High Latch Clock								•	
3-State Outputs						•	•	•	
Active-Low Output Enable						••	•	•	
Active-High Reset									
Active-Low Reset	•		•	•	•	•		•	•

SHIFT REGISTERS (CONTINUED)

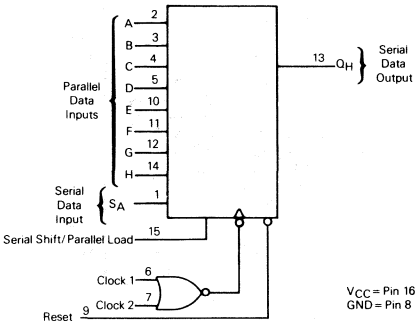
HC164



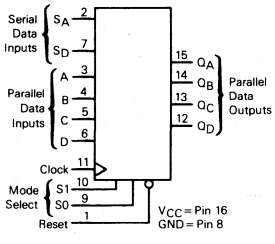
HC165



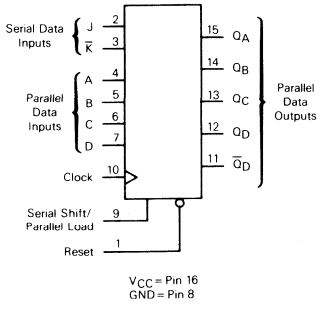
HC166



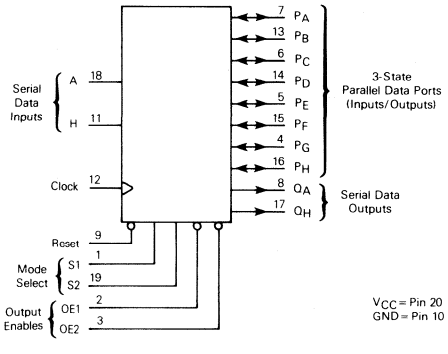
HC194



HC195

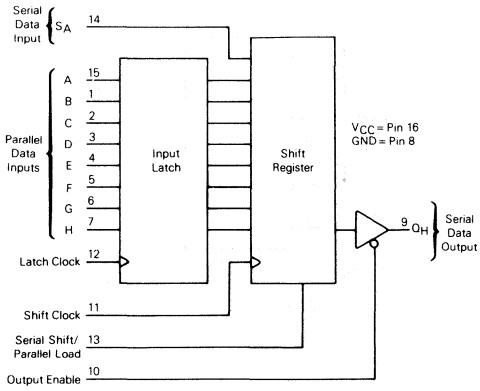


HC299

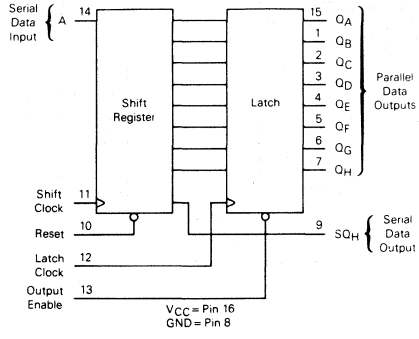


SHIFT REGISTERS (CONTINUED)

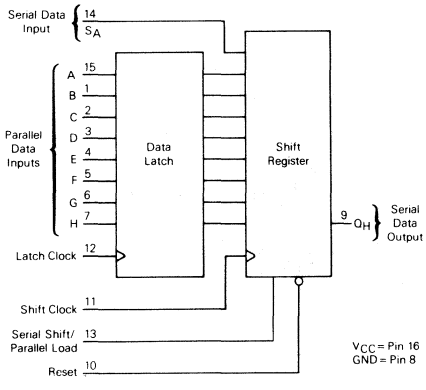
HC589



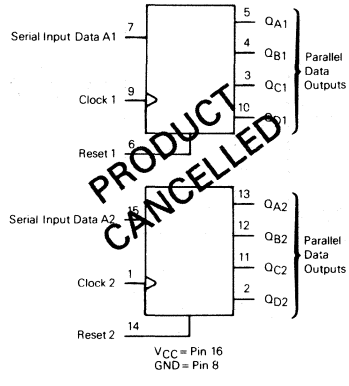
HC595



HC597



HC4015



PRODUCT CANCELLED

COUNTERS

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC160	Presettable BCD Counter with Asynchronous Reset	LS160A	4160	LS/CMOS	16
HC161	Presettable 4-Bit Binary Counter with Asynchronous Reset	LS161A	4161	LS/CMOS	16
HC162	Presettable BCD Counter with Synchronous Reset	LS162A	4162	LS/CMOS	16
HC163	Presettable 4-Bit Binary Counter with Synchronous Reset	LS163A	4163	LS/CMOS	16
HC190	Presettable BCD Up/Down Counter	LS190	*4510	LS	16
HC191	Presettable 4-Bit Binary Up/Down Counter	LS191	*4516	LS	16
HC192	Presettable BCD Up/Down Counter with Reset	LS192	*4510	LS	16
HC193	Presettable 4-Bit Binary Up/Down Counter with Reset	LS193	*4516	LS	16
HC390	Dual 4-Stage Binary Ripple Counter with ÷ 2 and ÷ 5 Sections	LS390		LS	16
HC393	Dual 4-Stage Binary Ripple Counter	LS393	*4520	LS	14
HC4017	Decade Counter/Divider		4017	CMOS	16
HC4020	14-Stage Binary Ripple Counter		4020	CMOS	16
HC4024	7-Stage Binary Ripple Counter		4024	CMOS	14
HC4040	12-Stage Binary Ripple Counter		4040	CMOS	16
HC4060	14-Stage Binary Ripple Counter with Oscillator		4060	CMOS	16
HC4518	Dual BCD Counter		4518	CMOS	16
HC4520	Dual 4-Bit Binary Counter		4520	CMOS	16

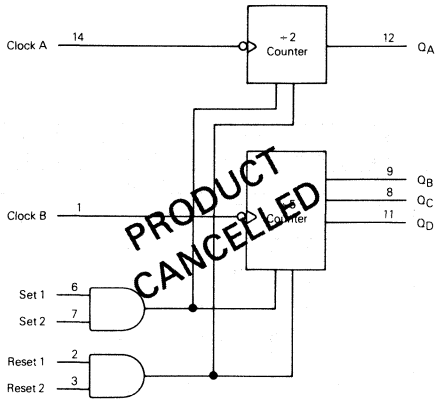
* Suggested alternative

Device	HC 160	HC 161	HC 162	HC 163	HC 190	HC 191	HC 192
#Pins	16	16	16	16	16	16	16
Single Device Dual Device	•	•	•	•	•	•	•
Ripple Counter Number of Ripple Counter Internal Stages Number of Stages with Available Outputs							
Count Up Count Down	•	•	•	•	• •	• •	• •
4-Bit Binary Counter BCD Counter Decimal Counter	•	•	•	•	•	•	•
Separate ÷ 2 Section Separate ÷ 5 Section Separate ÷ 6 Section Separate ÷ 8 Section							
On-Chip Oscillator Capability							
Separate Count-Up and Count-Down Clocks							•
Count Up/Count Down Control Input					•	•	
Positive-Transition Clocking Negative-Transition Clocking Active-High Clock Enable Active-Low Clock Enable	•	•	•	•	•	•	•
Active-High Count Enable Active-Low Count Enable	••	••	••	••	•	•	
Active-High Set Active-High Reset	•	•	•	•			•
4-Bit Binary Preset Data Inputs BCD Preset Data Inputs Active-Low Load Preset	• •	• •	• •	• •	• •	• •	• •
Carry Output Borrow Output Ripple Clock Output	•	•	•	•	• •	• •	• •

Device	HC 193	HC 390	HC 393	HC 4017	HC 4020	HC 4024	HC 4040	HC 4060	HC 4518	HC 4520
#Pins	16	16	14	16	16	14	16	16	16	16
Single Device	•			•	•	•	•	•		
Dual Device		•	•						•	•
Ripple Counter		•	•		•	•	•	•		
Number of Ripple Counter Internal Stages		4	4		14	7	12	14		
Number of Stages with Available Outputs		4	4		12	7	12	10		
Count Up	•	•	•	•	•	•	•	•	•	•
Count Down	•									
4-Bit Binary Counter	•		•							•
BCD Counter		•							•	
Decimal Counter				•						
Separate ÷ 2 Section		•								
Separate ÷ 5 Section		•								
Separate ÷ 6 Section										
Separate ÷ 8 Section										
On-Chip Oscillator Capability								•		
Separate Count-Up and Count-Down Clocks	•									
Count Up/Count Down Control Input										
Positive-Transition Clocking	•			•					•	•
Negative-Transition Clocking		•	•	•	•	•	•	•	•	•
Active-High Clock Enable				•					•	•
Active-Low Clock Enable				•					•	•
Active-High Count Enable										
Active-Low Count Enable										
Active-High Set										
Active-High Reset	•	•	•	•	•	•	•	•	•	•
4-Bit Binary Preset Data Inputs	•									
BCD Preset Data Inputs										
Active-Low Load Preset	•									
Carry Output	•									
Borrow Output	•									
Ripple Clock Output										

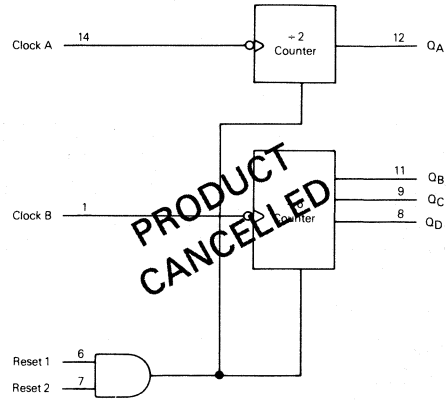
COUNTERS (CONTINUED)

HC90



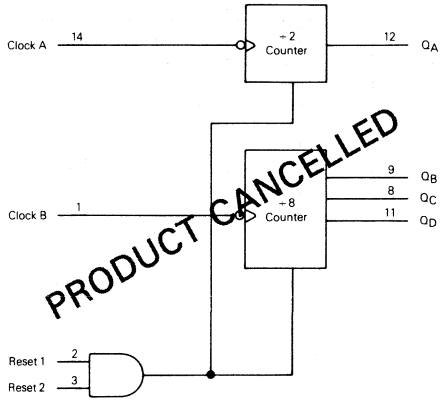
V_{CC} = Pin 5
GND = Pin 10
No Connection = Pins 4, 13

HC92



V_{CC} = Pin 5
GND = Pin 10
No Connection = Pins 2, 3, 4, 13

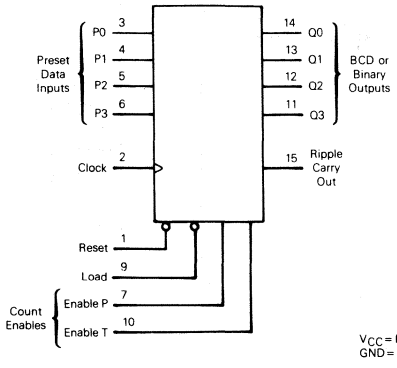
HC93



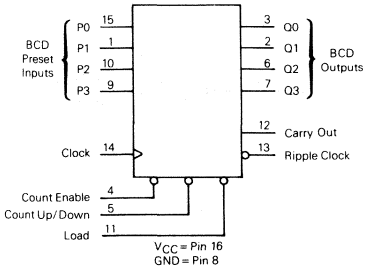
V_{CC} = Pin 5
GND = Pin 10
No Connection = Pins 4, 6, 7, 13

COUNTERS (CONTINUED)

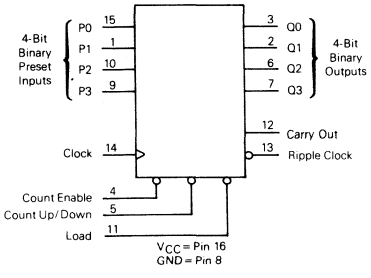
HC160 HC162
HC161 HC163



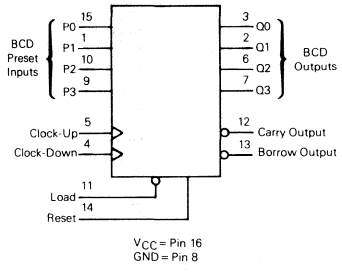
HC190



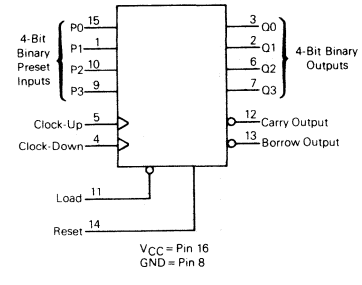
HC191



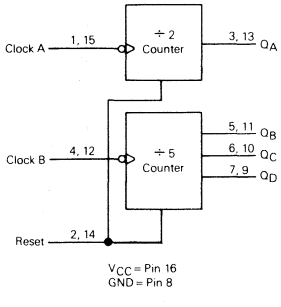
HC192



HC193

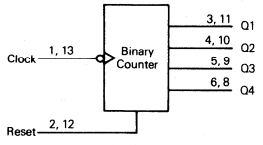


HC390



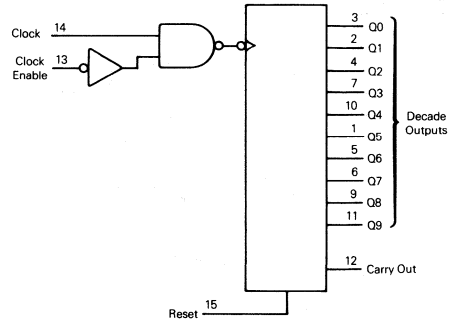
COUNTERS (CONTINUED)

HC393



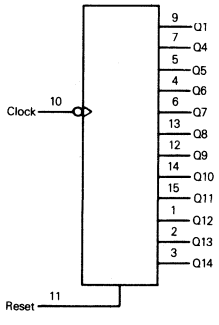
V_{CC} = Pin 14
GND = Pin 7

HC4017



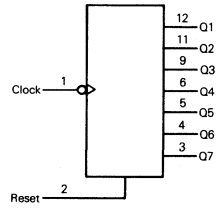
V_{CC} = Pin 16
GND = Pin 8

HC4020



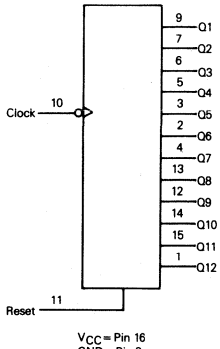
V_{CC} = Pin 16
GND = Pin 8

HC4024



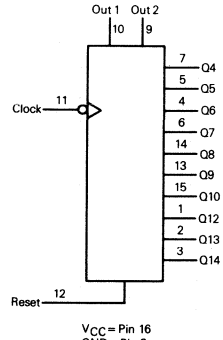
V_{CC} = Pin 14
GND = Pin 7
No Connection = Pins 8, 10 and 13

HC4040



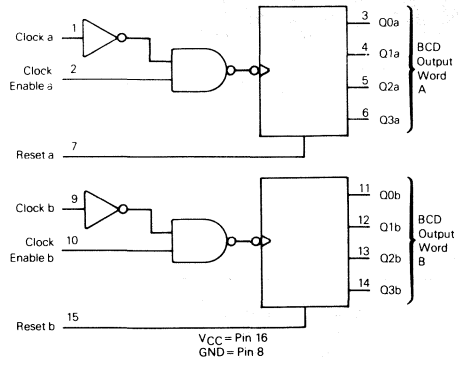
V_{CC} = Pin 16
GND = Pin 8

HC4060

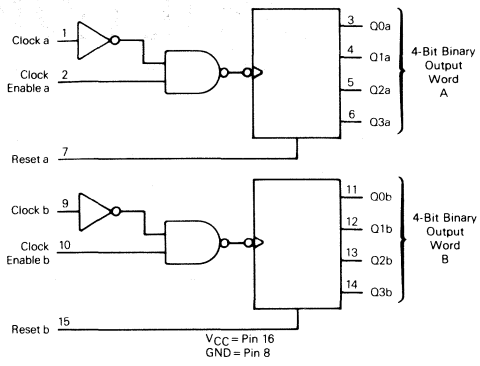


V_{CC} = Pin 16
GND = Pin 8

HC4518



HC4520



MONOSTABLE MULTIVIBRATORS

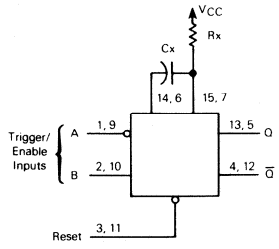
Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC123	Dual Retriggerable Monostable Multivibrator	LS123	*4538, *4528	LS	16
HC221	Dual Monostable Multivibrator	LS221	*4538, *4528	LS	16
HC423	Dual Retriggerable Monostable Multivibrator	LS423	*4538 *4528	LS	16
HC4538	Dual Precision Monostable Multivibrator (Retriggerable, Resettable)	*LS423	4538, 4528	CMOS	16

*Suggested alternative

Device	HC123	HC221	HC423	HC4538
#Pins	16	16	16	16
Dual Device	•	•	•	•
Precision Pulse Width				•
Retriggerable	•		•	•
Positive-Transition Trigger	•	•	•	•
Negative-Transition Trigger	•	•	•	•
Active-Low Trigger Enable	•	•	•	•
Active-High Trigger Enable	•	•	•	•
Active-Low Reset	•	•	•	•
Triggerable by Reset Pin	•	•		
Inverting Output	•	•	•	•
Noninverting Output	•	•	•	•

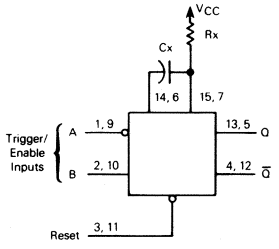
MONOSTABLE MULTIVIBRATORS (CONTINUED)

HC123



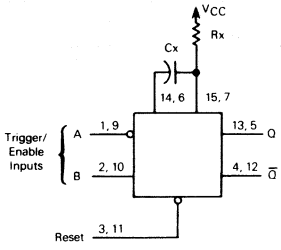
V_{CC} = Pin 16
GND = Pin 8

HC221



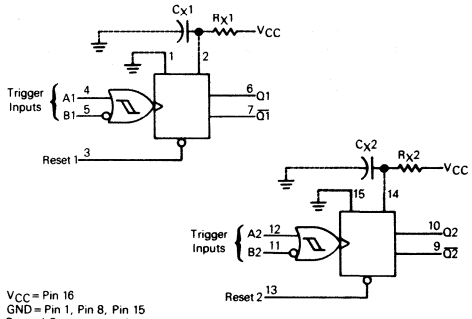
V_{CC} = Pin 16
GND = Pin 8

HC423



V_{CC} = Pin 16
GND = Pin 8

HC4538



V_{CC} = Pin 16
GND = Pin 1, Pin 8, Pin 15
R_X and C_X are external components

ARITHMETIC CIRCUITS

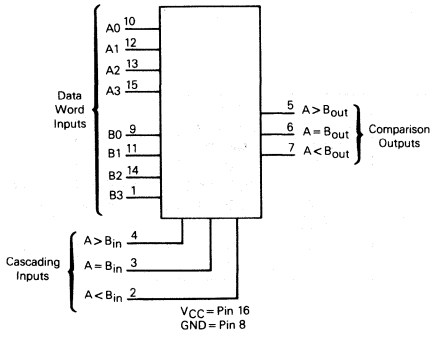
1

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC85	4-Bit Magnitude Comparator	LS85	*4585	LS	16
HC181	4-Bit Arithmetic Logic Unit	LS181	4581	LS/CMOS	24
HC182	Carry Lookahead Generator	LS182	4582	LS/CMOS	16
HC280	9-Bit Odd/Even Parity Generator/Checker	LS280	*4531	LS	14
HC283	4-Bit Binary Full Adder with Fast Carry	LS283, LS83	4008	LS283	16
HC688	8-Bit Equality Comparator	LS688		LS	20
HCT688	8-Bit Equality Comparator with LSTTL-Compatible Inputs	LS688		LS	20

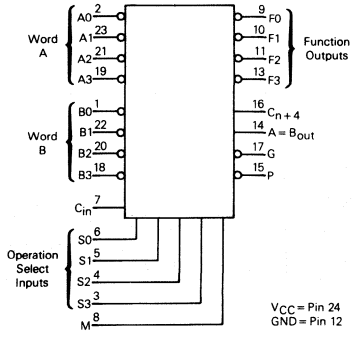
* Suggested alternative

ARITHMETIC CIRCUITS (CONTINUED)

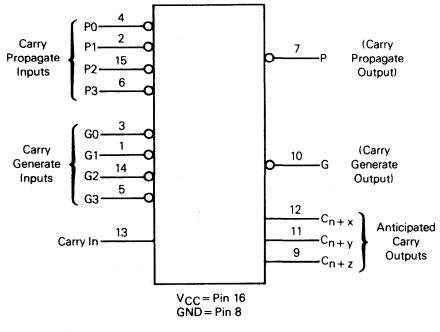
HC85



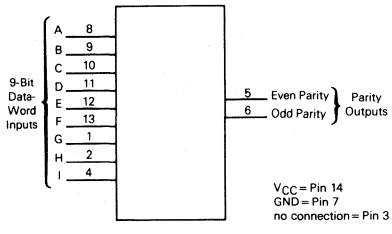
HC181



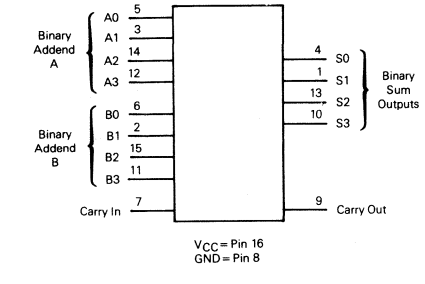
HC182



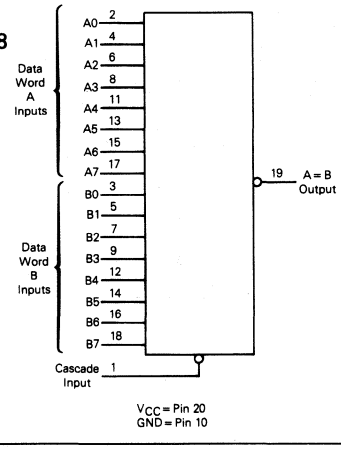
HC280



HC283



HC688
HCT688



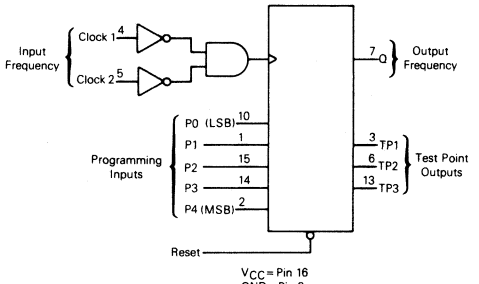
MISCELLANEOUS DEVICES

1

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC292	Programmable Frequency Divider/Digital Timer	LS292		LS	16
HC294	Programmable Frequency Divider/Digital Timer	LS294		LS	16
HC4046	Phase-Locked Loop	*LS297	4046	CMOS	16

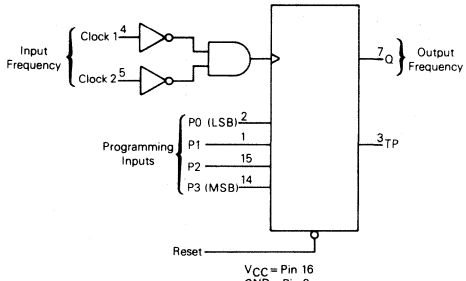
*Suggested alternative

HC292



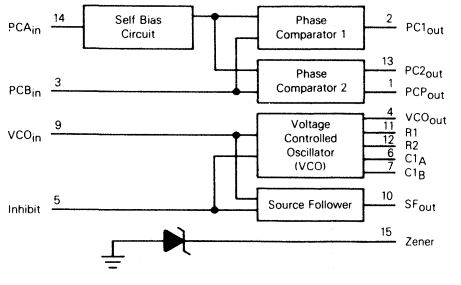
V_{CC} = Pin 16
GND = Pin 8
No Connection = Pin 9, 12

HC294



V_{CC} = Pin 16
GND = Pin 8
Pins 6, 9, 10, 12, 13 = No Connection

HC4046



V_{CC} = Pin 16
GND = Pin 8

LSTTL INPUT-COMPATIBLE DEVICES

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HCT00	Quad 2-Input NAND Gate with LSTTL-Compatible Inputs	LS00	4001	LS	14
HCT04	Hex Inverter with LSTTL-Compatible Inputs	LS04	*4069	LS/CMOS	14
HCT34	Hex Buffer with LSTTL-Compatible Inputs	LS07	*4050	LS	14
HCT138	1-of-8 Decoder/Demultiplexer with LSTTL-Compatible Inputs	LS138	*4028	LS	16
HCT240	Octal 3-State Inverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	LS240		LS	20
HCT241	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	LS241		LS	20
HCT244	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	LS244		LS	20
HCT245	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS245		LS	20
HCT373	Octal 3-State Noninverting D-Type Transparent Latch with LSTTL-Compatible Inputs	LS373, LS573		LS373	20
HCT374	Octal 3-State Noninverting D-Type Flip-Flop with LSTTL-Compatible Inputs	LS374, LS574		LS374	20
HCT640	Octal 3-State Inverting Bus Transceiver with LSTTL-Compatible Inputs	LS640		LS	20
HCT643	Octal 3-State Inverting and Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS643		LS	20
HCT688	8-Bit Equality Comparator with LSTTL-Compatible Inputs	LS688		LS	20

* Suggested alternative

The "Better" Program

2

2

The "BETTER" Program

Motorola's reliability and quality-enhanced program was developed to provide improved levels of quality and reliability for standard commercial products.

The "BETTER" program is offered on High-Speed CMOS in dual-in-line ceramic and plastic packages.

Motorola standard commercial integrated circuits are manufactured under stringent in-process controls and quality inspections combined with the industry's finest outgoing quality inspections. The "BETTER" program offers three levels of extra processing each tailored to meet different user needs at nominal costs.

The program is designed to:

- Eliminate Incoming Electrical Inspection
- Estimate Need for Independent Test Labs and Associated Extra Time and Costs
- Reduce Field Failures
- Reduce Service Calls
- Reduce Equipment Downtime
- Reduce Board and System Rework
- Reduce Infant Mortality
- Save Time and Money
- Increase End-Customer Satisfaction

BETTER PROCESSING — STANDARD PRODUCT PLUS:

100% Screen	Level I "S"	Level II "D"	Level III "DS"
Temp Cycle 10 Cycles −25°C to +150°C	X		X
25°C Functional and Parametric Test	X	X	X
High Temperature Test*	X		X
Burn-In — MIL-STD-883B		X	X
25°C Post Burn-In Functional and Parametric Test		X	X
Tightened QA Sample	X	X	X

*Functional and parametric test at 100°C for the 74HC series and 125°C for the 54HC series.

"BETTER" AQL GUARANTEES

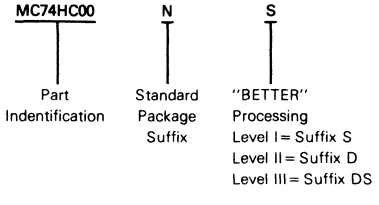
Test	Condition	AQL* Level I	AQL* Level II	AQL* Level III
High Temperature Functional	T_A = 100°C or T_A Max	0.065		0.065
DC Parametric	T_A = 25°C	0.065	0.065	0.065
DC Parametric	T_A Min, T_A Max	0.39	0.39	0.39
AC Parametric	T_A = 25°C	0.065	0.065	0.065
External Visual and Mechanical	Major/Minor	0.065	0.065	0.065
Hermeticity (Not Applicable to Plastic Packages)	Gross/Fine	0.15	0.15	0.15

"AQL" values shown are for reference only. "LTPD" type sampling plans that are equal to or tighter than values indicated may be used. Also, the guaranteed electrical and visual/mechanical AQL levels will be progressively tightened. Contact your nearest Motorola sales office for current values.

PART MARKING

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

HOW TO ORDER



Military/Hi-Rel Selector Guide

3

Military/Hi Rel CMOS Selector Guide

HIGH-SPEED CMOS 883B PROCESSED

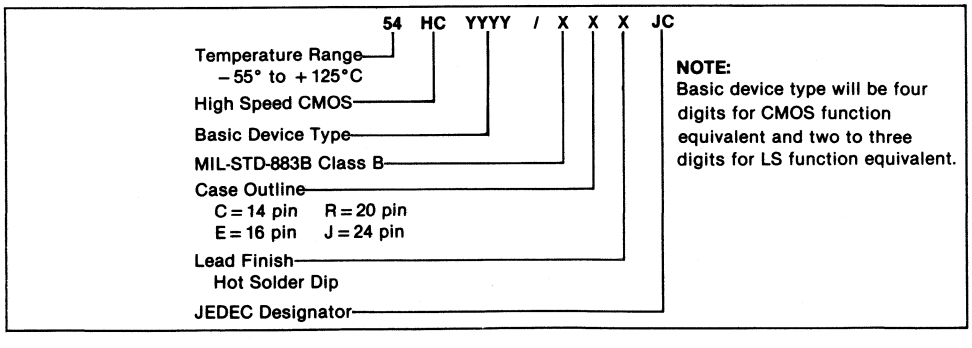
Parts shown are functional equivalent *except* when preceded by an asterisk (*), indicating a suggested alternative.

Military Part Number	Function	Functional Equivalent LSTTL Device	Functional Equivalent CMOS Device	Direct Pin Compatibility
54HC00/BCAJC	Quad 2-Input NAND Gate	LS00	4011	LS
54HC02/BCAJC	Quad 2-Input NOR Gate	LS02	4001	LS
54HC04/BCAJC	Hex Inverter	LS04	4069	LS/CMOS
54HC08/BCAJC	Quad 2-Input AND Gate	LS08	4081	LS
54HC10/BCAJC	Triple 3-Input NAND Gate	LS10	4023	LS
54HC11/BCAJC	Triple 3-Input AND Gate	LS11	4073	LS
54HC14/BCAJC	Hex Schmitt-Trigger Inverter	LS14	4584	LS/CMOS
54HC20/BCAJC	Dual 4-Input NAND Gate	LS20	4012	LS
54HC27/BCAJC	Triple 3-Input NOR Gate	LS27	4025	LS
54HC30/BCAJC	8-Input NAND Gate	LS30	4068	LS
54HC32/BCAJC	Quad 2-Input OR Gate	LS32	4071	LS
54HC42/BEAJC	1-of-10 Decoder	LS42	*4028	LS
54HC73/BCAJC	Dual J-K Flip-Flop with Clear	LS73A	*4027	LS
54HC74/BCAJC	Dual D-Type Flip-Flop with Set and Clear, Positive-Edge Triggered	LS74A	4013	LS
54HC75/BEAJC	4-Bit D-Type Latch	LS75	*4042	LS
54HC76/BEAJC	Dual J-K Flip-Flop with Set and Clear	LS76A	*4027	LS
54HC85/BEAJC	4-Bit Magnitude Comparator	LS85	*4585	LS
54HC86/BCAJC	Quad 2-Input Exclusive OR Gate	LS86	4070	LS
54HC107/BCAJC	Dual J-K Flip-Flop with Clear	LS107A	4027	LS
54HC109/BEAJC	Dual J-$\overline{K}$ Flip-Flop with Set and Clear, Positive-Edge Triggered	LS109A	*4027	LS
54HC112/BEAJC	Dual J-K Flip-Flop with Set and Clear, Negative-Edge Triggered	LS112A	*4027	LS
54HC123/BCAJC	Dual Monostable Multivibrator	LS123	*4528	LS
54HC132/BCAJC	Quad 2-Input Schmitt-Trigger NAND Gate	LS132	4093	LS
54HC133/BEAJC	13-Input NAND Gate	LS133		LS
54HC138/BEAJC	1-of-8 Decoder	LS138	*4028	LS
54HC139/BEAJC	Dual 1-of-4 Decoder	LS139	4555	LS/CMOS
54HC147/BEAJC	10-to-4 Priority Encoder	LS147	*4532	LS
54HC151/BEAJC	8-Input Multiplexer	LS151	*4512	LS
54HC153/BEAJC	Dual 4-Input Multiplexer	LS153	4539	LS/CMOS
54HC154/BJAJC	4-to-16 Decoder	LS154	*4514	LS
54HC157/BEAJC	Quad 2-Input Data Selector/Multiplexer	LS157		LS
54HC158/BEAJC	Quad 2-Input Data Selector/Multiplexer, Inverting Output	LS158		LS
54HC160/BEAJC	Decade Counter, Asynchronous Clear	LS160A	4160	LS/CMOS
54HC161/BEAJC	4-Bit Binary Counter, Asynchronous Clear	LS161A	4161	LS/CMOS
54HC162/BEAJC	Decade Counter, Synchronous Clear	LS162A	4162	LS/CMOS
54HC163/BEAJC	4-Bit Binary Counter, Synchronous Clear	LS163A	4163	LS/CMOS
54HC164/BCAJC	8-Bit Serial-to-Parallel Shift Register	LS164	*4034	LS
54HC165/BEAJC	Parallel-Load 8-Bit Shift Register	LS165	*4021	LS
54HC173/BEAJC	4-Bit D-Type Register, 3-State	LS173	4076	LS/CMOS
54HC174/BEAJC	Hex D-Type Flip-Flop	LS174	4174	LS/CMOS
54HC175/BEAJC	Quad D-Type Flip-Flop	LS175	4175	LS/CMOS
54HC192/BEAJC	BCD Decade Up/Down Counter	LS192	4510	LS
54HC193/BEAJC	4-Bit Binary Up/Down Counter	LS193	4516	LS
54HC194/BEAJC	4-Bit Bidirectional Universal Shift Register	LS194A	4194	LS/CMOS
54HC195/BEAJC	4-Bit Universal Shift Register	LS195A	*4035	LS
54HC221/BEAJC	Dual Monostable Multivibrator	LS221	*4528	LS
54HC240/BRAJC	Octal Buffer/Line Driver/Line Receiver, 3-State, Inverting Output	LS240		LS
54HC241/BRAJC	Octal Buffer/Line Driver/Line Receiver, 3-State	LS241		LS
54HC242/BCAJC	Quad Bus Transceiver, 3-State, Inverting Output	LS242		LS
54HC243/BCAJC	Quad Bus Transceiver, 3-State	LS243		LS
54HC244/BRAJC	Octal Buffer/Line Driver/Line Receiver, 3-State	LS244		LS
54HC245/BRAJC	Octal Bus Transceiver, 3-State	LS245		LS
54HC251/BEAJC	8-Input Multiplexer, 3-State	LS251	*4512	LS
54HC253/BEAJC	Dual 4-Input Multiplexer, 3-State	LS253	*4539	LS/CMOS

HIGH-SPEED CMOS (continued)

Military Part Number	Function	Functional Equivalent LSTTL Device	Functional Equivalent CMOS Device	Direct Pin Compatibility
54HC257/BEAJC	Quad 2-Input Data Selector/Multiplexer, 3-State	LS257	*4519	LS
54HC259/BEAJC	8-Bit Addressable Latch	LS259	*4099	LS
54HC266/BCAJC	Quad 2-Input Exclusive NOR Gate	LS266	4077	LS/CMOS
54HC280/BCAJC	9-Bit Odd/Even Parity Generator/Checker	LS280	*4531	LS
54HC299/BRAJC	8-Bit Universal Shift/Store Register, 3-State	LS299	*4094	LS
54HC354/BRAJC	8-Input Multiplexer, 3-State	LS354	*4512	LS
54HC356/BRAJC	8-Input Multiplexer, 3-State	LS356	*4512	LS
54HC365/BEAJC	Hex 3-State Bus Driver with Common 2-Input NOR Enable	LS365A		LS
54HC366/BEAJC	Hex 3-State Bus Driver with Common 2-Input NOR Enable, Inverting Output	LS366A		LS
54HC367/BEAJC	Hex 3-State Bus Driver with Separate 2-Bit and 4-Bit Sections	LS367A	4503	LS/CMOS
54HC368/BEAJC	Hex 3-State Bus Driver with Separate 2-Bit and 4-Bit Sections, Inverting Output	LS368A		LS
54HC373/BRAJC	Octal D-Type Transparent Latch, 3-State	LS373		LS
54HC374/BCAJC	Octal D-Type Flip-Flop, 3-State	LS374		LS
54HC390/BEAJC	Dual Decade Counter	LS390	*4518	LS
54HC393/BCAJC	Dual 4-Bit Binary Counter	LS393	*4520	LS
54HC423/BCAJC	Dual Monostable Multivibrator	LS423	*4538	LS
54HC533/BRAJC	Octal D-Type Transparent Latch, 3-State, Inverting Output	LS533		LS
54HC534/BRAJC	Octal D-Type Flip-Flop, 3-State, Inverting Output	LS534		LS
54HC563/BRAJC	Octal D-Type Transparent Latch, 3-State, Inverting Output	LS576		LS
54HC564/BRAJC	Octal D-Type Flip-Flop, 3-State, Inverting Output	LS580		LS
54HC573/BRAJC	Octal D-Type Transparent Latch, 3-State	LS573		LS
54HC574/BRAJC	Octal D-Type Flip-Flop, 3-State	LS574		LS
54HC640/BRAJC	Octal Bus Transceiver, 3-State, Inverting Output	LS640		LS
54HC643/BRAJC	Octal Bus Transceiver, 3-State	LS643		LS
54HC646/BJAJC	Octal Bus Transceiver and Register, 3-State	LS646		LS
54HC648/BJAJC	Octal Bus Transceiver and Register, 3-State	LS648		LS
54HC688/BRAJC	8-Bit Equality Comparator			
54HC4002/BCAJC	Dual 4-Input NOR Gate	*LS25	4002	CMOS
54HC4017/BEAJC	Decade Counter/Divider		4017	CMOS
54HC4020/BEAJC	14-Stage Binary Counter		4020	CMOS
54HC4040/BEAJC	12-Stage Binary Counter		4040	CMOS
54HC4049/BEAJC	Hex Inverting Buffer		4049	CMOS
54HC4050/BEAJC	Hex Buffer		4050	CMOS
54HC4060/BEAJC	14-Stage Binary Counter		4060	CMOS
54HC4075/BCAJC	Triple 3-Input OR Gate		4075	CMOS
54HC4078/BCAJC	8-Input NOR Gate		4078	CMOS
54HC4511/BEAJC	BCD-to-7-Segment Latch/Decoder/Driver	*LS46-49	4511	LS/CMOS
54HC4514/BJAJC	4-Bit Latch/4-to-16 Line Decoder		4514	CMOS
54HC4538/BEAJC	Dual Precision Retriggerable/Resettable Monostable Multivibrator	*LS221	4538	CMOS
54HC4543/BEAJC	BCD-to-7-Segment Latch/Decoder/Driver for Liquid-Crystal Displays	*LS46-49	4543	CMOS

HOW TO ORDER MILITARY HIGH-SPEED CMOS



NOTE:
Basic device type will be four digits for CMOS function equivalent and two to three digits for LS function equivalent.

3

Design Considerations

4

INTRODUCTION

CMOS devices have been used for many years in applications where the primary concerns were for low power consumption, wide power-supply range, and high noise immunity. The drawback to using metal-gate CMOS was the fact that it was too slow for many applications. Applications requiring high-speed devices, such as microprocessor memory decoding, had to go to the faster families such as LSTTL, sacrificing the best qualities of CMOS. The logical next step in the CMOS evolution was to introduce a family of devices that were fast enough for such applications, and that retained the best features of CMOS. In order to do this, Motorola has gone to a silicon-gate process with a gate length of 3.5 microns. The results of this change can be seen in Table 1 where HSCMOS devices are compared to standard (metal gate) CMOS, LSTTL, ALS, and FAST devices.

The transition from the metal-gate process to the 3.5-micron silicon-gate process was simplified by the fact that Motorola has been using a 5-micron silicon-gate process in the production of Motorola's CMOS memory, microprocessor and logic circuits since 1978. This experience has allowed the introduction of the High-Speed CMOS family into high volume production with proven production and reliability history.

The Motorola CMOS evolutionary process is shown in Figure 1, showing that one advantage of the 3.5-micron process is device size. The High-Speed CMOS (HSCMOS) device is a little more than half the size of its metal-gate predecessor, yielding significant die area savings. In addition to this, the silicon-gate process allows smaller gate and channel lengths due to the self-aligning gate feature. This process uses the gate to define the channel during processing, eliminating registration errors and, therefore, the need for gate overlaps. The elimination of the gate overlap significantly lowers the gate capacitance, resulting in higher speed capability. The smaller gate length also results in higher drive capability per unit gate width, insuring more efficient use of chip area.

In addition to process enhancements, the input protection network and latch-up characteristics have been improved over those of Metal-Gate CMOS. Precautions should still be taken, however, to guard against electrostatic discharge and latch-up. HSCMOS devices are, however, much less susceptible to these failure modes than are the metal-gate CMOS devices.

Motorola's new High-Speed CMOS family has a broad range of functions from basic gates, flip-flops and counters to bus-compatible devices. The family is made up of devices that are identical in pinout and are functionally equivalent to LSTTL devices, as well as the most popular metal-gate devices not available in TTL, offering the designer an excellent alternative to existing families without having to become familiar with a new set of device numbers.

Another important feature of the family is that it is mutually sourced by National Semiconductor, providing the systems designer with a true alternate source for all of the HSCMOS devices and getting the parts into production in a timely manner.

FIGURE 1 — CMOS EVOLUTION

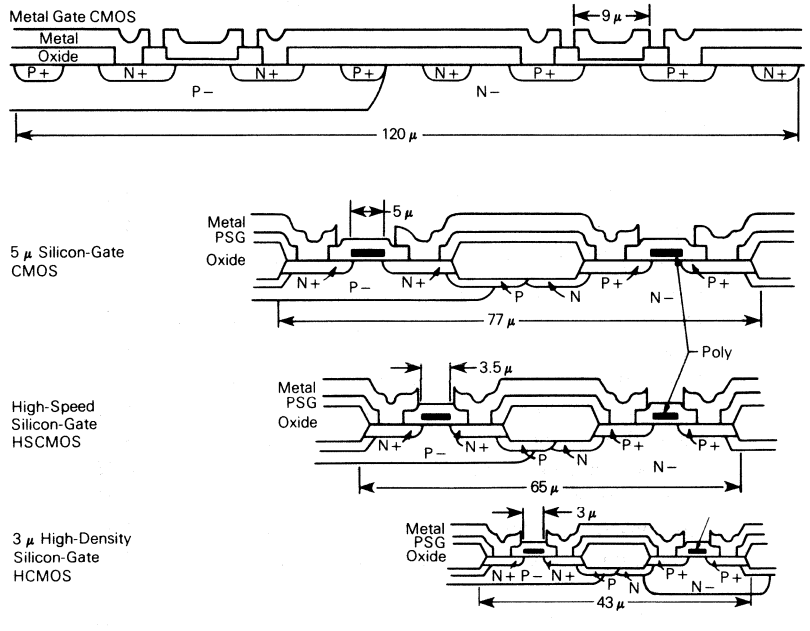


TABLE 1 — LOGIC FAMILY COMPARISONS

GENERAL CHARACTERISTICS (1)

(ALL MAXIMUM RATINGS)		TTL			CMOS		
Characteristic	**Symbol**	**LS**	**ALS**	**FAST**	**14000**	**Hi-Speed**	**Units**
Operating Voltage Range	$V_{CC/EE/DD}$	5±5%	5±5%	5±5%	3.0 to 18	2.0 to 6.0	V
Operating Temperature Range	T_A	0 to +70	0 to +70	0 to +70	−40 to +85	−40 to +85	°C
Input Voltage (limits)	$V_{IH\ (min)}$	2.0	2.0	2.0	3.5[4]	3.5[4]	V
	$V_{IL\ (max)}$	0.8	0.8	0.8	1.5[4]	1.0[4]	V
Output Voltage (limits)	$V_{OH\ (min)}$	2.7	2.7	2.7	$V_{DD}-0.05$	$V_{CC}-0.1$	V
	$V_{OL\ (max)}$	0.5	0.5	0.5	0.05	0.1	V
Input Current	I_{in} I_{INH}	20	20	20	±0.3	±1.0	μA
	I_{INL}	−400	−200	−600			
Output Current @ V_O (limit) unless otherwise specified	I_{OH}	−0.4	−0.4	−1.0	−2.1@2.5 V	−4.0 @ $V_{CC}-0.8$ V	mA
	I_{OL}	8.0	8.0	20	0.44@0.4 V	4.0@0.4 V	mA
DC Noise Margin Low/High	DCM	0.3/0.7	0.3/0.7	0.3/0.7	1.45[4]	0.90/1.35[4]	V
DC Fanout	–	20	20	33	>50(1)[2]	50(10)[2]	

SPEED/POWER CHARACTERISTICS (1)

(ALL TYPICAL RATINGS)		TTL			CMOS		
Characteristic	**Symbol**	**LS**	**ALS**	**FAST**	**14000**	**Hi-Speed**	**Units**
Quiescent Supply Current/Gate	I_G	0.4	0.2	1.1	0.0001	0.0005	mA
Power/Gate (Quiescent)	P_G	2.0	1.0	5.5	0.0006	0.001	mW
Propagation Delay	t_p	9.0	7.0	3.5	125	8.0	ns
Speed Power Product	–	18	7.0	19.2	0.075	0.01	pJ
Clock Frequency (D-F/F)	f_{max}	33	35	125	4.0	40	MHz
Clock Frequency (Counter)	f_{max}	40	45	125	5.0	40	MHz

PROPAGATION DELAY (1)

		TTL			CMOS		
		LS	**ALS**	**FAST**	**14000**	**HC**	**Units**
Gate, NOR or NAND:	Product No.	SN74LS00	SN74ALS00	74F00	MC14001B	74HC00	
t_{PLH}/t_{PHL}[5]	Typical	(10)[3]	(5)[3]	3.7	25	(8)[3]10	ns
	Maximum	(15)[3]	10	5.0	250	(15)[3]20	ns
Flip-Flop, D-type:	Product No.	SN74LS74	SN74ALS74	74F74	MC14013B	74HC74	
t_{PLH}/t_{PHL}[5] (Clock to Q)	Typical	(25)[3]	(12)[3]	6.2	175	(23)[2]25	ns
	Maximum	(40)[3]	20	8	350	(30)[3]32	ns
Counter:	Product No.	SN74LS163	SN74ALS163	74F163	MC14163B	74HC163	
t_{PLH}/t_{PHL}[5] (Clock to Q)	Typical	(18)[3]	(10)[3]	7	350	(20)[3]22	ns
	Maximum	(27)[3]	24	10	700	(27)[3]29	ns

NOTES: 1. Specifications are shown for the following conditions:
a) V_{DD}(CMOS) = 5.0 Vdc ± 10%(DC), 5.0 Vdc(AC); V_{CC}(TTL) = 5.0 Vdc ± 5%(DC), 5.0 Vdc(AC)
b) Basic Gates: LS00 or equivalent
c) $T_A = 25°C$
d) $C_L = 50$ pF(ALS, FAST, HC), 15 pF(LS, 14000 and Hi-Speed)
e) Commercial grade product
2. ( )fanout to LSTTL
3. ( )$C_L = 15$ pF
4. DC input voltage specifications are proportional to supply voltage over operating range.
5. The number specified is the larger of t_{PLH} and t_{PHL} for each device.

HANDLING PRECAUTIONS

High-Speed CMOS devices, like all MOS devices, have an insulated gate that is subject to voltage breakdown. The gate oxide for HSCMOS devices is about 800 Å thick and breaks down at a gate-source potential of about 100 V. The gates on the devices are protected by an improved resistor-diode network similar to the one used for metal-gate CMOS devices (Figure 2). The changes made to the protection network result in a two to three times improvement over the previous scheme, using the test setup as shown in Figure 3. The input protection network in HSCMOS uses a polysilicon resistor in series with the input and before the protection diodes, as opposed to the previous method where the diode to V_{CC} was tied directly to the input. This series resistor slows down the rise time of static discharge spikes to allow the protection diodes time to turn on.

Static damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged inputs are the easiest to detect in that the input has been completely destroyed and is either shorted to V_{CC}, shorted to ground, or open-circuited. The effect is that the device no longer responds to signals present at the damaged input. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performance. Another effect of static damage is that these inputs generally have increased leakage currents.

Although the enhanced gate-protection network does offer significant improvements over the metal-gate protection, these devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4-15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

1. Do not exceed the Maximum Ratings specified by the data sheet.

2. All unused device inputs should be connected to V_{CC} or GND.

3. All low impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the CMOS is powered up. Similarly, this type of equipment should be disconnected before power is turned off.

4. A circuit board containing CMOS devices is merely an extension of the device and the same handling precautions apply. Contacting edge connectors wired directly to CMOS device inputs can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address only an input of a CMOS integrated circuit, a resistor should be used in series with the input. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. This resistor will help limit accidental damage if the PC board is removed and brought into contact with static generating materials. For convenience, a graph of the typical added propagation delay is given in Figure 4, for a switch point of 0.5 V_{CC} and an input capacitance of 10 pF. Note that the maximum input rise and fall times should not be exceeded. For an input capacitance of 10 pF, a maximum series resistance of 30 kΩ can be used without violating input rise and fall times.

5. All CMOS devices should be stored or transported in materials that are antistatic. CMOS devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays, but should be left in their original container until ready for use.

6. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 5.

FIGURE 2 — INPUT PROTECTION NETWORKS

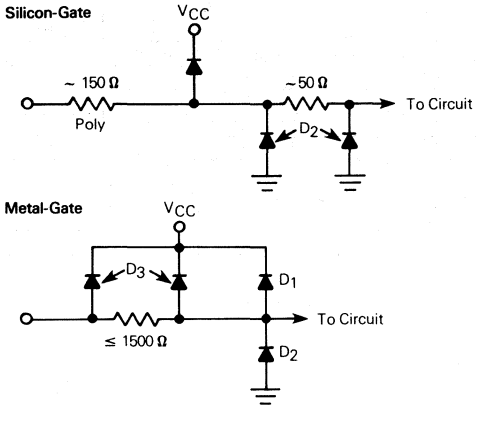


FIGURE 3 — ELECTROSTATIC DISCHARGE TEST CIRCUIT

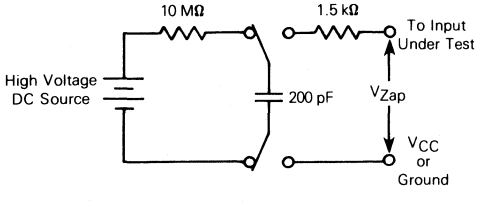
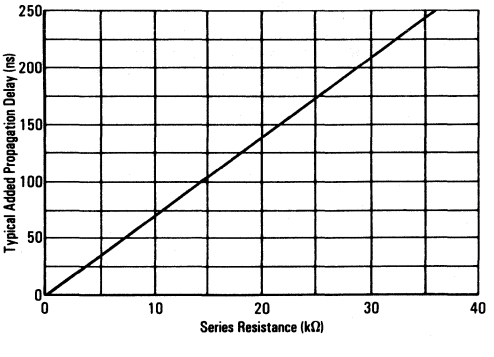


FIGURE 4 — SERIES RESISTANCE EFFECTS



7. Nylon or other static generating materials should not come in contact with CMOS circuits.

8. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices or boards. Reduce static build-up by use of one or more of the following: grounding suspect areas, using ionized air blowers, or utilizing room humidifiers.

9. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material.

10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.

11. The following steps should be observed during wave solder operations.
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.

12. The following steps should be observed during board cleaning operation.
    a. Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
    d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.

13. The use of static detection meters for line surveiliance is highly recommended.

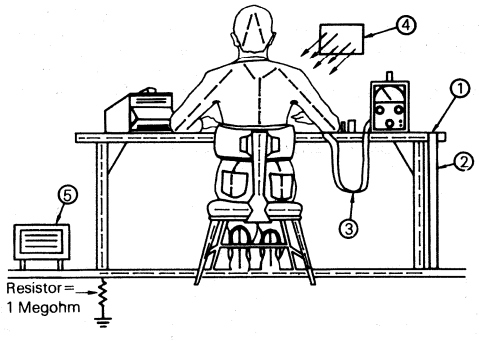
14. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.

15. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing CMOS devices to be certain there are no voltage transients present.

16. Double check test equipment setup for proper polarity of voltage before conducting parametric or functional testing.

4

FIGURE 5 — TYPICAL MANUFACTURING WORK STATION



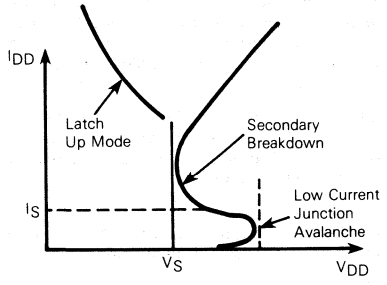
NOTES: 1. 1/16 inch conductive sheet stock covering bench top work area.
2. Ground Strap.
3. Wrist Strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room Humidifier. Primarily for use in areas where direct grounding is impractical.

POWER SUPPLIES

Two of the major reasons for choosing CMOS devices are the low power requirement and the ability to operate over a wide supply range. The power requirement for a totally CMOS system is low enough that applications normally requiring switching power supplies and cooling fans can be built with inexpensive conventional power supplies. Another feature of HSCMOS systems is that a battery backup may be used.

The maximum recommended power supply voltage for HSCMOS is limited to 6.0 Vdc. Figure 6 offers some insight as to how this specification was derived. In the figure, V_S is the maximum power supply voltage and I_S is the sustaining current for the latch-up mode. The value of V_S was chosen so that the secondary breakdown effect may be avoided. The low-current junction avalanche region is between 10 and 14 Vdc at $T_A = 25°C$.

FIGURE 6 — SECONDARY BREAKDOWN CHARACTERISTICS



Data Sheet Maximum Supply Rating

In an ideal system design, a power supply should be designed to deliver only enough current to insure proper operation of all devices. The obvious benefit of this type design is cost savings; an added benefit is protection against the possibility of latch-up related failures. This system protection can be provided by the power supply filter and/or voltage regulator.

HSCMOS devices are ideally suited to battery or battery backup systems. A few precautions should be taken when designing battery operated systems.

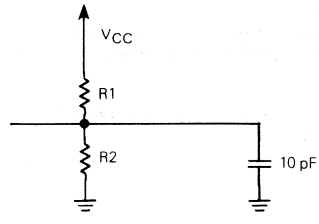
1. Recommended power supply voltages should be observed. For battery backup systems such as the one in Figure 7, $V_{Batt} \geq 2.0\ V + 0.7\ V$ to account for the voltage drop across the series diode.
2. Inputs that might go above the battery backup voltage should use either a series resistor to limit the input current or use the HC4050 or HC4049 high-to-low voltage translators.
3. Outputs that are subject to voltage levels above V_{CC} or below ground should be protected with a series resistor to limit the current to an acceptable level or clamping diodes.

INPUTS

A basic knowledge of HSCMOS inputs is essential for the CMOS designer. This section deals with input characteristics and rules regarding their use.

CMOS inputs, while in the recommended operating range ($GND \leq V_{in} \leq V_{CC}$), can be modeled as shown in Figure 8. For input voltages in this range, diodes D1 and D2 are modeled as resistors, representing the reverse bias impedance of the diodes. The maximum input current is worst case, 1 μA, when the inputs are at V_{CC} or ground, and $V_{CC} = 6$ Vdc.

FIGURE 8 — INPUT MODEL FOR $GND \leq V_{in} \leq V_{CC}$



It is possible, when inputs are left open-circuited, for the inputs to be biased at or near the typical CMOS switchpoint, 0.45 V_{CC}, where both the P-channel and N-channel transistors are conducting, causing excess current drain. Due to the high gain of the buffered devices (see Figure 9), the CMOS device can go into oscillation from any noise in the system, resulting in even higher current drain.

FIGURE 7 — BATTERY BACKUP SYSTEM

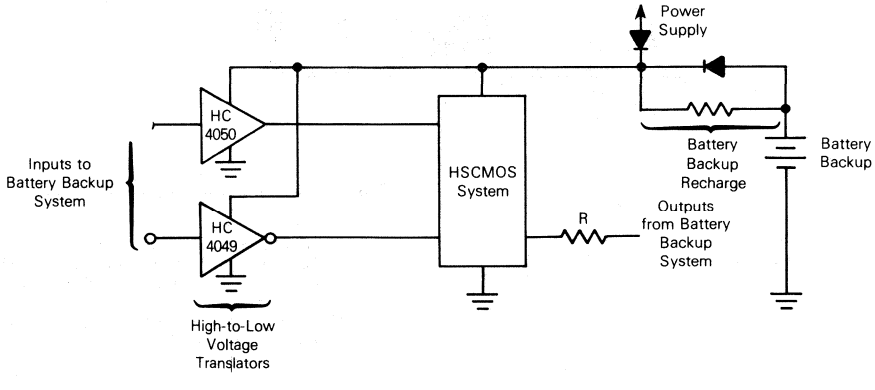
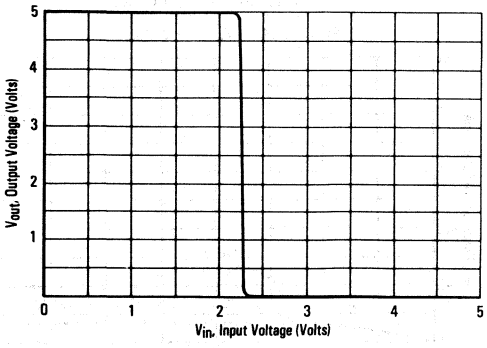
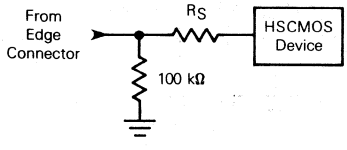


FIGURE 9 — TYPICAL TRANSFER CHARACTERISTICS FOR BUFFERED DEVICES



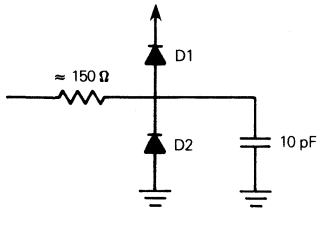
For these reasons, all unused CMOS inputs should be connected either to V_{CC} or ground. For applications with inputs going to edge connectors, a 100 kΩ resistor to ground should be used, as well as a series resistor for static protection and current limiting (see HANDLING for series resistor calculation). For best results, the resistors should be configured as in Figure 10.

FIGURE 10 — EXTERNAL PROTECTION



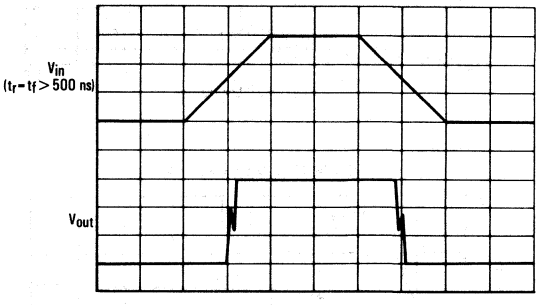
For inputs outside of the recommended operating range, the CMOS input is modeled as in Figure 11. The enhanced resistor-diode protection network allows the user greater freedom when designing a worst case system. The device inputs are guaranteed to withstand voltages from −1.5 V to V_{CC}+1.5 Vdc and a maximum current of 20 mA. At low capacitive loads, the output rise and fall times of HSCMOS devices can be as low as 3 ns producing some amount of overshoot and undershoot. With the above input ratings, most designs will require no special terminations or design considerations.

FIGURE 11 — INPUT MODEL FOR $V_{in} > V_{CC}$ AND $V_{in} < GND$



Another specification that should be noted is the maximum input rise and fall times. Figure 12 shows the results of exceeding the 500 ns maximum rise and fall times. The reason for the oscillation on the output is that as the voltage passes through the switching threshold region with a slow rise time, any noise that is on the input line is amplified, and is passed through to the output. This oscillation may have a low enough frequency to cause succeeding stages to switch, giving unexpected results. If input rise or fall times are expected to exceed 500 ns, Schmitt-trigger devices such as the HC14 and HC132 are recommended.

FIGURE 12 — MAXIMUM RISE TIME VIOLATION



OUTPUTS

All HSCMOS outputs, with the exception of the HCU04, are buffered to insure consistent output voltage and current specifications across the family. All buffered outputs have guaranteed output voltages of V_{OL} = 0.1 V and $V_{OH} = V_{CC} - 0.1$ V for I_{out} = 20 μA (20 HSCMOS loads). The output drives for standard drive devices are such that both 74HC and 54HC devices can drive ten LSTTL loads and maintain $V_{out} \leq 0.4$ V across the full temperature range; bus-driver devices can drive fifteen LSTTL loads under the same conditions.

The outputs of all HSCMOS devices are limited to externally forced output voltages of $-0.5 \leq V_{out} \leq V_{CC} + 0.5$ Vdc. For voltages outside this range, a silicon controlled rectifier (SCR) formed by parasitic transistors can be triggered, causing the device to latch up. For more information on this, see Latch Up.

The maximum rated output current given on the individual data sheets is 25 mA for standard outputs and 35 mA for bus drivers. The output short circuit currents of these devices will typically exceed these limits. The outputs can, however, be shorted for short periods of time for logic testing, if the maximum package power dissipation of 500 mW is not violated.

For applications that require driving high capacitive loads where fast propagation delays are needed (e.g., driving power MOSFETs), devices within the same package may be paralleled. Paralleling devices in different packages may result in devices switching at different points on the input voltage waveform, creating output short circuits and yielding undesirable output voltage waveforms.

As a design aid, output characteristic curves are given for both P-channel source and N-channel sink currents. The curves given include expected minimum curves for T_A = 25°, 85° and 125°C, as well as typical values for T_A = 25°C. These curves, Figures 13-24, are intended as design aids, not as guarantees.

STANDARD OUTPUT CHARACTERISTICS

N-CHANNEL SINK CURRENT

FIGURE 13 — V_{GS} = 2 Vdc

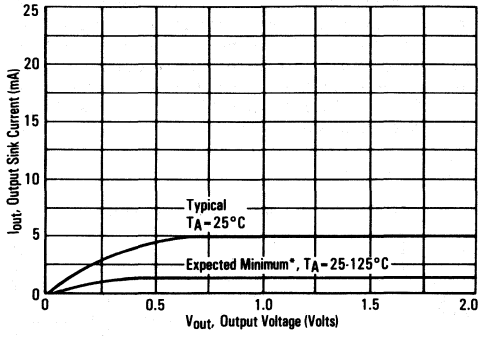


FIGURE 15 — V_{GS} = 4.5 Vdc

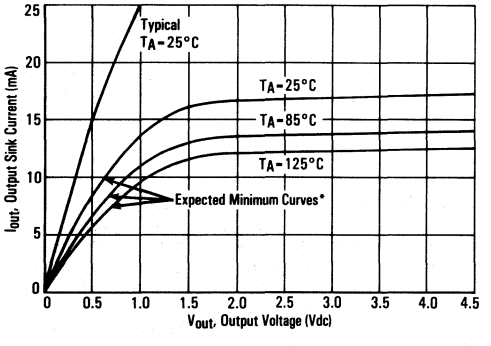
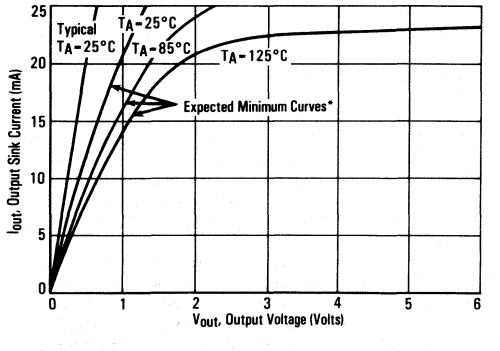


FIGURE 17 — V_{GS} = 6.0 Vdc



P-CHANNEL SOURCE CURRENT

FIGURE 14 — V_{GS} = −2 Vdc

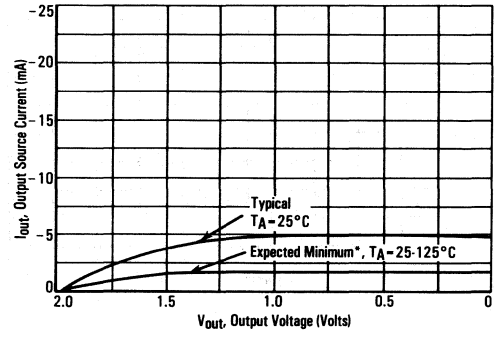


FIGURE 16 — V_{GS} = −4.5 Vdc

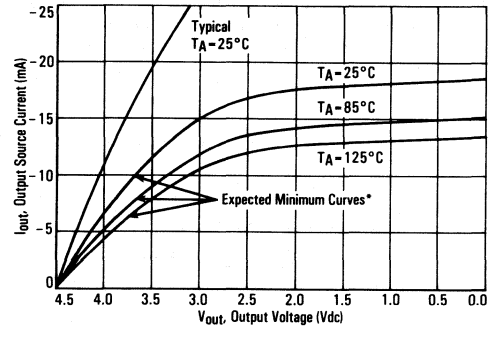
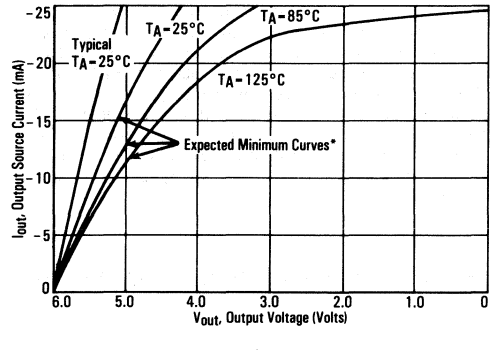


FIGURE 18 — V_{GS} = −6.0 Vdc

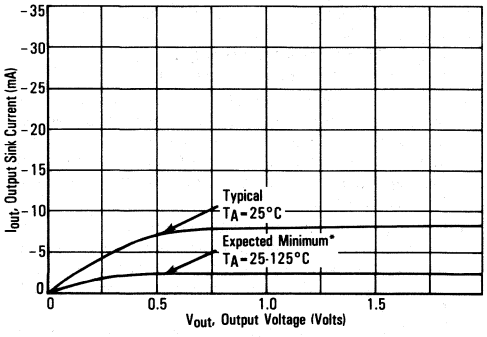


*The expected minimum curves are not guarantees, but are design aids.

BUS-DRIVER OUTPUT CHARACTERISTICS

N-CHANNEL SINK CURRENT

FIGURE 19 — $V_{GS} = 2.0$ Vdc



P-CHANNEL SOURCE CURRENT

FIGURE 20 — $V_{GS} = -2.0$ Vdc

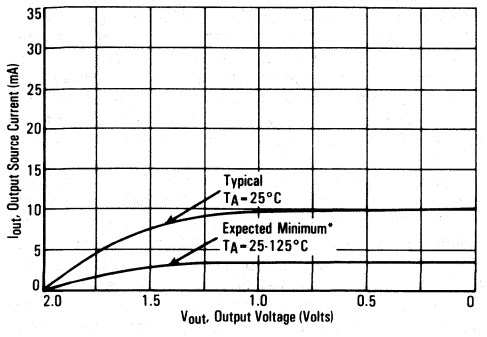


FIGURE 21 — $V_{GS} = 4.5$ Vdc

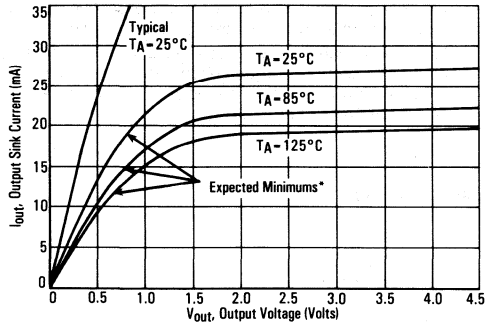


FIGURE 22 — $V_{GS} = -4.5$ Vdc

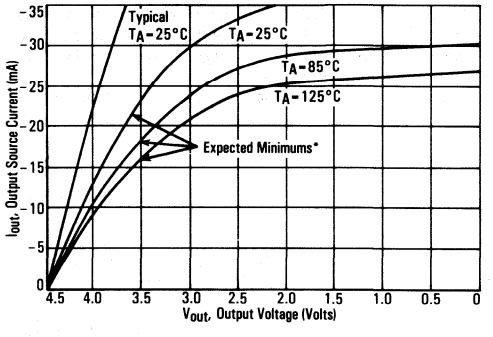


FIGURE 23 — $V_{GS} = 6.0$ Vdc

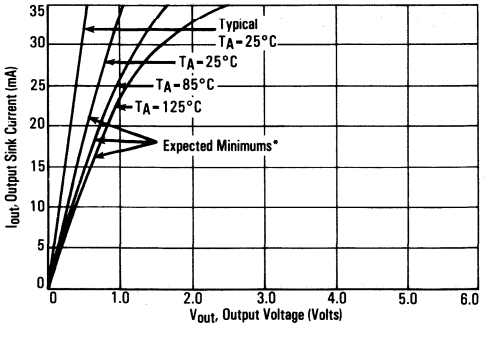
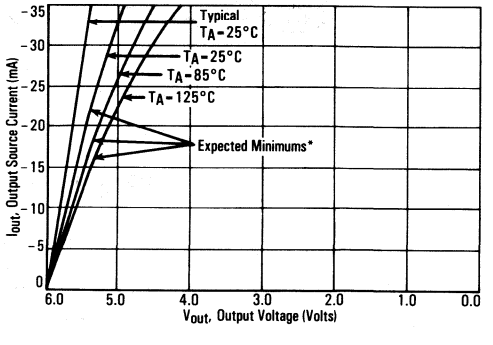


FIGURE 24 — $V_{GS} = -6.0$ Vdc



*The expected minimum curves are not guarantees, but are design aids.

4

LATCH UP

Latch-up immunity in HSCMOS devices has been greatly improved over the standard metal-gate CMOS family. Typically, these devices will not latch up with currents of 75 mA forced into or out of the inputs or 150 mA for the outputs under worst case conditions ($T_A = 125°C$ and $V_{CC} = 6$ Vdc). At room temperatures, the parts can typically withstand currents forced into or out of the outputs of over 300 mA. As for the inputs, the input protection network will typically fail before latch-up currents are reached ($|I_{in}| > 90$ mA). For most designs, latch up will not be a problem, but the designer should be aware of it, what causes it and how to prevent it.

Figure 25 shows the layout of a typical CMOS inverter and Figure 26 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the devices on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than $V_{CC} + 0.5$ Vdc or less than -0.5 Vdc and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, it will, if the supply current is not limited, destroy the device. Ways to prevent such occurrences are listed below.

1. Insure that inputs and outputs are limited to the maximum rated values.
   $-1.5 \le V_{in} \le V_{CC} + 1.5$ Vdc referenced to GND
   $-0.5 \le V_{out} \le V_{CC} + 0.5$ Vdc referenced to GND
   $|I_{in}| \le 20$ mA
   $|I_{out}| \le 25$ mA for standard outputs
   $|I_{out}| \le 35$ mA for bus-driver outputs
2. If voltage transients of sufficient energy to latch up the device are expected on the outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the Maximum Ratings values.
3. If voltage transients are expected on the inputs, protection diodes may be used to clamp the voltage or a series resistor may be used to limit the current to a level less than the maximum rating of $I_{in} = 20$ mA (see Figure 4 for resistor values).
4. Sequence power supplies so that the inputs or outputs of HSCMOS devices are not powered up first (e.g., recessed edge connectors may be used in plug-in board applications and/or series resistors).
5. Power supply lines should be free of excessive noise. Care in board layout and filtering should be used.
6. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power-supply filtering network or with a current-limiting regulator.

FIGURE 25 — CMOS WAFER CROSS SECTION

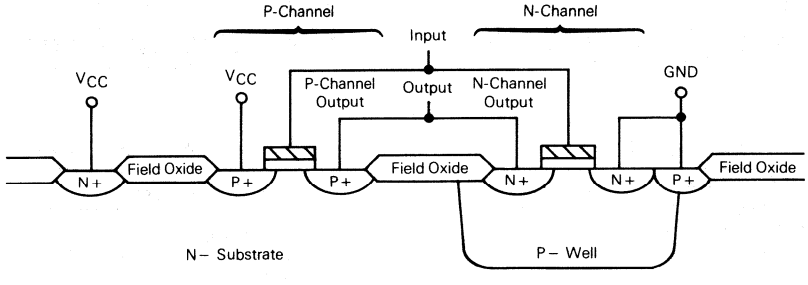
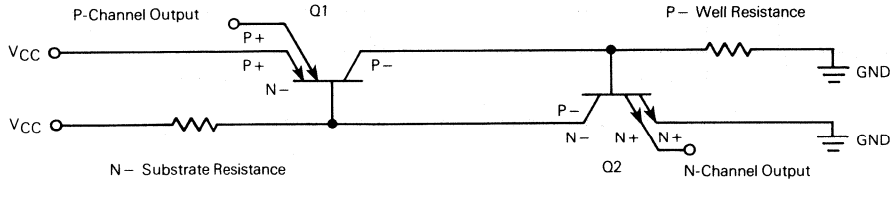


FIGURE 26 — LATCH UP CIRCUIT SCHEMATIC



POWER DISSIPATION

Power consumption for HSCMOS is dependent on the power-supply voltage, frequency of operation, internal capacitance, and load. The power consumption may be calculated for each package by summing the quiescent power consumption, $I_{CC}V_{CC}$, and the switching power required by each device within the package. The device dynamic power requirements can be calculated by the equation:

$$P_D = (C_L + C_{PD})V_{CC}^2 f$$

In this equation, f is the frequency in hertz, C_L is the total load capacitance present at the output under test, and C_{PD}, power dissipation capacitance, is a measure of internal capacitances given specifically for power consumption calculations. C_{PD} is calculated in the following manner:

1. The power-supply voltage is set to $V_{CC} = 6$ Vdc.
2. Signal inputs are set up so that as many outputs as possible are switching, giving a worst case situation.
3. The power supply current is measured and recorded at input frequencies of 200 kHz and 1 MHz.
4. The power dissipation capacitance is calculated by solving the two simultaneous equations:

$$P_{D1} = C_{PD}V_{CC}^2 f_1 + I_{CC}V_{CC}$$

and

$$P_{D2} = C_{PD}V_{CC}^2 f_2 + I_{CC}V_{CC}$$

giving

$$C_{PD} = \frac{P_{D1} - P_{D2}}{V_{CC}^2(f_1 - f_2)}$$

or

$$C_{PD} = \frac{I_{D1} - I_{D2}}{V_{CC}(f_1 - f_2)}$$

where I_{D1} = supply current at $f_1 = 200$ kHz
I_{D2} = supply current at $f_2 = 1$ MHz

On HSCMOS data sheets, C_{PD} is a typical value and is given either for the package or for the individual device (i.e., gates, flip-flops, etc.) within the package. An example of calculating the package power requirement is given using the 74HC00, as shown in Figure 27.

From the data sheet:

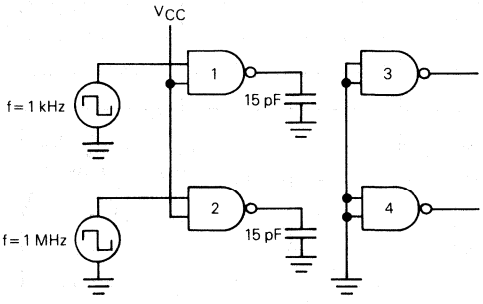
$I_{CC} = 0.001\ \mu$A typical at room temperature
$C_{PD} = 20$ pF per gate

$$P_D = (C_{PD} + C_L)V_{CC}^2 f + V_{CC}I_{CC}$$

$P_{D1} = (20\text{ pF} + 15\text{ pF})(5\text{ V})^2(1\text{ kHz}) = 0.875\ \mu$W
$P_{D2} = (20\text{ pF} + 15\text{ pF})(5\text{ V})^2(1\text{ MHz}) = 875\ \mu$W
$P_{D3} = (20\text{ pF})(5\text{ V})^2(0\text{ Hz}) = 0\ \mu$W
$P_{D4} = (20\text{ pF})(5\text{ V})^2(0\text{ Hz}) = 0\ \mu$W

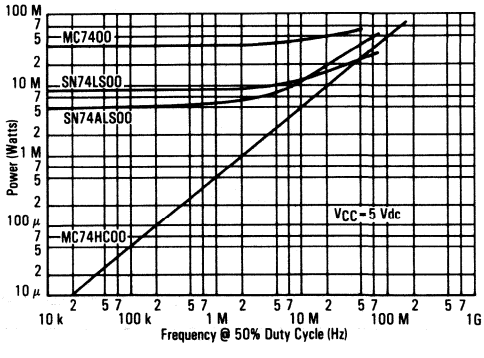
$$P_D(\text{total}) = V_{CC}I_{CC} + P_{D1} + P_{D2} + P_{D3} + P_{D4}$$
$$= 0.005\ \mu\text{W} + 0.875\ \mu\text{W} + 875\ \mu\text{W} + 0\ \mu\text{W}$$
$$= 876\ \mu\text{W}$$

FIGURE 27 — POWER CONSUMPTION CALCULATION EXAMPLE



As seen by this example, the power dissipated by CMOS devices is dependent on frequency. When operating at very high frequencies, HSCMOS devices can consume as much power as LSTTL devices, as shown in Figure 28. The power savings of HSCMOS is realized when used in a system, where only a few of the devices will actually be switching at the system frequency. The power consumption savings comes from the fact that for CMOS, only the devices that are switching consume significant power.

FIGURE 28 — 2-INPUT NAND GATE POWER CONSUMPTION VERSUS DEVICE FREQUENCY (NO LOAD) HIGH-SPEED CMOS VERSUS TTL, LSTTL, AND ALS (TYPICAL VALUES)



The maximum rated package power dissipation for HSCMOS packages is 500 mW for both ceramic and plastic packages. The plastic packages derate at − 12 mW/°C from 65°C and − 12 mW/°C from 85°C for ceramic packages. This is illustrated in Figure 29.

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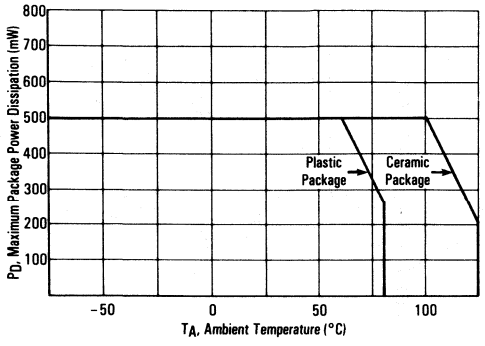
FIGURE 29 — MAXIMUM PACKAGE POWER DISSIPATION VERSUS TEMPERATURE



CAPACITIVE LOADING EFFECTS

In addition to temperature and power-supply effects, capacitive loading effects should be taken into account. The additional propagation delay may be calculated if the short circuit current for the device is known. Expected minimum numbers may be determined from Table 2 and knowing that the propagation delay is measured to the 50% point of the output waveform (typically 0.5 V_{CC}).

From the equation

$$i = \frac{C dv_C}{dt}$$

we can use the approximation

$$I = \frac{C\triangle V}{\triangle t}$$

so $$\triangle t = \frac{C\triangle V}{I}$$

or $$\triangle t = \frac{C(0.5\ V_{CC})}{I}$$

This equation gives the general form of the additional propagation delay. To calculate the propagation delay of a device for a particular load capacitance, C_L, the following equation may be used.

$$t_{PT} = t_P(C_{LDS}) + 0.5\ V_{CC}(C_L - C_{LDS})/I_{OS}$$

where

t_{PT} = total propagation delay
$t_P(C_{LDS})$ = specified propagation delay with load C_{LDS}
C_{LDS} = Data Sheet load capacitance
C_L = actual load capacitance
I_{OS} = short circuit current (Table 2)

An example is given here for t_{PHL} of the 74HC00 driving a 150 pF load.

$$V_{CC} = 4.5\ V$$

$$t_{PHL}(50\ pF) = 18\ ns$$

$$C_L = 150\ pF$$

$$I_{OS} = 17.3\ mA$$

$$t_{PHL}(150\ pF) = 18\ ns + \frac{(0.5)(4.5\ V)(150\ pF - 50\ pF)}{17.3\ mA}$$

$$= 18\ ns + 13\ ns$$

$$= 31\ ns$$

Another example for $C_L = 0$ pF and all other parameters the same.

$$t_{PLH}(0\ pF) = 18\ ns + \frac{(0.5)(4.5\ V)(0\ pF - 50\ pF)}{17.3\ mA}$$

$$= 18\ ns + (-6.5\ ns)$$

$$t_{PLH} = 11.5\ ns$$

This method gives the expected propagation delay, and is intended as a design aid, and not as a guarantee.

TABLE 2 — EXPECTED MINIMUM SHORT CIRCUIT CURRENTS*

Parameter	V_{CC}	Standard Drivers 25°C	Standard Drivers 85°C	Standard Drivers 125°C	Bus Drivers 25°C	Bus Drivers 85°C	Bus Drivers 125°C	Units
Output Short Circuit Source Current	2.0	1.89	1.83	1.80	3.75	3.64	3.60	mA
	4.5	18.5	15.0	13.4	37.0	30.0	26.6	
	6.0	35.2	28.0	24.6	70.6	56.1	49.2	
Output Short Circuit Sink Current	2.0	1.55	1.55	1.55	2.45	2.45	2.43	mA
	4.5	17.3	14.0	12.5	27.2	22.1	19.6	
	6.0	33.4	26.5	23.2	52.6	41.7	36.5	

* These values are intended as design aids, not as guarantees.

TEMPERATURE EFFECTS

The information in this section should give the designer a better feel for how HSCMOS devices operate over the operating temperature range. The graphs in this section are intended to be design aids, not guarantees.

One of the inherent advantages of CMOS devices is that the N-channel and P-channel transistors track each other over a wide temperature range. For this reason, CMOS parameters such as output current, propagation delays, and transition times vary in a predictable way. Figure 30 shows the temperature relationships for these parameters, as well as for channel resistance. To show the effects of temperature on noise margin, Figure 31 shows the typical transfer characteristics for devices with buffered inputs and outputs. Note that the typical switch point is at 45% of the supply voltage and is minimally affected by temperature.

FIGURE 30 — NORMALIZED PLOT OF TYPICAL SINK-CURRENT (I_{OL}), SOURCE-CURRENT (I_{OH}), CHANNEL RESISTANCE (R_C), PROPAGATION DELAY TIMES (t_{PHL}, t_{PLH}), AND RISE AND FALL TIMES (t_r, t_f) versus AMBIENT TEMPERATURE (T_A)

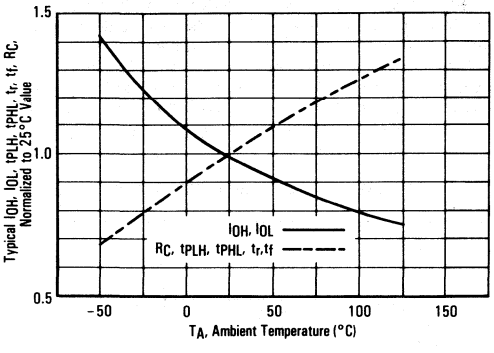
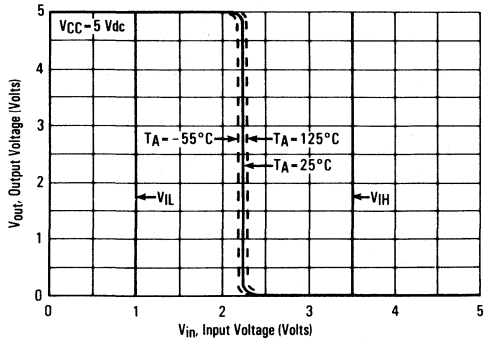


FIGURE 31 — TEMPERATURE EFFECTS ON TRANSFER CHARACTERISTICS



VOLTAGE EFFECTS

The transconductive gain, I_{out}/V_{in}, of MOS transistors, is proportional to the gate voltage minus the threshold voltage, $V_G - V_T$. The gate voltage at the input of the final stage of buffered device is approximately the power supply voltage, V_{CC} or GND. Since $V_G = V_{CC}$ or GND, the output drive current is proportional to the supply voltage. Propagation delays for CMOS devices are also affected by the power supply voltage, because most of the delay is due to charging and discharging internal capacitances. Figures 32 and 33 show the typical variation of current drive and propagation delay, normalized to $V_{CC} = 4.5$ Vdc for $2.0 \leq V_{CC} \leq 6.0$ Vdc. These curves may be used with the tables on each data sheet to arrive at parametric values not shown specifically in that particular table.

FIGURE 32 — NORMALIZED CURRENT DRIVE versus V_{CC}

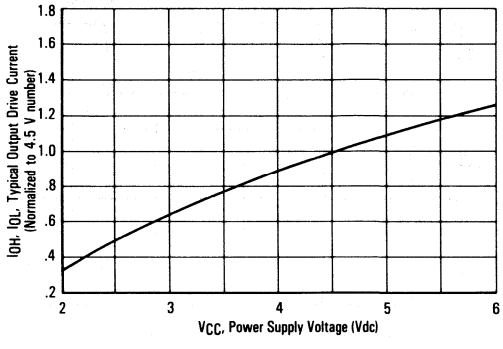
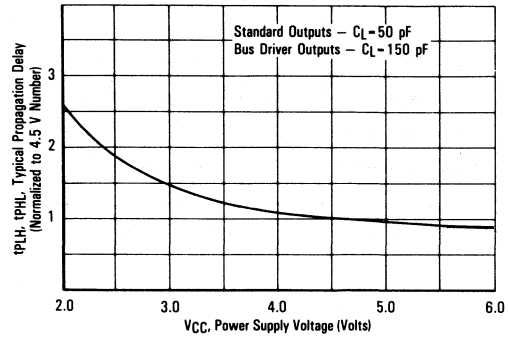


FIGURE 33 — NORMALIZED PROPAGATION DELAY versus V_{CC}



4

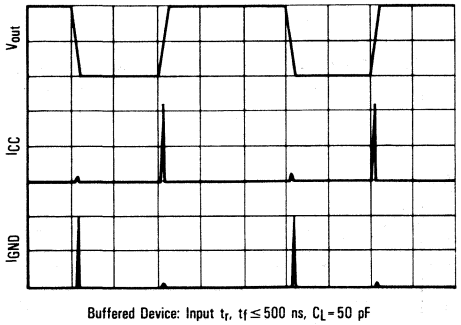
DECOUPLING CAPACITORS

The switching waveforms shown in Figures 34 and 35 show the current spikes introduced to the power supply and ground lines. This effect is shown for a load capacitance of less than 5 pF and for 50 pF. For ideal power supply lines with no series impedance, the spikes would pose no problem. However, actual power supply and ground lines do possess series impedance, giving rise to noise problems. For this reason, care should be taken in board layouts, insuring low impedance paths to and from logic devices. In addition to good layout practices, decoupling capacitors should be used to absorb the switching spikes. As a general guideline, each gate should be decoupled with at least 0.01 μF and at least 0.1 μF per 20 gates, distributed as evenly as possible over the circuit board.

FIGURE 34 — SWITCHING CURRENTS FOR $C_L < 5$ pF

Buffered Device: Input t_r, $t_f \leq 500$ ns, $C_L < 5$ pF

FIGURE 35 — SWITCHING CURRENTS FOR $C_L = 50$ pF



Buffered Device: Input t_r, $t_f \leq 500$ ns, $C_L = 50$ pF

INTERFACING

HSCMOS devices have a wide operating voltage range ($V_{CC} = 2-6$ Vdc) and sufficient current drive to interface with most other logic families available today. In this section, various interface schemes are given to aid the designer (Figures 36-41), as well as explanations of the High-Speed CMOS designators. The various types of CMOS devices with their input/output levels and comments are given in Table 3, to aid the designer in choosing the right device for interfacing applications.

Device Designators are as follows:

HC — This is a high-speed CMOS device with CMOS input switching levels and buffered CMOS outputs. The numbering of devices with this designator follows the LSTTL numbering sequence and are functional and pinout equivalents of those devices (e.g., HC00, HC688, etc.). Exceptions to this are devices that are functional and pinout equivalent to metal-gate CMOS devices (e.g., HC4002, HC4538, etc.).

HCU — This is an unbuffered high-speed CMOS device, with only one stage between the input and output. Since this is an unbuffered device, input and output levels may differ from buffered devices. At present, the family contains only one unbuffered device, the HCU04.

HCT — This is a high-speed CMOS device with an LSTTL-to-CMOS input buffer stage. These devices are designed to interface with LSTTL outputs operating at $V_{CC} = 5$ V $\pm 10\%$, but are functional over the entire HSCMOS voltage range of $2.0 \leq V_{CC} \leq 6.0$ Vdc. These devices have fully buffered CMOS outputs that will drive HSCMOS or LSTTL devices with no additional interfacing circuitry.

FIGURE 36 — HC TO LSTTL INTERFACING

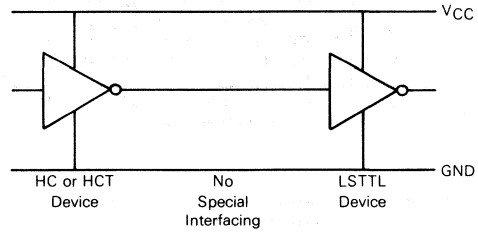


FIGURE 37 — LSTTL TO HCT INTERFACING

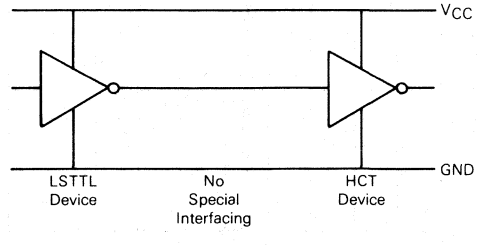


FIGURE 38 — LSTTL TO HC INTERFACING

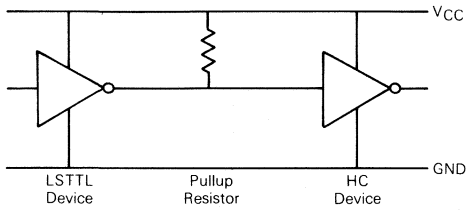
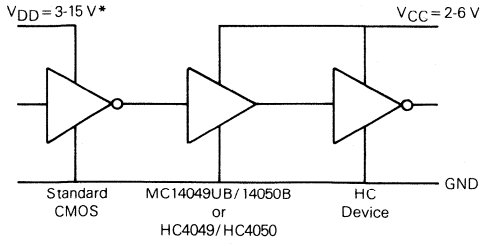


FIGURE 40 — HIGH VOLTAGE CMOS TO HSCMOS



*V_{OH} must be greater than V_{IH} of low voltage Device; V_{DD} = 3-18 V may be used if interfacing to 14049UB/14050B.

FIGURE 39 — LSTTL TO LOW-VOLTAGE HSCMOS

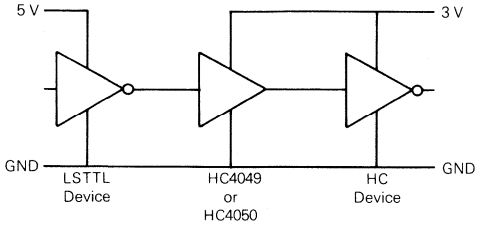


FIGURE 41 — UP/DOWN LEVEL SHIFTING USING THE MC14504B

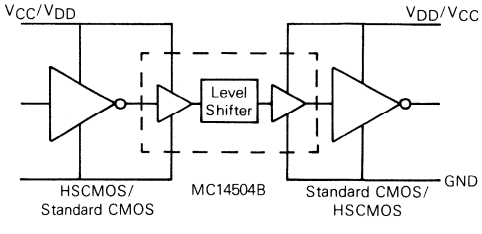


TABLE 3 — INTERFACING GUIDE

Device	Input Level	Output Level	Comments
HCXXX	CMOS	CMOS	LSTTL functional and pinout equivalent devices.
HC4XXX	CMOS	CMOS	CMOS functional and pinout equivalent devices.
HCUXX	CMOS	CMOS	Used in linear applications.
HCTXXX	TTL	CMOS	HSCMOS device with TTL-to-CMOS input buffering.
HC4049, HC4050	$-0.5 \le V_{in} \le 15$ Vdc	CMOS	High-to-low level translators, CMOS switching levels.
MC14049 MC14050	$-0.5 \le V_{in} \le 18$ Vdc	CMOS	Metal-gate CMOS high-to-low level translators, CMOS switching levels.
MC14504	CMOS or TTL	CMOS	Metal-gate CMOS high-to-low or low-to-high level translator.

Data Sheets

5

MOTOROLA

MC54/74HC00

Advance Information

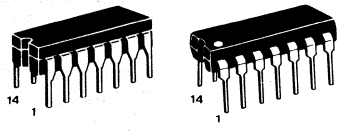
HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD 2-INPUT NAND GATE

QUAD 2-INPUT NAND GATE

The MC54/74HC00 is identical in pinout to the LS00. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632

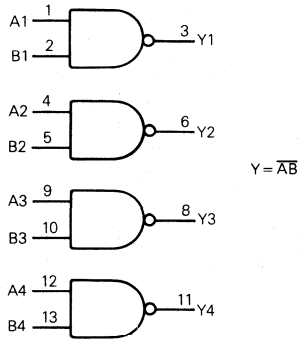
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

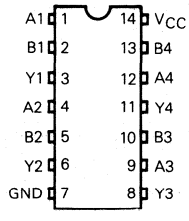
LOGIC DIAGRAM



$Y = \overline{AB}$

V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



5

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output Y	8	15	ns
t_{PHL}	(Figures 1 and 2)	8	15	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	45	90	113	134	ns
		4.5	9	18	23	27	
		6.0	8	15	19	23	
t_{PHL}		2.0	45	90	113	134	ns
		4.5	9	18	23	27	
		6.0	8	15	19	23	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	20	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption per gate:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS

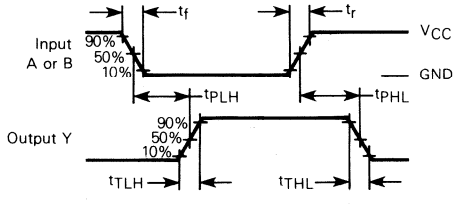
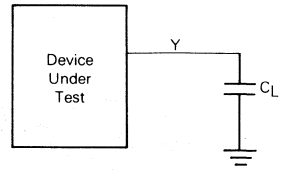


FIGURE 2 — TEST CIRCUIT



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MOTOROLA

MC54/74HCT00

Product Preview

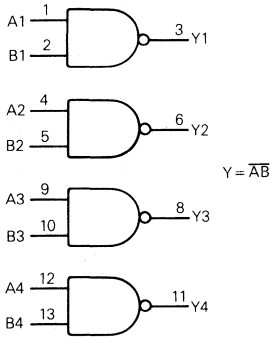
QUAD 2-INPUT NAND GATE (WITH LSTTL-COMPATIBLE INPUTS)

The MC54/74HCT00 may be used as a level converter for interfacing LSTTL to High-Speed CMOS. The inputs of HCT devices are compatible with both LSTTL and CMOS output voltage levels. Therefore, no pullup resistors are required at the inputs of the HCT00 when interfacing with LSTTL.

The HCT00 is identical in pinout to the LS00.

- Compatible with LSTTL Outputs — No Pullup Resistor Required
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Voltage Range: 4.5 to 5.5 Volts
- Low Quiescent Current Characteristic of CMOS Devices
- Diode Protection on All Inputs

LOGIC DIAGRAM

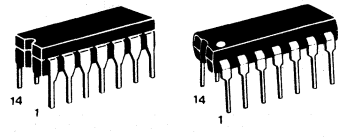


$Y = \overline{AB}$

V_{CC} = Pin 14
GND = Pin 7

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD 2-INPUT NAND GATE (WITH LSTTL-COMPATIBLE INPUTS)



J SUFFIX
CERAMIC PACKAGE
CASE 632

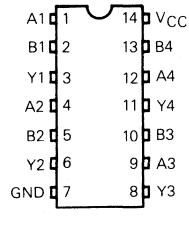
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCTXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCTXXN (Plastic Package)
MC74HCTXXJ (Ceramic Package)

PIN ASSIGNMENT



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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

MC54/74HC02

Advance Information

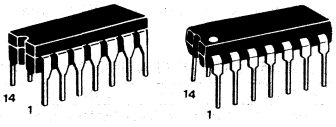
HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD 2-INPUT
NOR GATE

QUAD 2-INPUT NOR GATE

The MC54/74HC02 is identical in pinout to the LS02. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632

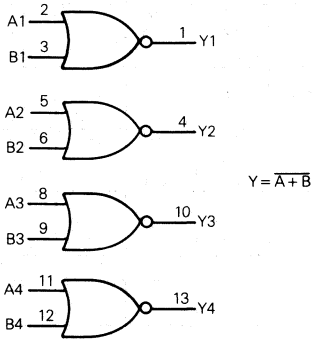
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

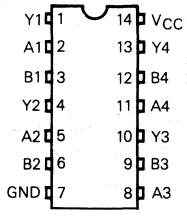
LOGIC DIAGRAM



$Y = \overline{A + B}$

V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\|$ = 20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\|$ = 20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{out} = −20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} I_{out} = −4.0 mA I_{out} = −5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{out} = 20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{out} = 4.0 mA I_{out} = 5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	—	2	20	40	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output Y	8	15	ns
t_{PHL}	(Figures 1 and 2)	8	15	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	45	90	113	134	ns
		4.5	9	18	23	27	
		6.0	8	15	19	23	
t_{PHL}		2.0	45	90	113	134	ns
		4.5	9	18	23	27	
		6.0	8	15	19	23	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	20	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption per gate:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS

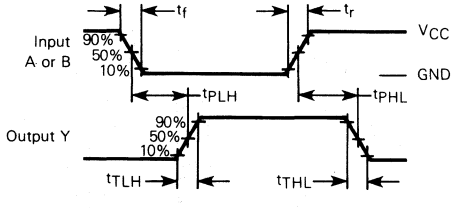
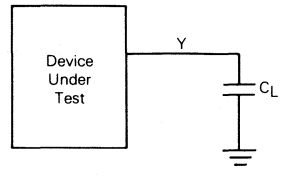


FIGURE 2 — TEST CIRCUIT



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MOTOROLA

MC54/74HC03

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

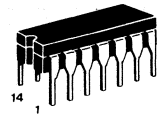
QUAD 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUTS

QUAD 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUTS

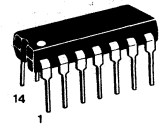
The MC54/74HC03 is identical in pinout to the LS03. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC03 NAND gate has, as its output, a high-performance MOS N-Channel transistor. This NAND gate can, therefore, with a suitable pullup resistor, be used in wired-AND applications. Having the output characteristic curves given in this data sheet, this device can be used as an LED driver or in any other application that only requires a sinking current.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum — With Suitable Pullup Resistor
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632



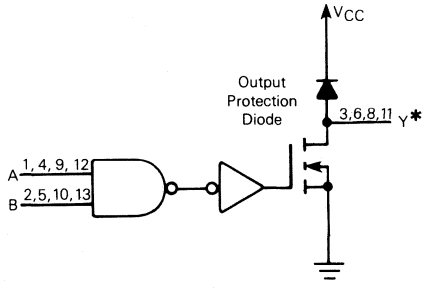
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

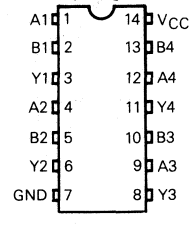
FUNCTION DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

* Denotes open-drain outputs.

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z = High Impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C 54HC and 74HC		85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed			Unit
V_{IH}	Minimum High-Level Input Voltage (Figure 2 for $V_{out}=V_{CC}-0.1$ V)	$V_{out}=0.1$ V or $V_{CC}-0.1$ V $\|I_{out}\|=20$ μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage (Figure 2 for $V_{out}=V_{CC}-0.1$ V)	$V_{out}=0.1$ V or $V_{CC}-0.1$ V $\|I_{out}\|=20$ μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in}=V_{IH}$ or V_{IL} $I_{out}=20$ μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in}=V_{IH}$ or V_{IL} $I_{out}=4.0$ mA $I_{out}=5.2$ mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in}=V_{CC}$ or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	$V_{in}=V_{CC}$ or GND $I_{out}=0$ μA	6.0	—	2	20	40	μA
I_{OZ}	Maximum Output Leakage Current	A or B = V_{IL} $V_{out}=V_{CC}$ or GND	6.0	—	±0.5	±5.0	±10.0	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLZ}	Maximum Propagation Delay, A or B to Output Y (Figures 1 and 2)	C_L = 5 pF	7	20	ns
t_{PZL}		C_L = 15 pF	10	20	ns
t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	C_L = 15 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{PLZ}	Maximum Propagation Delay, A or B to Output Y (Figures 1 and 2)	C_L = 50 pF	2.0	63	125	158	186	ns
			4.5	13	25	32	37	
			6.0	11	21	27	32	
t_{PZL}			2.0	63	125	158	186	ns
			4.5	13	25	32	37	
			6.0	11	21	27	32	
t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	C_L = 50 pF	2.0	38	75	95	110	ns
			4.5	8	15	19	22	
			6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		–	5	10	10	10	pF
C_{out}	Maximum Output Capacitance (A or B = GND)		–	6	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		–		–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: P_D (per gate) = $C_{PD}\ V_{CC}^2 f + I_{CC}\ V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS

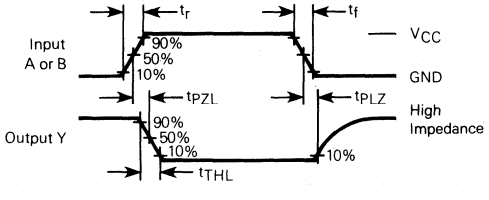


FIGURE 2 — TEST CIRCUIT

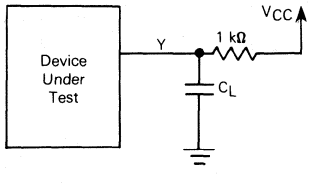
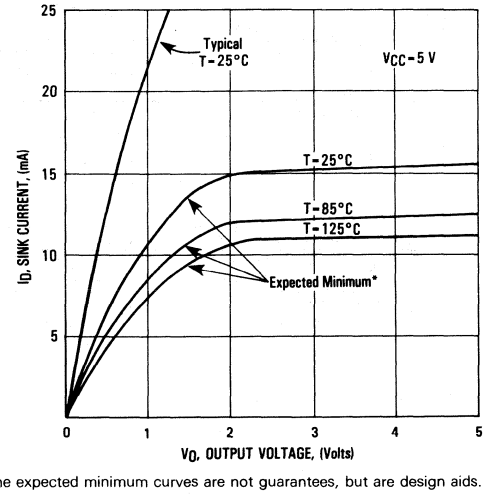


FIGURE 3 — OPEN-DRAIN OUTPUT CHARACTERISTICS

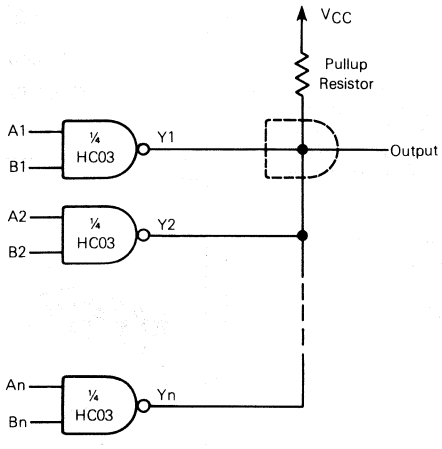


* The expected minimum curves are not guarantees, but are design aids.

5

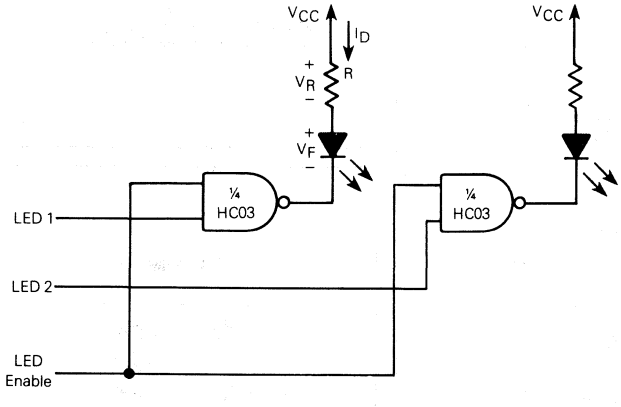
TYPICAL APPLICATIONS

Wired AND



$$\text{Output} = Y1 \bullet Y2 \bullet \ldots \bullet Yn$$
$$= A1 \bullet B1 + A2 \bullet B2 + \ldots + An \bullet Bn$$

LED Driver with Blanking



Design Example

Conditions: $I_D \cong 10$ mA

Using Figure 3 typical curve, @ $I_D = 10$ mA, $V_{DS} \cong 0.4$ V

$$\therefore R = \frac{V_{CC} - V_F - V_O}{I_D}$$
$$= \frac{5\text{ V} - 1.7\text{ V} - 0.4\text{ V}}{10\text{ mA}}$$
$$= 290\ \Omega$$

Use R = 270 Ω

5

MOTOROLA

MC54/74HC04

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

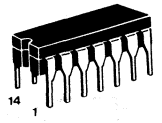
HEX INVERTER

HEX INVERTER

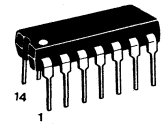
The MC54/74HC04 is identical in pinout to the LS04 and the MC14069. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six three-stage inverters. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and GND.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632



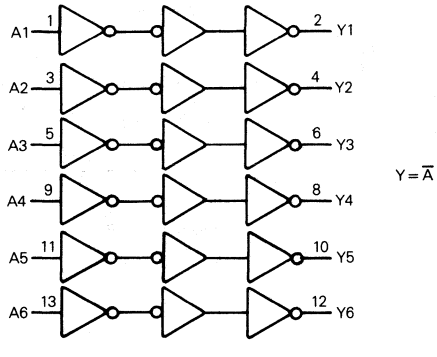
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

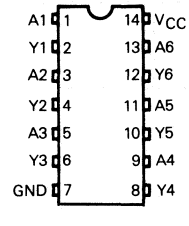
LOGIC DIAGRAM



$Y = \overline{A}$

V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C 54HC and 74HC		85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed			Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A to Output Y	10	17	ns
t_{PHL}	(Figures 1 and 2)	10	17	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0	55	86	108	129	ns
		4.5	11	19	24	29	
		6.0	9	16	20	24	
t_{PHL}		2.0	55	86	108	129	ns
		4.5	11	19	24	29	
		6.0	9	16	20	24	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	20	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

SWITCHING WAVEFORM AND TEST CIRCUIT

FIGURE 1

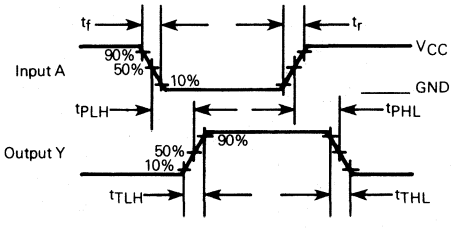
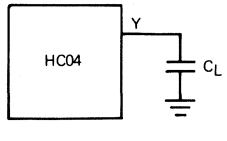


FIGURE 2 — TEST CIRCUIT



MOTOROLA

MC54/74HCT04

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

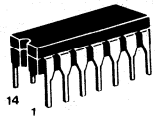
HEX INVERTER
(WITH LSTTL-COMPATIBLE
INPUTS)

HEX INVERTER
(WITH LSTTL-COMPATIBLE INPUTS)

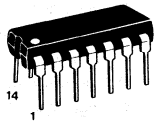
The MC54/74HCT04 may be used as a level converter for interfacing LSTTL to High-Speed CMOS. The inputs of HCT devices are compatible with both LSTTL and CMOS output voltage levels. Therefore, no pullup resistors are required at the inputs of the HCT04 when interfacing with LSTTL.

The HCT04 is identical in pinout to the LS04.

- Compatible with LSTTL Outputs — No Pullup Resistor Required
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Voltage Range: 4.5 to 5.5 Volts
- Low Quiescent Current Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632



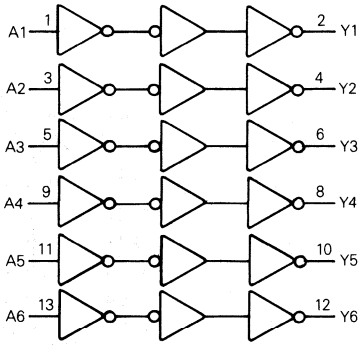
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCTXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCTXXN (Plastic Package)
MC74HCTXXJ (Ceramic Package)

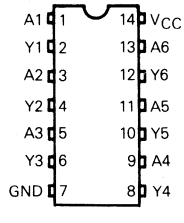
LOGIC DIAGRAM



$Y = \overline{A}$

V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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MOTOROLA

MC54/74HCU04

Advance Information

HEX UNBUFFERED INVERTER

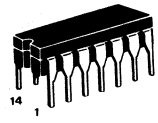
The MC54/74HCU04 is identical in pinout to the LS04 and the MC14069UB. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six single-stage inverters. These inverters are well suited for use as oscillators, pulse shapers and in many other applications requiring a high-input impedance amplifier.

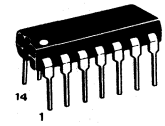
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HCU Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

HEX UNBUFFERED INVERTER



J SUFFIX
CERAMIC PACKAGE
CASE 632



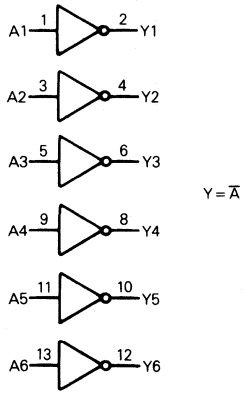
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCUXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCUXXN (Plastic Package)
MC74HCUXXJ (Ceramic Package)

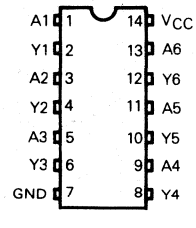
LOGIC DIAGRAM



$Y = \overline{A}$

V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HCU Series 54HCU Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	No Limit	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.5 V or V_{CC}−0.5 V* $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.3 2.5 3.3	1.7 3.6 4.8	1.7 3.6 4.8	1.7 3.6 4.8	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.5 V or V_{CC}−0.5 V* $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.5 1.6 2.2	0.3 0.8 1.1	0.3 0.8 1.1	0.3 0.8 1.1	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0		1.8 4.0 5.5	1.8 4.0 5.5	1.8 4.0 5.5	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.86 5.36	3.76 5.26	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0		0.2 0.5 0.5	0.2 0.5 0.5	0.2 0.5 0.5	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.20 0.20	0.32 0.32	0.37 0.37	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

* For V_{CC}=2.0 V, V_{out}=0.2 V or V_{CC}−0.2 V

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A to Output Y	7	13	ns
t_{PHL}	(Figures 1 and 2)	7	13	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0	50	82	103	120	ns
		4.5	10	16	21	24	
		6.0	8	14	18	20	
t_{PHL}		2.0	50	82	103	120	ns
		4.5	10	16	21	24	
		6.0	8	14	18	20	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	8	15	15	15	pF
C_{PD}	Power Dissipation Capacitance*	–	90	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption (per inverter):
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS

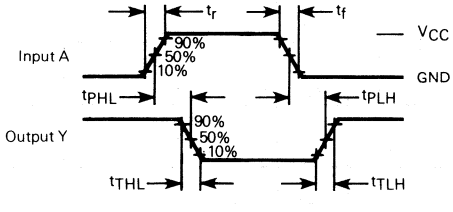
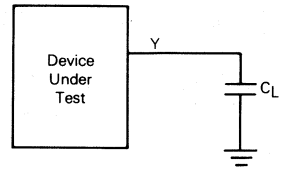


FIGURE 2 — TEST CIRCUIT



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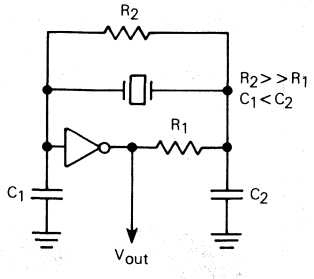
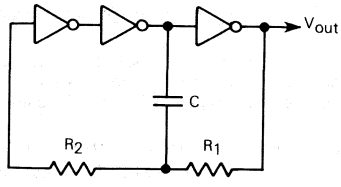
TYPICAL APPLICATIONS

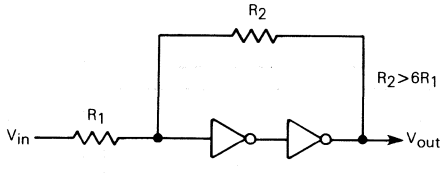
Crystal Oscillator



Stable RC Oscillator



Schmitt Trigger



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MOTOROLA

MC54/74HC08

Advance Information

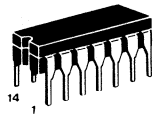
HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD 2-INPUT AND GATE

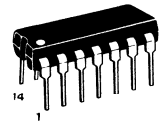
QUAD 2-INPUT AND GATE

The MC54/74HC08 is identical in pinout to the LS08. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632



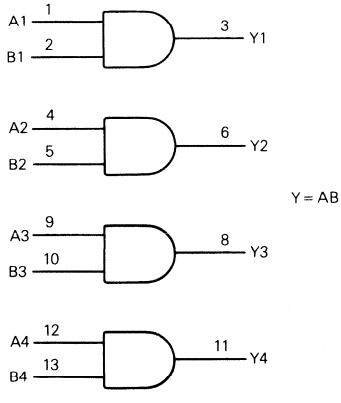
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

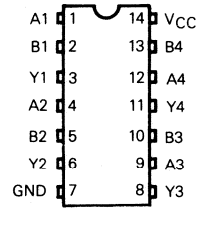
74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C 54HC and 74HC		85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed			Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output Y	7	15	ns
t_{PHL}	(Figures 1 and 2)	12	20	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	60	121	151	175	ns
		4.5	12	24	30	35	
		6.0	10	20	25	30	
t_{PHL}		2.0	60	121	151	175	ns
		4.5	12	24	30	35	
		6.0	10	20	25	30	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	38	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption per gate:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS

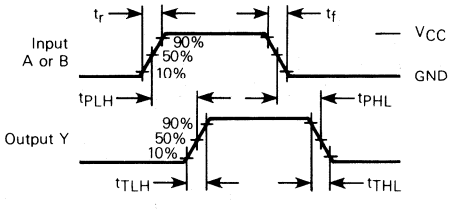
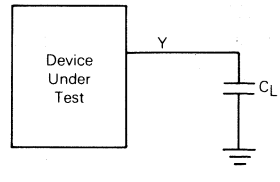


FIGURE 2 — TEST CIRCUIT



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MOTOROLA

MC54/74HC10

Advance Information

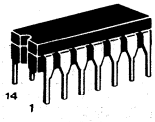
HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

TRIPLE 3-INPUT NAND GATE

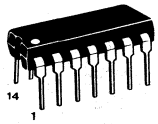
TRIPLE 3-INPUT NAND GATE

The MC54/74HC10 is identical in pinout to the LS10. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632



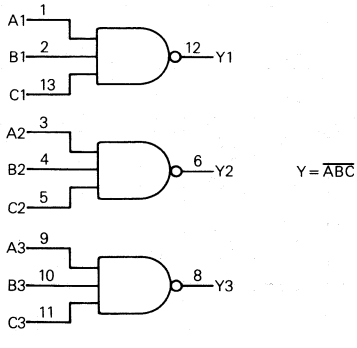
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

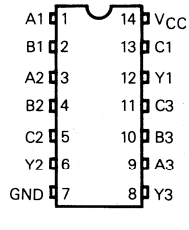
LOGIC DIAGRAM



$Y = \overline{ABC}$

V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C 54HC and 74HC		85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed			Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A, B, or C to Output Y	10	15	ns
t_{PHL}	(Figures 1 and 2)	10	15	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 1 and 2)	2.0	48	95	120	142	ns
		4.5	10	19	24	28	
		6.0	8	16	20	24	
t_{PHL}		2.0	48	95	120	142	ns
		4.5	10	19	24	28	
		6.0	8	16	20	24	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–		–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption per gate:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS

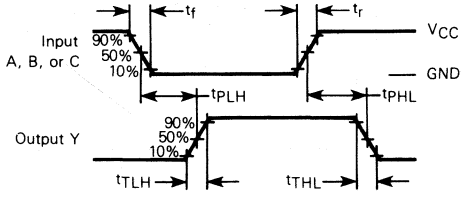
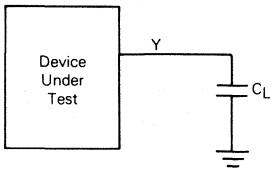


FIGURE 2 — TEST CIRCUIT



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MOTOROLA

MC54/74HC11

Advance Information

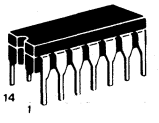
HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

TRIPLE 3-INPUT AND GATE

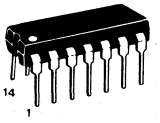
TRIPLE 3-INPUT AND GATE

The MC54/74HC11 is identical in pinout to the LS11. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632



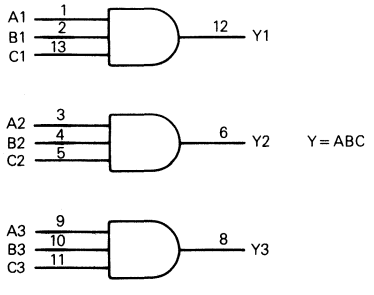
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

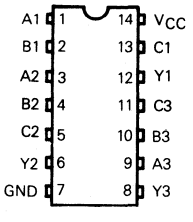
74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

FUNCTION DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A, B, or C to Output Y	12	20	ns
t_{PHL}	(Figures 1 and 2)	12	20	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 1 and 2)	2.0	48	125	156	190	ns
		4.5	16	25	31	38	
		6.0	13	21	27	31	
t_{PHL}		2.0	48	125	156	190	ns
		4.5	16	25	31	38	
		6.0	13	21	27	31	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	—	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	—	35	—	—	—	pF

* C_{PD} is used to determine the no-load dynamic power consumption per gate:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

SWITCHING WAVEFORM AND TEST CIRCUIT

FIGURE 1

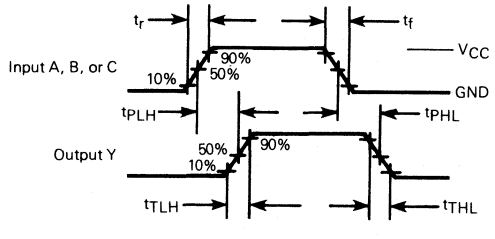
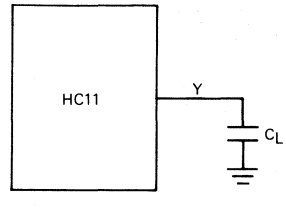
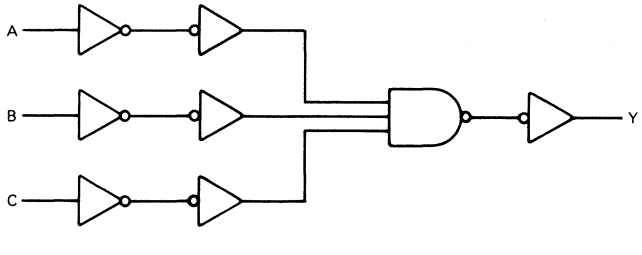


FIGURE 2 — TEST CIRCUIT



LOGIC DIAGRAM
(⅙ of the device)



MOTOROLA

MC54/74HC14

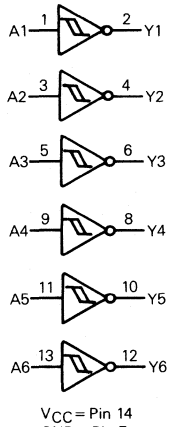
Advance Information

HEX SCHMITT-TRIGGER INVERTER

The MC54/74HC14 is identical in pinout to the LS14. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

FUNCTION DIAGRAM

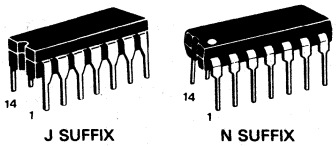


$Y = \overline{A}$

V_{CC} = Pin 14
GND = Pin 7

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

HEX SCHMITT-TRIGGER INVERTER



J SUFFIX
CERAMIC PACKAGE
CASE 632

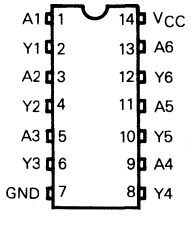
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

PIN ASSIGNMENT



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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	No Limit	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{T+} (Max)	Maximum Positive-Going Threshold Voltage (Figure 3)	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{T-} (Min)	Minimum Negative-Going Threshold Voltage (Figure 3)	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_H (Max)*	Maximum Hysteresis Voltage (Figure 3)	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.5 0.9 1.0	1.2 2.25 3.0	1.2 2.25 3.0	1.2 2.25 3.0	V
V_H (Min)	Minimum Hysteresis Voltage (Figure 3)	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.5 0.9 1.0	0.2 0.4 0.6	0.2 0.4 0.6	0.2 0.4 0.6	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{T+} (Max) or V_{T-} (Min) I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{T+} (Max) or V_{T-} (Min) I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{T+} (Max) or V_{T-} (Min) I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{T+} (Max) or V_{T-} (Min) I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

*$V_H = V_{T+} - V_{T-}$ [But V_H (Max) is specified as less than V_{T+} Max − V_{T-} Min]

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A to Output Y	12	22	ns
t_{PHL}	(Figures 1 and 2)	12	22	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0	60	125	156	188	ns
		4.5	13	25	31	38	
		6.0	11	21	26	32	
t_{PHL}		2.0	60	125	156	188	ns
		4.5	13	25	31	38	
		6.0	11	21	26	32	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	27	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption per inverter:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORM

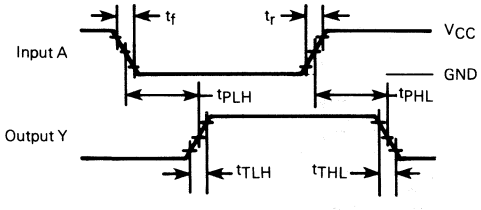

FIGURE 2 — TEST CIRCUIT

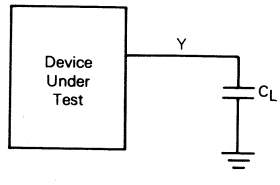

FIGURE 3 — TYPICAL INPUT THRESHOLD, V_{T+}, V_{T-}, VERSUS POWER SUPPLY VOLTAGE

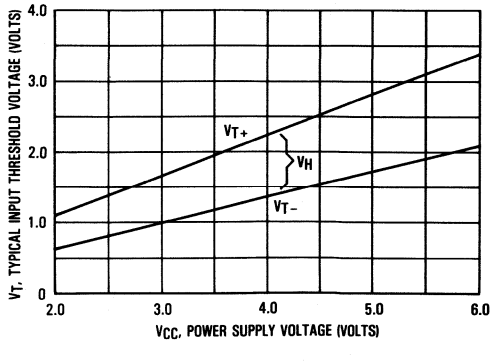

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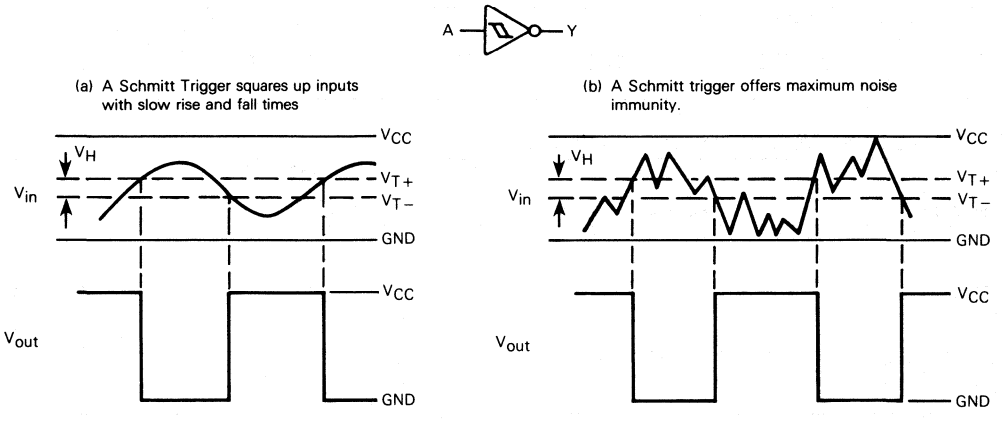
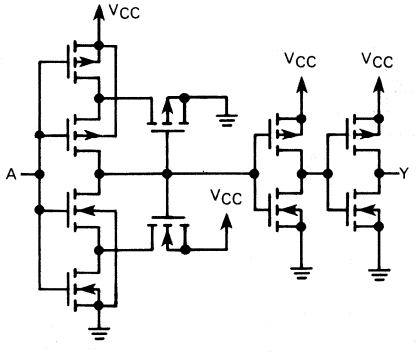
FIGURE 4 — TYPICAL SCHMITT-TRIGGER APPLICATIONS



SCHEMATIC DIAGRAM



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MOTOROLA

MC54/74HC20

Advance Information

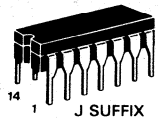
DUAL 4-INPUT NAND GATE

The MC54/74HC20 is identical in pinout to the LS20. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

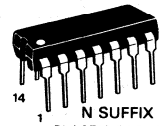
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL 4-INPUT NAND GATE



J SUFFIX
CERAMIC PACKAGE
CASE 632



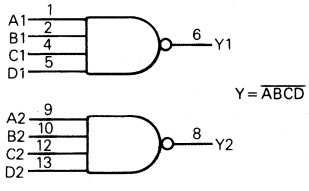
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

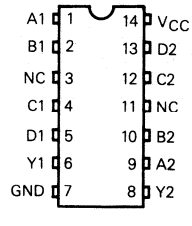
LOGIC DIAGRAM



$Y = \overline{ABCD}$

V_{CC} = Pin 14
GND = Pin 7
NC = Pins 3, 11

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

5

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC		Unit
		Typical	Guaranteed Limit	
t_{PLH}	Maximum Propagation Delay, Input A, B, C, or D to Output Y	8	15	ns
t_{PHL}	(Figures 1 and 2)	8	15	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
			Typical	Guaranteed Limit		
t_{PLH}	Maximum Propagation Delay, Input A, B, C, or D to Output Y (Figures 1 and 2)	2.0	45	90	113	134	ns
		4.5	9	18	23	27	
		6.0	8	15	19	23	
t_{PHL}		2.0	45	90	113	134	ns
		4.5	9	18	23	27	
		6.0	8	15	19	23	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	20	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption per gate:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS

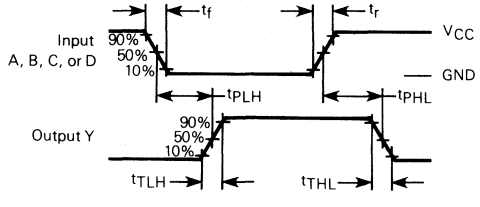
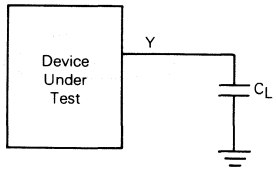


FIGURE 2 — TEST CIRCUIT



5

MOTOROLA

MC54/74HC27

Advance Information

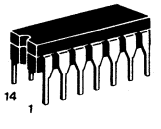
HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

TRIPLE 3-INPUT NOR GATE

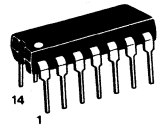
TRIPLE 3-INPUT NOR GATE

The MC54/74HC27 is identical in pinout to the LS27. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632



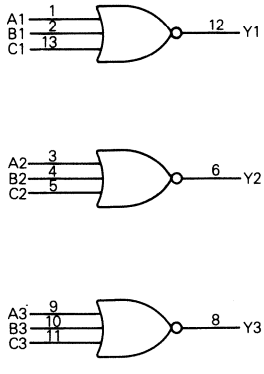
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

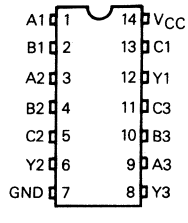
LOGIC DIAGRAM



$Y = \overline{A + B + C}$

V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A, B, or C to Output Y	8	15	ns
t_{PHL}	(Figures 1 and 2)	8	15	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 1 and 2)	2.0	45	90	113	134	ns
		4.5	9	18	23	27	
		6.0	8	15	19	23	
t_{PHL}		2.0	45	90	113	134	ns
		4.5	9	18	23	27	
		6.0	8	15	19	23	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	36	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption per gate:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS

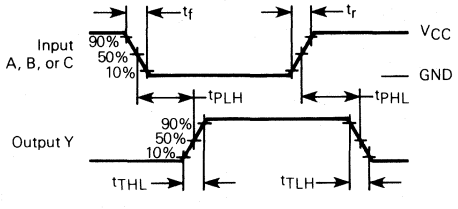
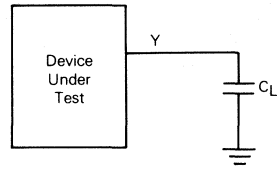
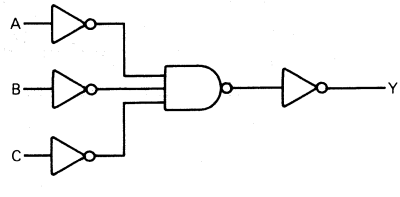


FIGURE 2 — TEST CIRCUIT



LOGIC DETAIL
(1/3 of the device)



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MOTOROLA

MC54/74HC30

Product Preview

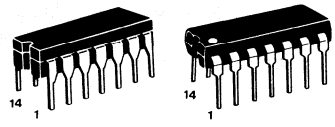
8-INPUT NAND GATE

The MC54/74HC30 is identical in pinout to the LS30. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

8-INPUT NAND GATE



J SUFFIX
CERAMIC PACKAGE
CASE 632

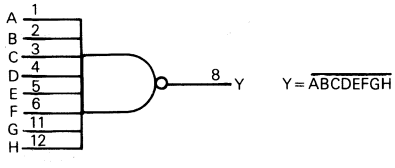
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

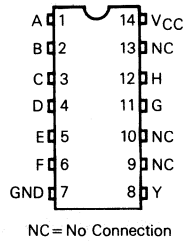
LOGIC DIAGRAM



Pins 9, 10, 13 = no connection

V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



NC = No Connection

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

5

MOTOROLA

MC54/74HC32

Product Preview

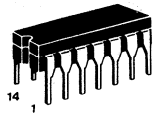
HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD 2-INPUT OR GATE

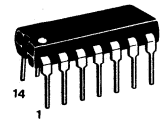
QUAD 2-INPUT OR GATE

The MC54/74HC32 is identical in pinout to the LS32. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632



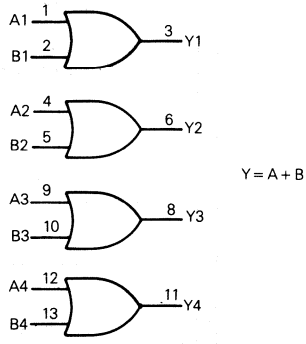
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

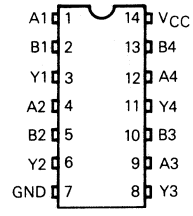
LOGIC DIAGRAM



$Y = A + B$

V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



Advance Information Data Sheet Available
Contact Your Motorola Representative

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

5

MOTOROLA

MC54/74HC42

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

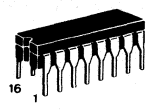
1-OF-10 DECODER

1-OF-10 DECODER

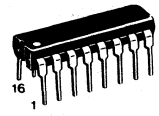
The MC54/74HC42 is identical in pinout to the LS42. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC42 decodes a BCD Address to one-of-ten active-low outputs. For Address inputs with a hexadecimal equivalent greater than 9, all outputs, Y0-Y9, will remain high.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620



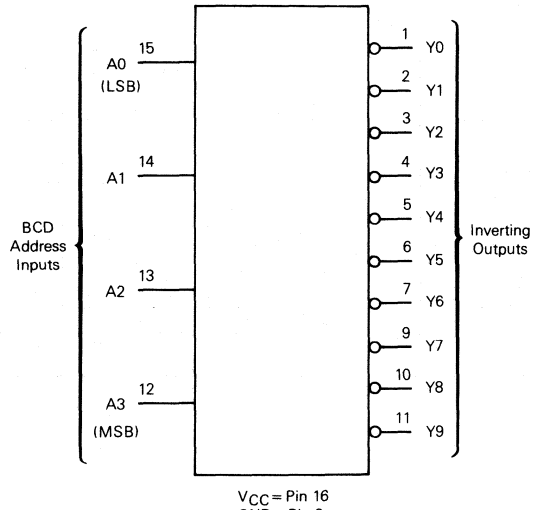
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

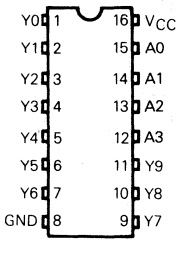
74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A to Output Y		25	ns
t_{PHL}	(Figures 1 and 2)		25	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{PHL}		2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–		–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS

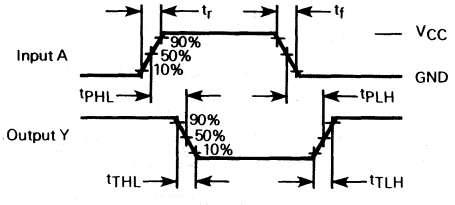
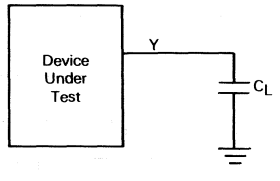


FIGURE 2 — TEST CIRCUIT



TRUTH TABLE

Inputs A3	A2	A1	A0	Outputs Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

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PIN DESCRIPTIONS

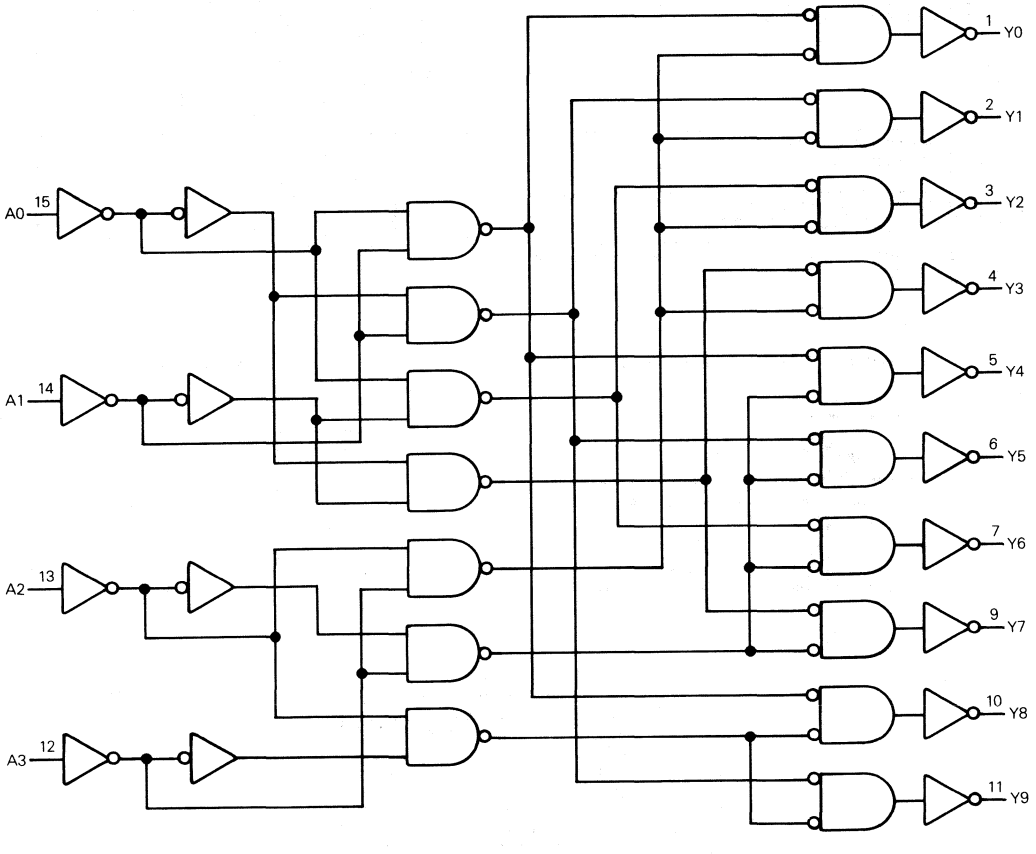
INPUTS

A0, A1, A2, A3, (PINS 15, 14, 13, 12) — BCD **Address** Inputs. The BCD address present at these inputs determines which output is active-low. These inputs are arranged such that A3 is the most-significant bit and A0 is the least-significant bit. Addresses with a hexadecimal equivalent number greater than nine are not decoded.

OUTPUTS

Y0-Y9 (PINS 1-7, 9-11) — Active-Low Decoded Outputs. These outputs assume a low level when addressed and remain high when not addressed.

LOGIC DIAGRAM



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MOTOROLA

MC54/74HC51

Advance Information

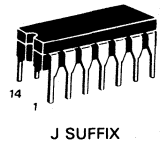
HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

2-WIDE, 2-INPUT/2-WIDE, 3-INPUT AND-OR-INVERT GATES

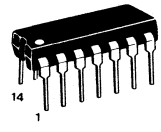
2-WIDE, 2-INPUT/2-WIDE, 3-INPUT AND-OR-INVERT GATES

The MC54/74HC51 is identical in pinout to the LS51. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632



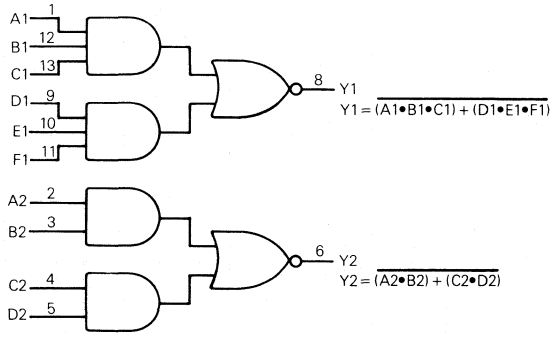
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

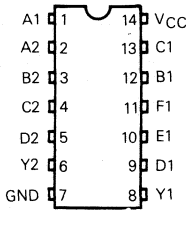
74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Any Input to Output Y	9	20	ns
t_{PHL}	(Figures 1 and 2)	9	20	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{PHL}		2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–		–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS

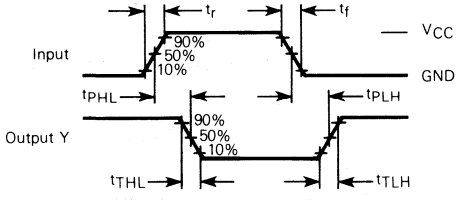
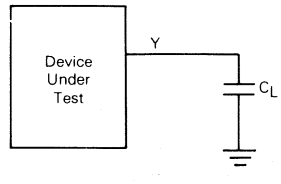


FIGURE 2 — TEST CIRCUIT



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MOTOROLA

MC54/74HC58

Advance Information

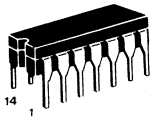
HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

2-WIDE, 2-INPUT/2-WIDE, 3-INPUT AND-OR GATES

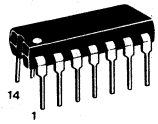
2-WIDE, 2-INPUT/2-WIDE, 3-INPUT AND-OR GATES

The MC54/74HC58 is identical to the MC54/74HC51 except that the outputs are inverted. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632



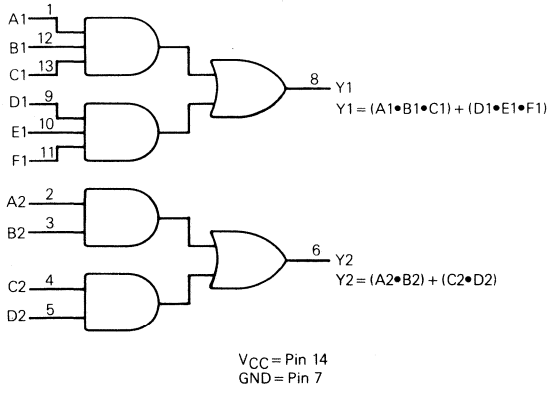
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

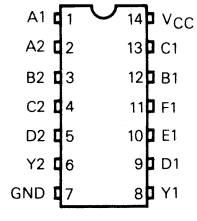
74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	–	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	–	2	20	40	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC		Unit
		Typical	Guaranteed Limit	
t_{PLH}	Maximum Propagation Delay, Any Input to Output Y	9	20	ns
t_{PHL}	(Figures 1 and 2)	10	20	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
			Typical	Guaranteed Limit		
t_{PLH}	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{PHL}		2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–		–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS

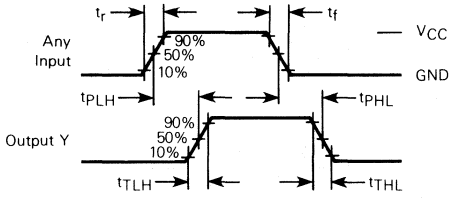
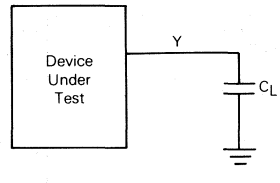


FIGURE 2 — TEST CIRCUIT



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MOTOROLA

MC54/74HC73

Advance Information

DUAL J-K FLIP-FLOP WITH RESET

The MC54/74HC73 is identical in pinout to the LS73. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

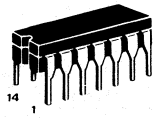
Each flip-flop is negative-edge clocked and has an active-low asynchronous reset.

The MC54/74HC73 is identical in function to the HC107, but has a different pinout.

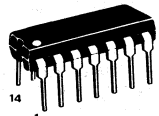
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 40 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL J-K FLIP-FLOP WITH RESET



J SUFFIX
CERAMIC PACKAGE
CASE 632



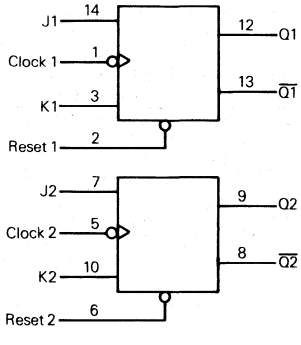
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

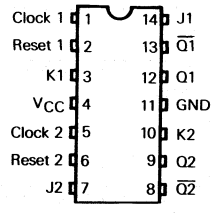
74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 4
GND = Pin 11

PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs	
Reset	Clock	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	No Change	
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	H	H	Toggle	
H	L	X	X	No Change	
H	H	X	X	No Change	
H	↑	X	X	No Change	

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	4	40	80	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	50	30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$	16	21	ns
t_{PHL}	(Figures 1 and 4)	16	21	
t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$	21	26	ns
t_{PHL}	(Figures 2 and 4)	21	26	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	11	5	4	3	MHz
		4.5	54	27	21	18	
		6.0	64	31	24	20	
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	2.0	63	126	160	185	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{PHL}		2.0	63	126	160	185	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$ (Figures 2 and 4)	2.0	78	155	194	250	ns
		4.5	16	31	39	47	
		6.0	13	26	32	40	
t_{PHL}		2.0	78	155	194	250	ns
		4.5	16	31	39	47	
		6.0	13	26	32	40	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (per Flip-Flop)		80	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	50	100	125	150	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	−20	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−3	0	0	0	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	50	100	125	150	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

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SWITCHING WAVEFORMS

FIGURE 1

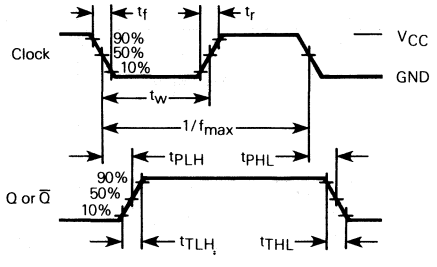


FIGURE 2

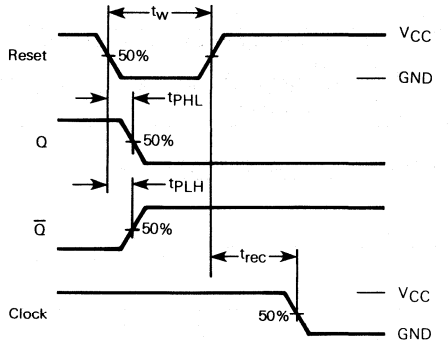


FIGURE 3

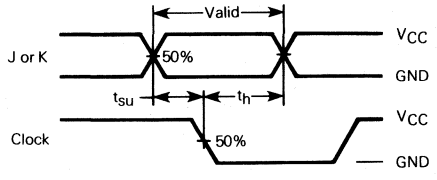
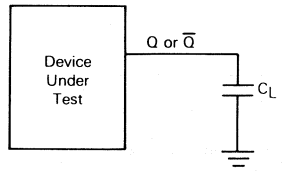


FIGURE 4



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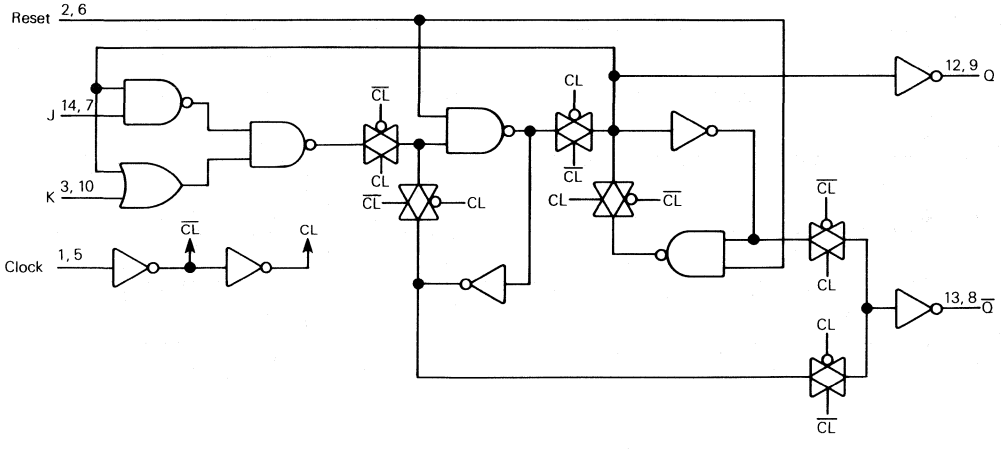
LOGIC DIAGRAM



MOTOROLA

MC54/74HC74

Advance Information

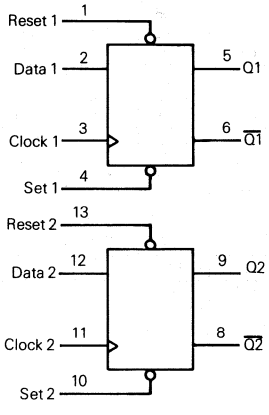
DUAL D-TYPE FLIP-FLOP WITH SET AND RESET

The MC54/74HC74 is identical in pinout to the LS74. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two D-type flip-flops with individual Set, Reset, and Clock inputs. Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and $\overline{Q}$ outputs are available from each flip-flop. The Set and Reset inputs are asynchronous.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 40 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

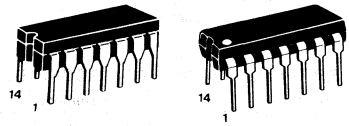
BLOCK DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL D-TYPE FLIP-FLOP WITH SET AND RESET



J SUFFIX
CERAMIC PACKAGE
CASE 632

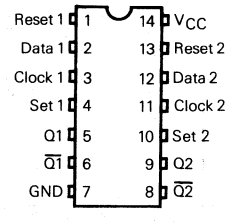
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

* Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	4	40	80	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	40	30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$	20	30	ns
t_{PHL}	(Figures 1 and 4)	20	30	
t_{PLH}	Maximum Propagation Delay, Set or Reset to Q or $\overline{Q}$	25	40	ns
t_{PHL}	(Figures 2 and 4)	25	40	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	11	5	4	4	MHz
		4.5	54	27	21	18	
		6.0	64	32	25	21	
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PHL}		2.0	88	175	221	261	
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PLH}	Maximum Propagation Delay, Set or Reset to Q or $\overline{Q}$ (Figures 2 and 4)	2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{PHL}		2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (per Flip-Flop)		60	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Clock to Data (Figure 3)	2.0	−5	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−5	0	0	0	
t_{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0	−10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

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SWITCHING WAVEFORMS

FIGURE 1

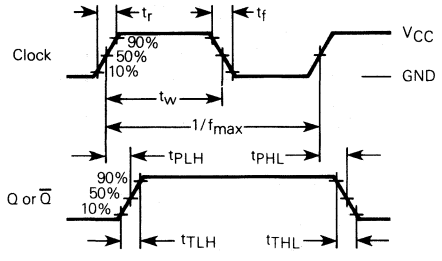


FIGURE 2

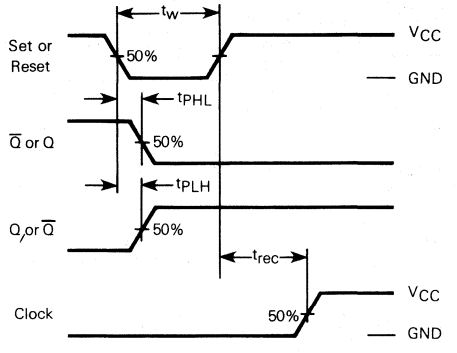


FIGURE 3

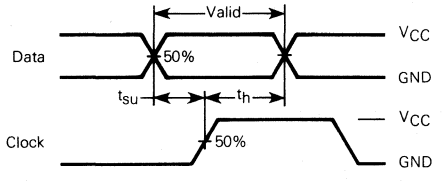
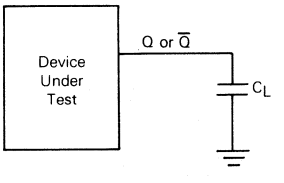


FIGURE 4 — TEST CIRCUIT



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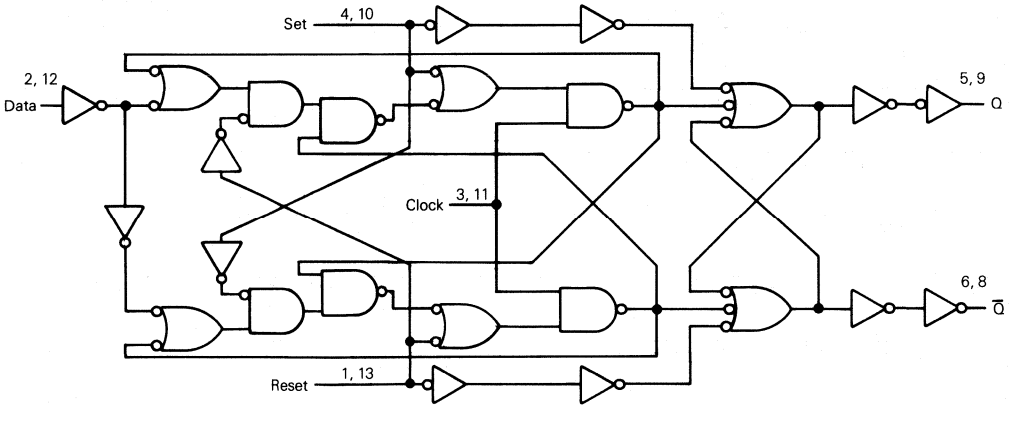
LOGIC DIAGRAM



MOTOROLA

MC54/74HC75

Advance Information

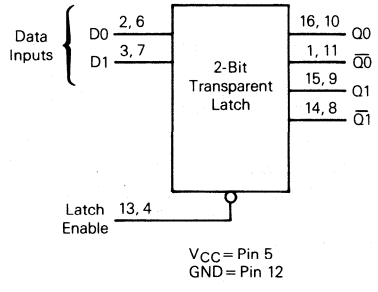
DUAL 2-BIT TRANSPARENT LATCH

The MC54/74HC75 is identical in pinout to the LS75. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 2-bit transparent latches. Each latch stores the input data while Latch Enable is at a logic low. The outputs follow the data inputs when Latch Enable is at a logic high.

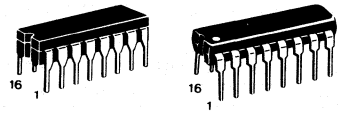
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 40 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM



HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL 2-BIT TRANSPARENT LATCH



J SUFFIX
CERAMIC PACKAGE
CASE 620

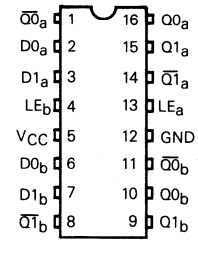
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs	
D	Latch Enable	Q	Q̄
L	H	L	H
H	H	H	L
X	L	Q_0	$\bar{Q}_0$

X = Don't Care
Q_0 = Latched Data

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	4	40	80	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, D to Q (Figure 1)	14	23	ns
t_{PHL}		14	23	
t_{PLH}	Maximum Propagation Delay, D to $\overline{Q}$ (Figure 1)	10	20	ns
t_{PHL}		10	20	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Q (Figure 2)	16	27	ns
t_{PHL}		16	27	
t_{PHL}	Maximum Propagation Delay, Latch Enable to $\overline{Q}$ (Figure 2)	11	23	ns
t_{PLH}		11	23	
t_{TLH}, t_{THL}	Maximum Output Transition Time (Figure 3)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125° 54HC	Unit
t_{PLH}	Maximum Propagation Delay, D to Q (Figure 1)	2.0	37	125	156	188	ns
		4.5	15	25	32	38	
		6.0	14	21	27	32	
t_{PHL}		2.0	37	125	156	188	ns
		4.5	15	25	32	38	
		6.0	14	21	27	32	
t_{PLH}	Maximum Propagation Delay, D to $\overline{Q}$ (Figure 1)	2.0	29	110	138	165	ns
		4.5	12	22	28	33	
		6.0	11	19	24	29	
t_{PHL}		2.0	29	110	138	165	ns
		4.5	12	22	28	33	
		6.0	11	19	24	29	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Q (Figure 2)	2.0	40	145	181	218	ns
		4.5	18	29	36	44	
		6.0	16	25	31	38	
t_{PHL}		2.0	40	145	181	218	ns
		4.5	18	29	36	44	
		6.0	16	25	31	38	
t_{PLH}	Maximum Propagation Delay, Latch Enable to $\overline{Q}$ (Figure 2)	2.0	36	125	156	183	ns
		4.5	15	25	31	38	
		6.0	14	22	28	33	
t_{PHL}		2.0	36	125	156	183	ns
		4.5	15	25	31	38	
		6.0	14	22	28	33	
t_{TLH}, t_{THL}	Maximum Output Transition Time (Figure 3)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	40	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption (Per 2-Bit Latch): $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{su}	Minimum Setup Time, D to Latch Enable (Figure 4)	2.0	50	100	125	150	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Latch Enable to D (Figure 4)	2.0	−20	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−3	0	0	0	
t_w	Minimum Pulse Width, Latch Enable Input (Figure 4)	2.0	40	80	100	120	ns
		4.5	8	16	20	24	
		6.0	7	14	18	21	
t_r, t_f	Maximum Input Rise and Fall Time	–	1000	500	500	500	ns

SWITCHING WAVEFORMS

FIGURE 1

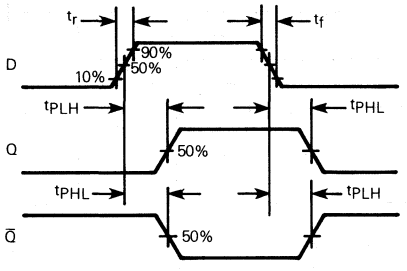


FIGURE 2

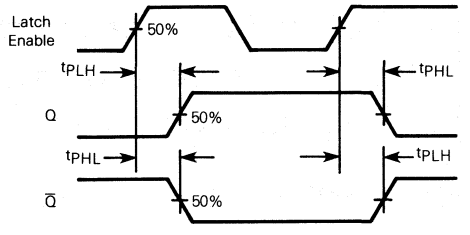


FIGURE 3

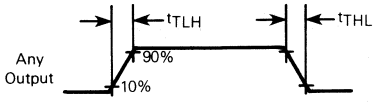
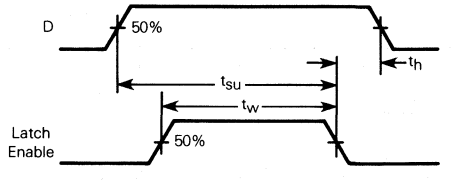
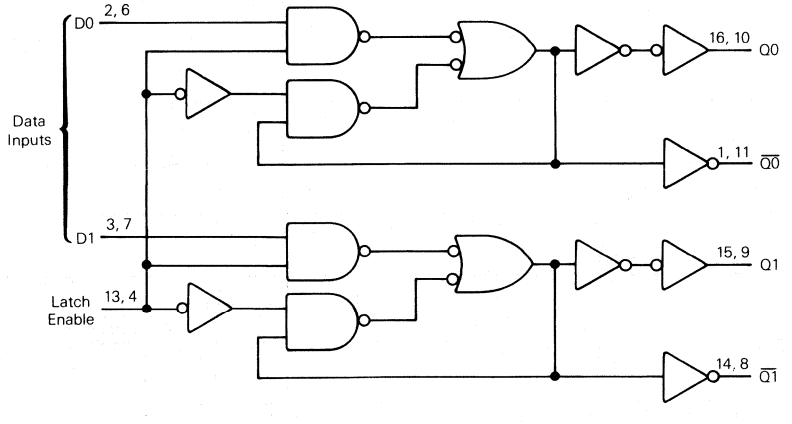


FIGURE 4



LOGIC DIAGRAM



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MOTOROLA

MC54/74HC76

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL J-K FLIP-FLOP WITH SET AND RESET

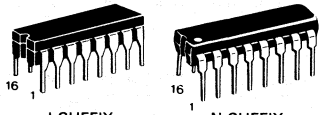
DUAL J-K FLIP-FLOP WITH SET AND RESET

The MC54/74HC76 is identical in pinout to the LS76. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has active-low asynchronous Set and Reset inputs.

The HC76 is identical in function to the HC112, but has a different pinout.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 40 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs
- Similar in Function to the LS76 Except When Set and Reset are Low Simultaneously



J SUFFIX
CERAMIC PACKAGE
CASE 620

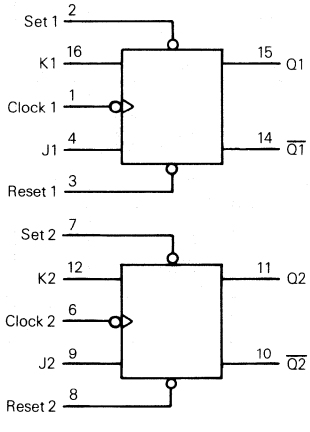
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

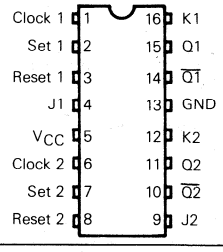
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 5
GND = Pin 13

PIN ASSIGNMENT



FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	No Change	
H	H	↓	L	H	L	H
H	H	↓	H	L	H	L
H	H	↓	H	H	Toggle	
H	H	L	X	X	No Change	
H	H	H	X	X	No Change	
H	H	↑	X	X	No Change	

*Both outputs will remain low as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	4	40	80	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC		Unit
		Typical	Guaranteed Limit	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	50	30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$	16	21	ns
t_{PHL}	(Figures 1 and 4)	16	21	
t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$	21	26	ns
t_{PHL}	(Figures 2 and 4)	21	26	
t_{PLH}	Maximum Propagation Delay, Set to Q or $\overline{Q}$	23	28	ns
t_{PHL}	(Figures 2 and 4)	23	28	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
			Typical	Guaranteed Limit			
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	9	5	4	3	MHz
		4.5	45	27	21	18	
		6.0	53	31	24	20	
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	2.0	100	126	160	183	ns
		4.5	20	25	32	37	
		6.0	17	22	27	32	
t_{PHL}		2.0	100	126	160	183	ns
		4.5	20	25	32	37	
		6.0	17	22	27	32	
t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$ (Figures 2 and 4)	2.0	126	155	191	250	ns
		4.5	25	31	39	47	
		6.0	22	26	33	40	
t_{PHL}		2.0	126	155	191	250	ns
		4.5	25	31	39	47	
		6.0	22	26	33	40	
t_{PLH}	Maximum Propagation Delay, Set to Q or $\overline{Q}$ (Figures 2 and 4)	2.0	137	165	210	240	ns
		4.5	28	33	41	50	
		6.0	23	28	35	40	
t_{PHL}		2.0	137	165	210	250	ns
		4.5	28	33	41	50	
		6.0	23	28	35	40	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	30	75	95	110	ns
		4.5	8	15	19	22	
		6.0	7	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (per Flip-Flop)		80	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
			Typical	Guaranteed Limit			
t_{su}	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	77	100	125	150	ns
		4.5	15	20	25	30	
		6.0	13	17	21	25	
t_h	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	−20	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−3	0	0	0	
t_{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0	55	100	125	150	ns
		4.5	11	20	25	30	
		6.0	9	17	21	25	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

SWITCHING WAVEFORMS

FIGURE 1

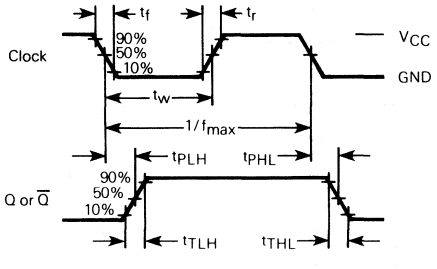


FIGURE 2

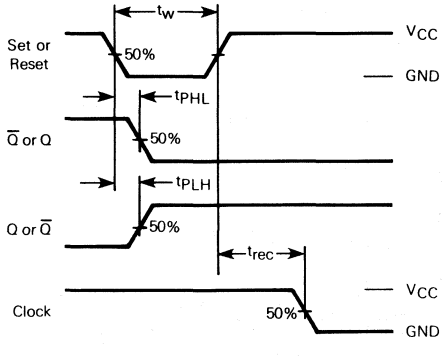


FIGURE 3

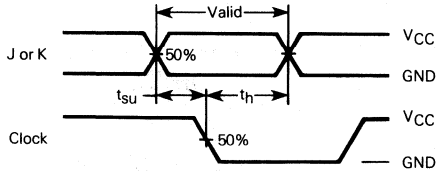
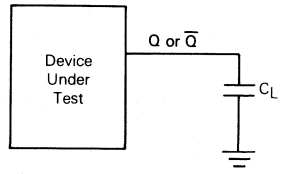
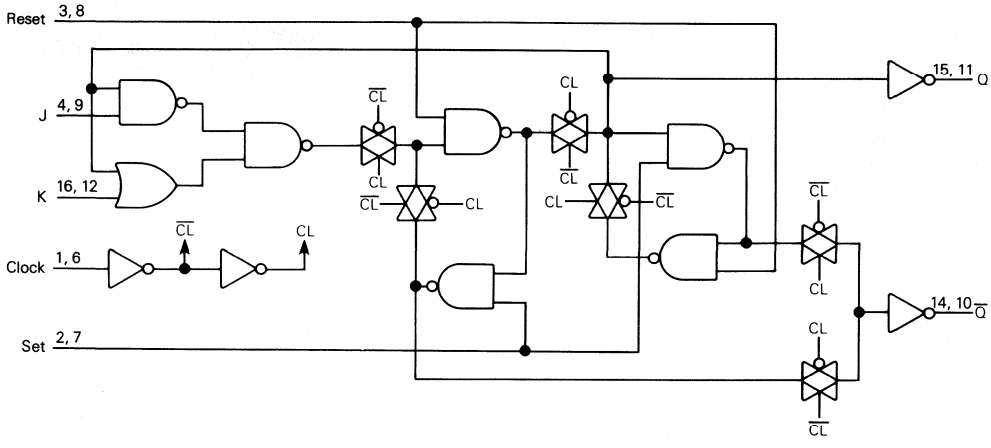


FIGURE 4



LOGIC DIAGRAM



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MOTOROLA

MC54/74HC85

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

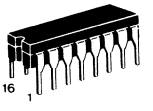
4-BIT MAGNITUDE COMPARATOR

4-BIT MAGNITUDE COMPARATOR

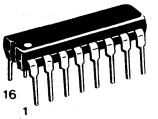
The MC54/74HC85 is identical in pinout to the LS85. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This 4-Bit Magnitude Comparator compares two 4-bit words and gives a high voltage level on either the $A > B_{out}$, $A = B_{out}$, or $A < B_{out}$ output, leaving the other two at a low voltage level. This device also has $A > B_{in}$, $A = B_{in}$, and $A < B_{in}$ inputs, eliminating the need for external gates when cascading.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620



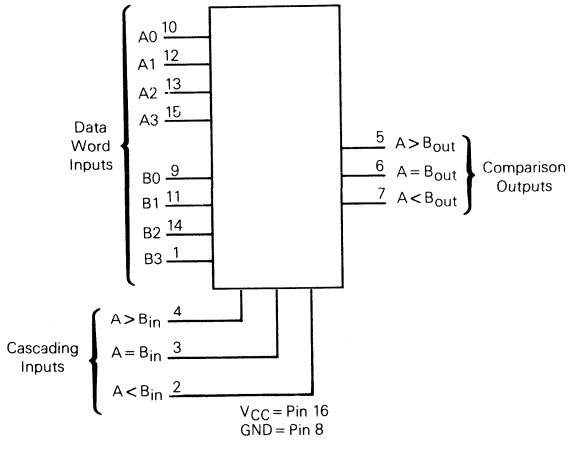
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

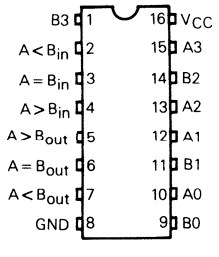
54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Inputs A or B to Outputs A>B or A<B	21	40	ns
t_{PHL}	(Figures 1 and 2)	21	40	
t_{PLH}	Maximum Propagation Delay, Inputs A or B to Output A = B	18	35	ns
t_{PHL}	(Figure 1 and 2)	18	35	
t_{PLH}	Maximum Propagation Delay, Input A<B or A = B to Output A>B	16	30	ns
t_{PHL}	(Figures 1 and 2)	16	30	
t_{PLH}	Maximum Propagation Delay, Input A>B or A = B to Output A<B	16	30	ns
t_{PHL}	(Figures 1 and 2)	16	30	
t_{PLH}	Maximum Propagation Delay, Input A = B to Output A = B	13	25	ns
t_{PHL}	(Figures 1 and 2)	13	25	
t_{TLH}, t_{THL}	Maximum Output Transition Tin.e, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Outputs A>B or A<B (Figures 1 and 2)	2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{PHL}		2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{PLH}	Maximum Propagation Delay, Inputs A or B to Output A = B (Figures 1 and 2)	2.0	100	200	252	298	ns
		4.5	20	40	50	60	
		6.0	17	34	43	51	
t_{PHL}		2.0	100	200	252	298	ns
		4.5	20	40	50	60	
		6.0	17	34	43	51	
t_{PLH}	Maximum Propagation Delay, Input A<B or A = B to Output A>B (Figures 1 and 2)	2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PHL}		2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PLH}	Maximum Propagation Delay, Input A>B or A = B to Output A<B (Figures 1 and 2)	2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PHL}		2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PLH}	Maximum Propagation Delay, Input A = B to Output A = B (Figures 1 and 2)	2.0	73	145	183	216	ns
		4.5	15	29	37	43	
		6.0	12	25	31	37	
t_{PHL}		2.0	73	145	183	216	ns
		4.5	15	29	37	43	
		6.0	12	25	31	37	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		75	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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FIGURE 1 — SWITCHING WAVEFORMS

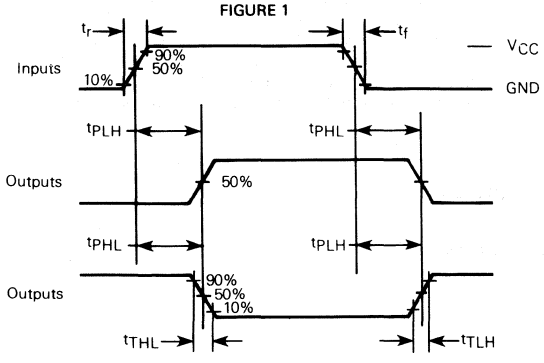
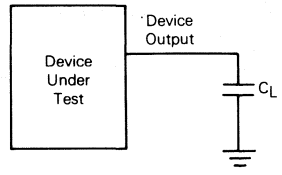


FIGURE 2 — TEST CIRCUIT



FUNCTION TABLE

Data Word Inputs				Cascading Inputs			Output		
A3, B3	A2, B2	A1, B1	A0, B0	$A>B_{in}$	$A=B_{in}$	$A<B_{in}$	$A>B_{out}$	$A=B_{out}$	$A<B_{out}$
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	L	H
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	L	H
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	L	H
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	L	H
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	H	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	X	H	X	L	H	L

X = Don't Care

PIN DESCRIPTIONS

INPUTS

A0, A1, A2, A3 (Pins 10, 12, 13, 15) — Data Word A Inputs. The data word present at these inputs is compared to Data Word B. A3 is the most significant bit and A0 is the least significant bit.

B0, B1, B2, B3 (Pins 9, 11, 14, 1) — Data Word B Inputs. The data word present at these inputs is compared to Data Word A. B3 is the most significant bit and B0 is the least significant bit.

CONTROLS

$A>B_{in}$, $A=B_{in}$, $A<B_{in}$ (Pins 4, 3, 2) — Cascading Inputs. These inputs determine the states of the outputs only when data word A equals data word B. The $A=B_{in}$ input overrides both the $A>B_{in}$ and $A<B_{in}$ inputs.

For single stage operation or for the least significant stage in cascaded operation, the $A<B_{in}$ and $A>B_{in}$ inputs should be tied to ground and the $A=B_{in}$ input tied to V_{CC}. Between cascaded comparators, the $A<B_{out}$, $A=B_{out}$, and $A>B_{out}$ outputs should be tied to $A<B_{in}$, $A=B_{in}$, and $A>B_{in}$, respectively, of the succeeding stage.

5

OUTPUTS

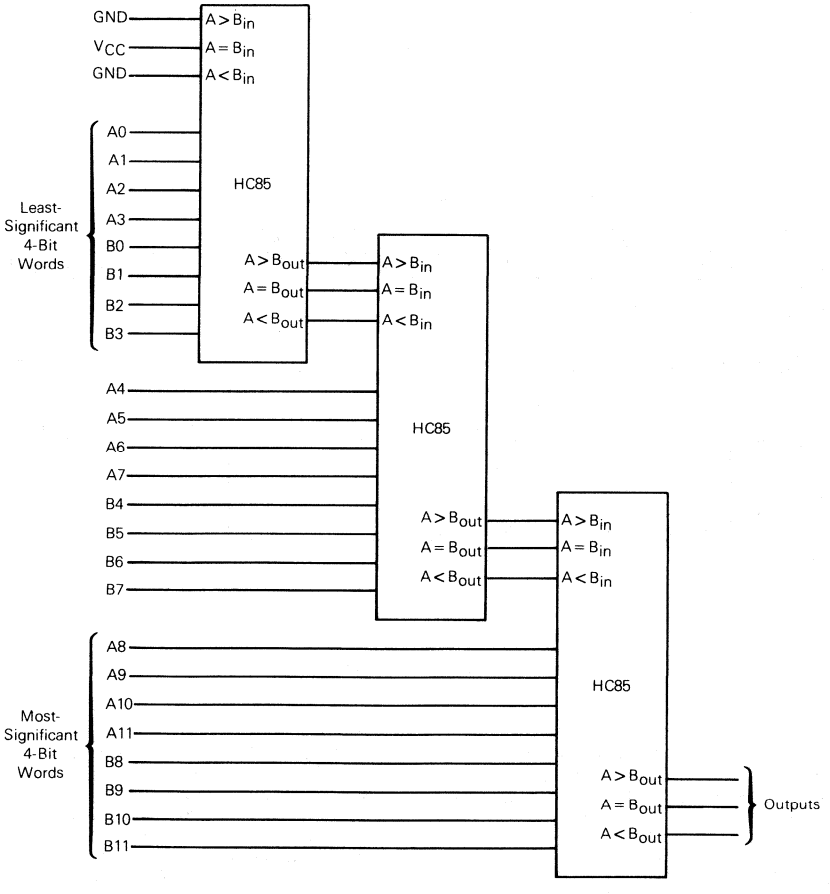
$A > B_{out}$ (Pin 5) — A-Greater-Than-B Output. This output is at a high voltage level when word A is greater than word B, regardless of the data present at the cascading inputs. This output is also high when word A equals word B and the $A > B_{in}$ input is high ($A < B_{in}$ and $A = B_{in}$ are at a low voltage level).

$A = B_{out}$ (Pin 6) — A-Equals-B Output. This output is high when word A equals word B and the $A = B_{in}$ input is high. $A < B_{in}$ and $A > B_{in}$ have no effect when the comparator is in this condition and $A = B_{in}$ is at a high voltage level.

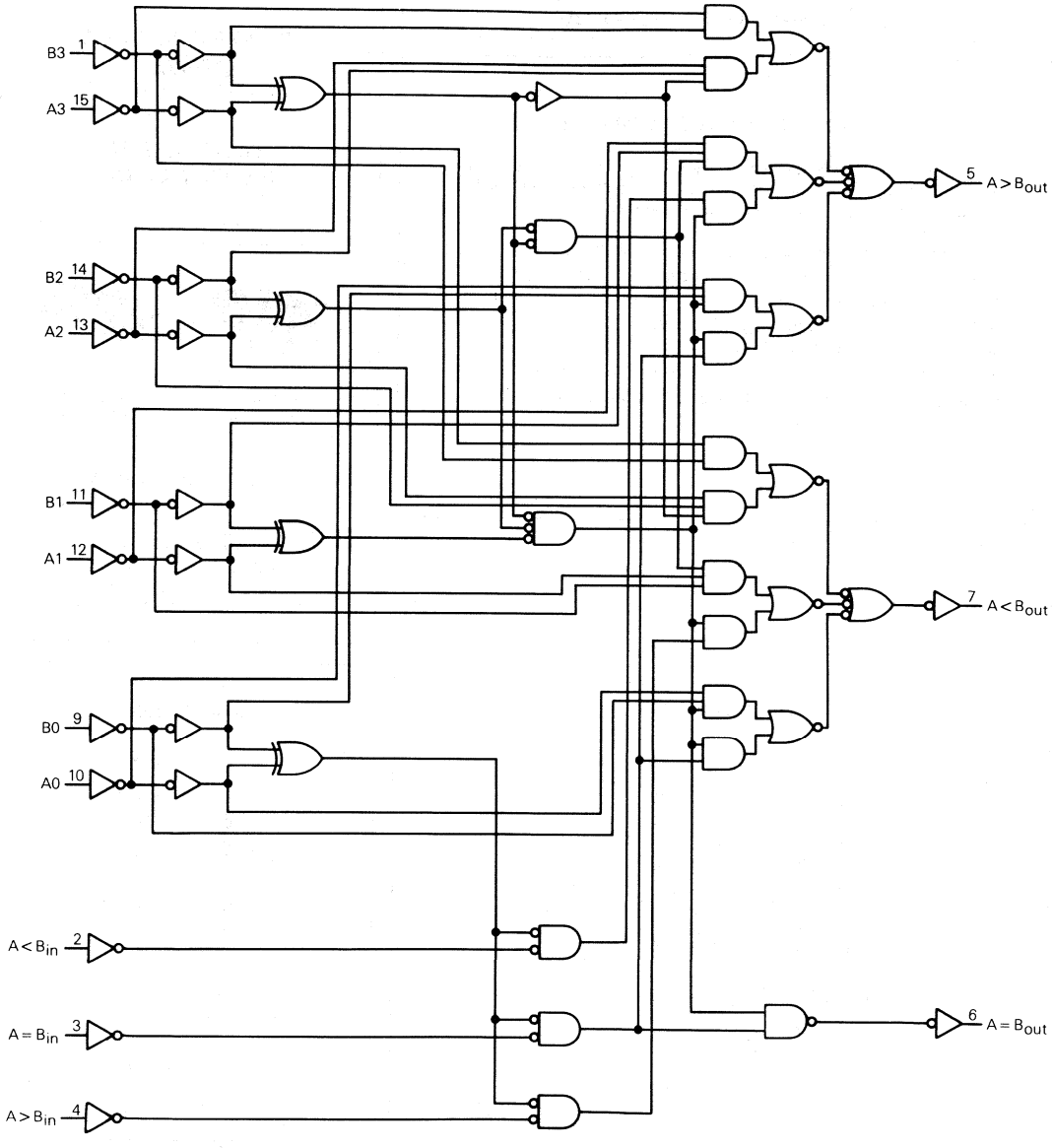
$A < B_{out}$ (Pin 7) — A-Less-Than-B Output. This output is at a high voltage level when word A is less than word B, regardless of data present at the cascading inputs. This output is also high when word A equals word B and the $A < B_{in}$ input is high ($A > B_{in}$ and $A = B_{in}$ are at a low voltage level).

TYPICAL APPLICATION

CASCADING COMPARATORS



LOGIC DIAGRAM



MOTOROLA

MC54/74HC86

Advance Information

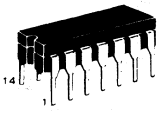
QUAD 2-INPUT EXCLUSIVE OR GATE

The MC54/74HC86 is identical in pinout to the LS86. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

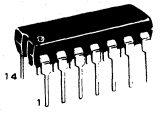
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD 2-INPUT EXCLUSIVE OR GATE



J SUFFIX
CERAMIC PACKAGE
CASE 632

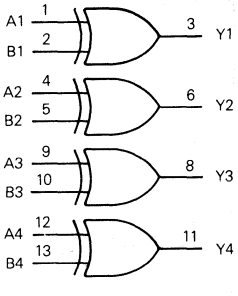


N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)
74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

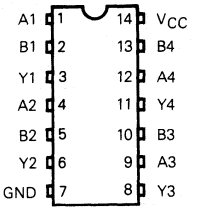
FUNCTION DIAGRAM



$Y = A \oplus B$
$= \bar{A}B + A\bar{B}$

V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



TRUTH TABLE

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

5

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output Y	8	20	ns
t_{PHL}	(Figures 1 and 2)	9	20	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	60	120	151	179	ns
		4.5	12	24	30	36	
		6.0	10	20	26	30	
t_{PHL}		2.0	60	120	151	179	ns
		4.5	12	24	30	36	
		6.0	10	20	26	30	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	33	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption per gate:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS

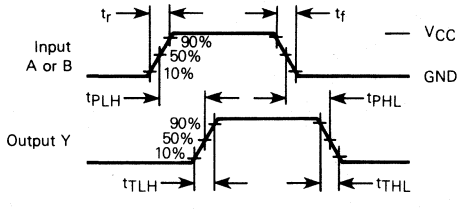
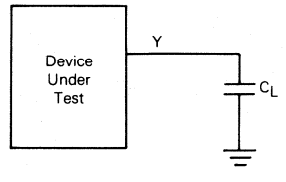
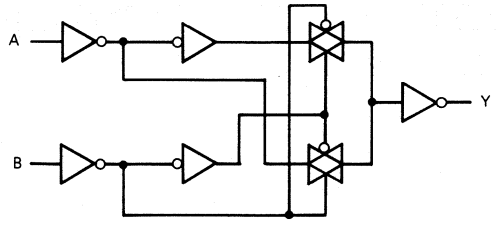


FIGURE 2 — TEST CIRCUIT



LOGIC DIAGRAM
(¼ of Device)



MOTOROLA

MC54/74HC90

Product Preview

4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷5 SECTIONS

The MC54/74HC90 is identical in pinout to the LS90. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC90 is a 4-bit ripple type counter consisting of four master/slave flip-flops that are internally connected to provide separate divide-by-two and divide-by-five sections. Each section has a separate Clock input which initiates state changes of the counter on the high-to-low clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC90. Q_A is the output of the divide-by-two section; Q_B, Q_C, and Q_D are the binary outputs of the divide-by-five section.

A gated AND asynchronous Reset is provided which resets all the flip-flops to a low logic level. A gated AND asynchronous Set is provided which overrides the clocks and the Reset inputs and sets the outputs to nine (HLLH).

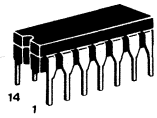
Because the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

1. A BCD Counter — The Clock B input must be externally connected to the Q_A output. The Clock A input receives the incoming count and a BCD count sequence is produced.
2. A Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_D output must be externally connected to the Clock A input. The input count is then applied to the Clock B input and a divide-by-ten square wave is obtained at output Q_A.
3. Divide-By-Two and Divide-By-Five Counters — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function, (with the Clock A as the input and Q as the output). The Clock B input is used to obtain binary divide-by-five operation at the Q_D output.

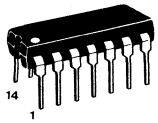
- Choice of Counting Modes: BCD, ÷2, ÷5, and ÷10
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷5 SECTIONS



J SUFFIX
CERAMIC PACKAGE
CASE 632



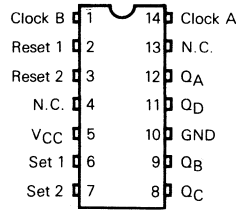
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

PIN ASSIGNMENT

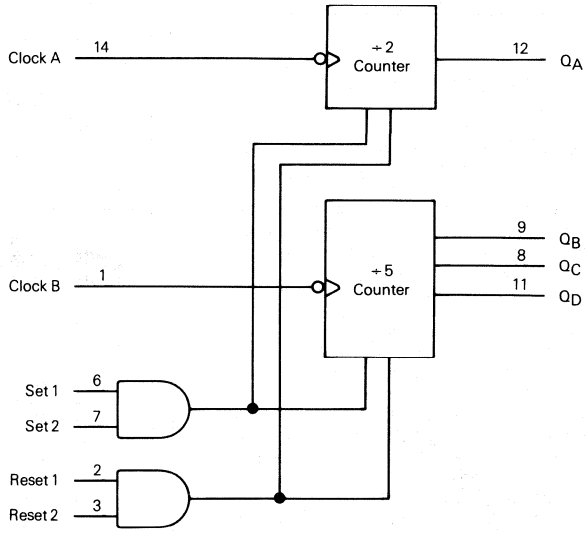


N.C. = No Connection

MODE SELECTION TABLE

Inputs					Outputs	
Reset		Set				
1	2	1	2	Clock	$Q_D Q_C Q_B$	Q_A
H	H	L	X	X	L L L	L
H	H	X	L	X	L L L	L
X	X	H	H	X	H L L	H
L	X	L	X	↘	Count	Toggle
X	L	X	L	↘	Count	Toggle
L	X	X	L	↘	Count	Toggle
X	L	L	X	↘	Count	Toggle

BLOCK DIAGRAM



V_{CC} = Pin 5
GND = Pin 10
No Connection = Pins 4, 13

5

MOTOROLA

MC54/74HC92

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷6 SECTIONS

4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷6 SECTIONS

The MC54/74HC92 is identical in pinout to the LS92. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC92 is a 4-bit ripple counter consisting of a four master/sale flip-flops that are internally connected to provide separate divide-by-two and divide-by-six sections. Each section has a separate Clock input which initiates state changes of the counter on the high-to-low clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC92. Q_A is the output of the divide-by-two section; Q_B, Q_C and Q_D are the binary outputs of the divide-by-six section.

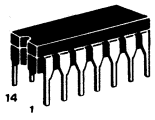
A gated AND asynchronous Reset is provided which resets all the flip-flops.

Because the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

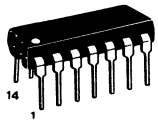
1. A Modulo-12, Divide-By-Twelve Counter — The Clock B input must be externally connected to the Q_A output. The Clock A input receives the incoming count and Q_D produces a symmetrical divide-by-twelve square wave output.
2. Divide-By-Two and Divide-By-Six Counters — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The Clock B input is used to obtain divide-by-three operation at the Q_B and Q_C outputs and divide-by-six operation at the Q_D output.

- Choice of Counting Modes: ÷2, ÷6, and ÷12
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

PRODUCT CANCELLED



J SUFFIX
CERAMIC PACKAGE
CASE 632



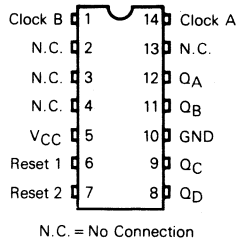
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

PIN ASSIGNMENT



N.C. = No Connection

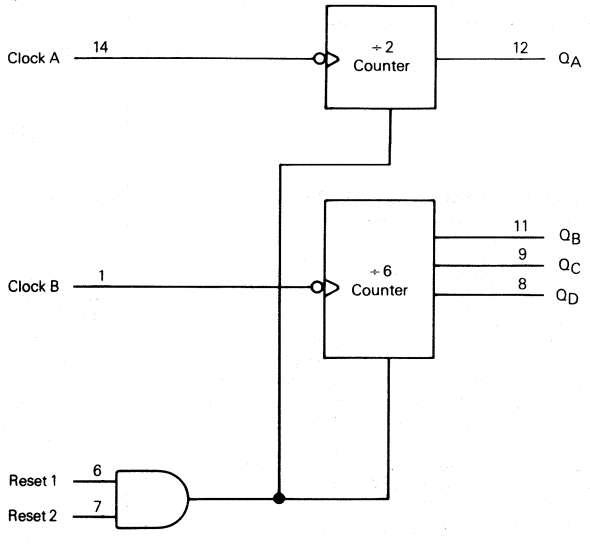
MODE SELECTION TABLE

Inputs			Outputs			
Reset 1	Reset 2	Clock	Q_D	Q_C	Q_B	Q_A
H	H	X	L	L	L	L
L	H	↘	Count			Toggle
H	L	↘	Count			Toggle
L	L	↘	Count			Toggle

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

5

BLOCK DIAGRAM



V_{CC} = Pin 5
GND = Pin 10
No Connection = Pins 2, 3, 4, 13

5

MOTOROLA

MC54/74HC93

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷8 SECTIONS

4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷8 SECTIONS

The MC54/74HC93 is identical in pinout to the LS93. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

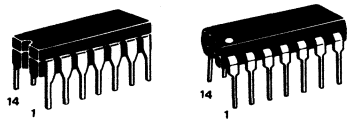
The HC93 is a 4-bit ripple type counter consisting of four master/slave flip-flops that are internally connected to provide separate divide-by-two and divide-by-eight sections. Each section has a separate Clock input which initiates state changes of the counter on the high-to-low clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC93. Q_A is the output of the divide-by-two section, while Q_B, Q_C, and Q_D are the binary outputs of the divide-by-eight section.

A gated AND asynchronous Reset is provided which resets all the flip-flops.

Because the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

1. A 4-Bit Ripple Counter — The Q_A output must be externally connected to the Clock B input. The input count pulses are applied to the Clock A input. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs.
2. A 3-Bit Ripple Counter — The input count pulses are applied to the Clock B input. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

- Choice of Counting Modes: ÷2, ÷8, and ÷16
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632

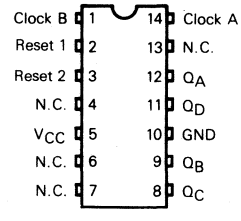
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

PIN ASSIGNMENT



N.C. = No Connection

MODE SELECTION TABLE

Inputs			Outputs			
Reset 1	Reset 2	Clock	Q_D	Q_C	Q_B	Q_A
H	H	X	L	L	L	L
L	H	↘	Count			Toggle
H	L	↘	Count			Toggle
L	L	↘	Count			Toggle

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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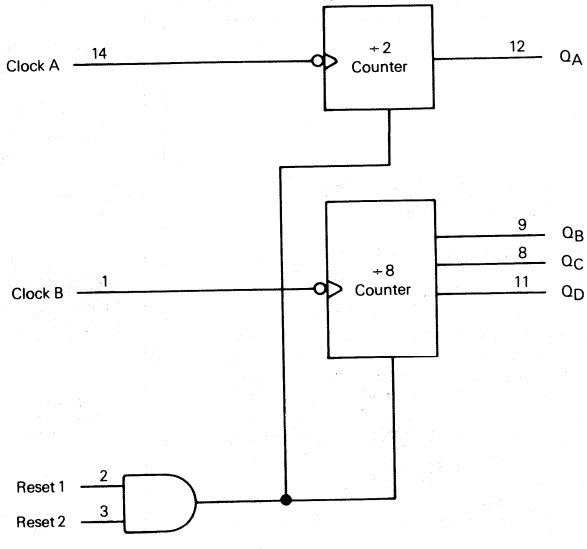
BLOCK DIAGRAM



V_{CC} = Pin 5
GND = Pin 10
No Connection = Pins 4, 6, 7, 13

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MOTOROLA

MC54/74HC107

Advance Information

DUAL J-K FLIP-FLOP WITH RESET

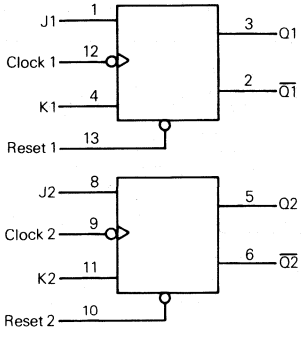
The MC54/74HC107 is identical in pinout to the LS107. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has an active-low asynchronous reset.

The HC107 is identical in function to the HC73, but has a different pinout.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 40 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM

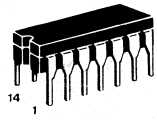


V_{CC} = Pin 14
GND = Pin 7

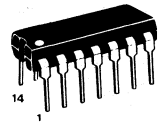
This document contains information on a new product. Specifications and information herein are subject to change without notice.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL J-K FLIP-FLOP WITH RESET



J SUFFIX
CERAMIC PACKAGE
CASE 632



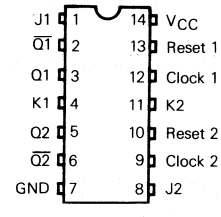
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs	
Reset	Clock	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	No Change	
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	H	H	Toggle	
H	L	X	X	No Change	
H	H	X	X	No Change	
H	↑	X	X	No Change	

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	4	40	80	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	50	30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	16	21	ns
t_{PHL}		16	21	
t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$ (Figures 2 and 4)	21	26	ns
t_{PHL}		21	26	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	9	5	4	3	MHz
		4.5	45	27	21	18	
		6.0	53	31	24	20	
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	2.0	100	126	160	185	ns
		4.5	20	25	32	37	
		6.0	17	21	27	32	
t_{PHL}		2.0	100	126	160	185	ns
		4.5	20	25	32	37	
		6.0	17	21	27	32	
t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$ (Figures 2 and 4)	2.0	126	155	194	250	ns
		4.5	25	31	39	47	
		6.0	21	26	32	40	
t_{PHL}		2.0	126	155	194	250	ns
		4.5	25	31	39	47	
		6.0	21	26	32	40	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (per Flip-Flop)		80	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	77	100	125	150	ns
		4.5	15	20	25	30	
		6.0	13	17	21	25	
t_h	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	−20	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−3	0	0	0	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	55	100	125	150	ns
		4.5	11	20	25	30	
		6.0	9	17	21	25	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

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SWITCHING WAVEFORMS

FIGURE 1

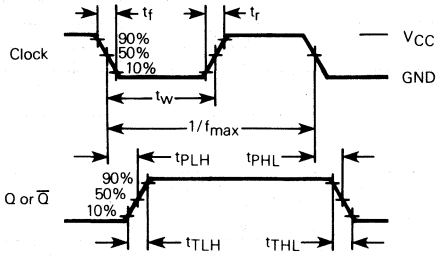


FIGURE 2

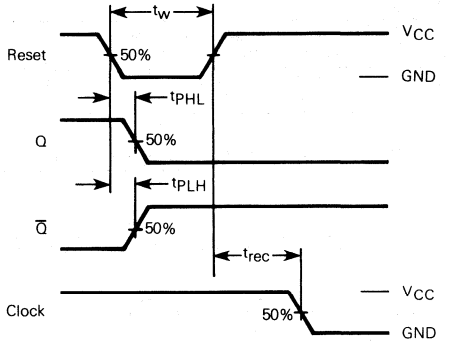


FIGURE 3

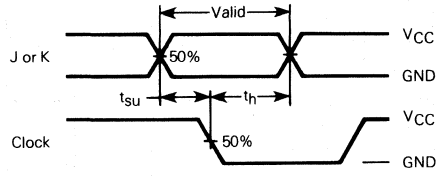
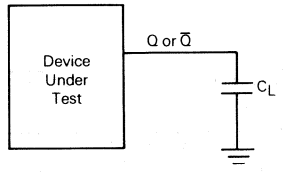


FIGURE 4



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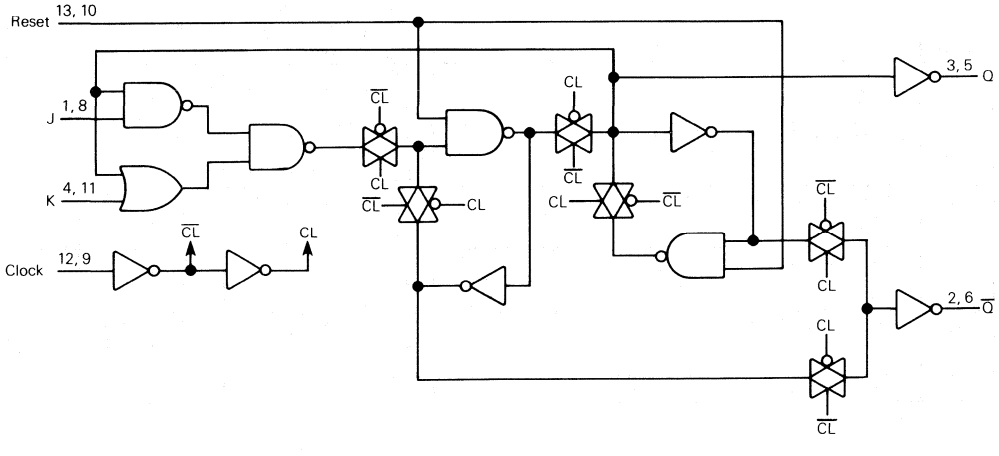
LOGIC DIAGRAM



MOTOROLA

MC54/74HC109

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

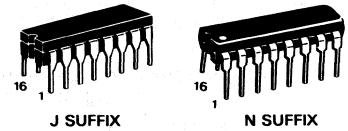
DUAL J-$\overline{K}$ FLIP-FLOP WITH SET AND RESET

DUAL J-$\overline{K}$ FLIP-FLOP WITH SET AND RESET

The MC54/74HC109 is identical in pinout to the LS109. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two J-$\overline{K}$ flip-flops with individual set, reset, and clock inputs. Changes at the inputs are reflected at the outputs with the next low to high transition of the clock. Both Q and $\overline{Q}$ outputs are available from each flip-flop.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 40 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620

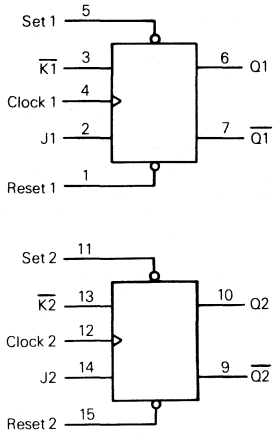
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

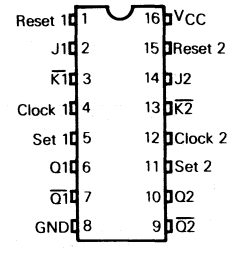
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	L	H
H	H	↓	H	L	Toggle	
H	H	↓	L	H	No Change	
H	H	↓	H	H	H	L
H	H	L	X	X	No Change	

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	4	40	80	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)		30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		30	ns
t_{PHL}	(Figures 1 and 4)		30	
t_{PLH}	Maximum Propagation Delay, Set or Reset to Q or $\overline{Q}$		40	ns
t_{PHL}	(Figures 2 and 4)		40	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	11	5	4	4	MHz
		4.5	54	27	21	18	
		6.0	64	32	25	21	
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PHL}		2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PLH}	Maximum Propagation Delay, Set or Reset to Q or $\overline{Q}$ (Figures 2 and 4)	2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{PHL}		2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (per Flip-Flop)			–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, J and $\overline{K}$ to Clock (Figure 3)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Clock to J and $\overline{K}$ (Figure 3)	2.0	−10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_{rec}	Minimum Recovery Time, Set or Reset (Figure 2)	2.0	−10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_w	Minimum Pulse Width, Set and Reset (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

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SWITCHING WAVEFORMS

FIGURE 1

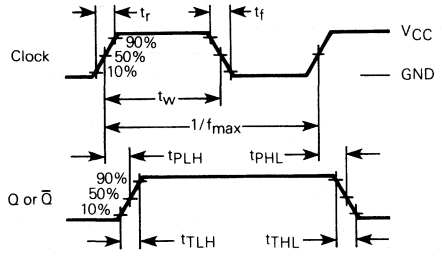


FIGURE 2

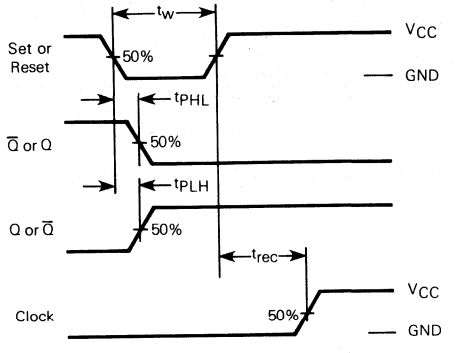


FIGURE 3

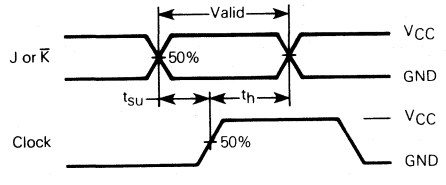
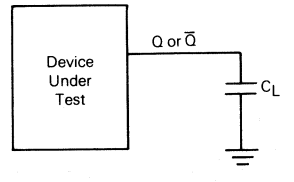


FIGURE 4



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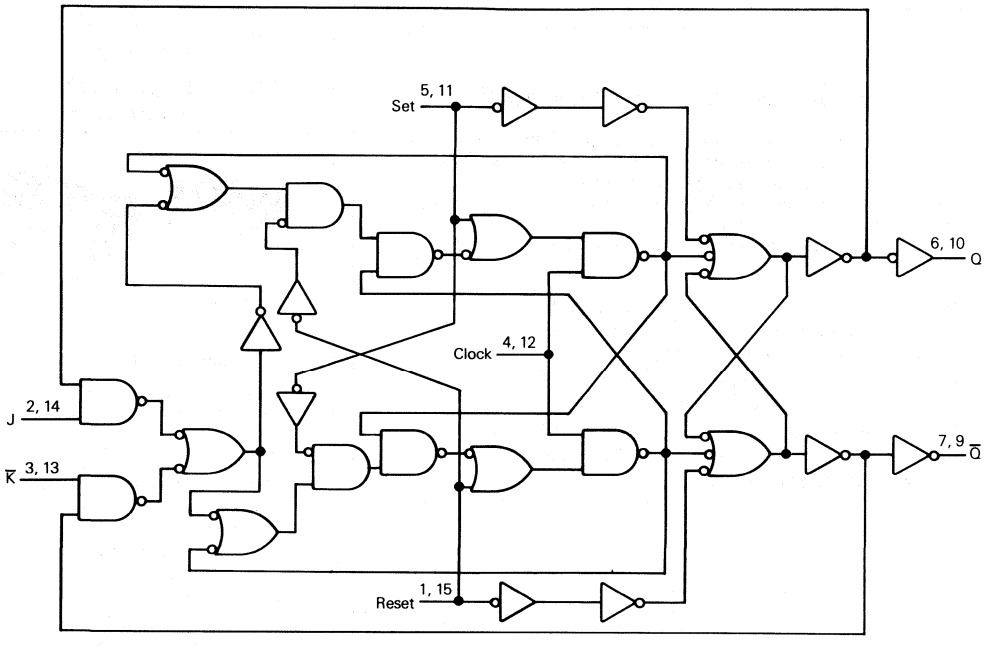
LOGIC DIAGRAM



5

MOTOROLA

MC54/74HC112

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL J-K FLIP-FLOP WITH
SET AND RESET

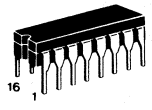
DUAL J-K FLIP-FLOP WITH SET AND RESET

The MC54/74HC112 is identical in pinout to the LS112. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

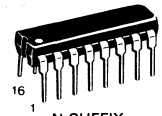
Each flip-flop is negative-edge clocked and has active-low asynchronous Set and Reset inputs.

The HC112 is identical in function to the HC76, but has a different pinout.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 40 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs
- Similar in Function to the LS112 Except When Set and Reset are Low Simultaneously



J SUFFIX
CERAMIC PACKAGE
CASE 620



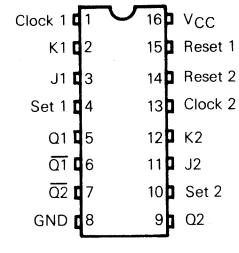
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

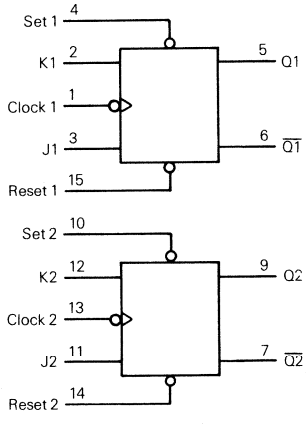
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	No Change	
H	H	↓	L	H	L	H
H	H	↓	H	L	H	L
H	H	↓	H	H	Toggle	
H	H	L	X	X	No Change	
H	H	H	X	X	No Change	
H	H	↑	X	X	No Change	

*Both outputs will remain low as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	4	40	80	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	50	30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$	16	21	ns
t_{PHL}	(Figures 1 and 4)	16	21	
t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$	21	26	ns
t_{PHL}	(Figures 2 and 4)	21	26	
t_{PLH}	Maximum Propagation Delay, Set to Q or $\overline{Q}$	23	28	ns
t_{PHL}	(Figures 2 and 4)	23	28	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	9	5	4	3	MHz
		4.5	45	27	21	18	
		6.0	53	31	24	20	
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	2.0	100	126	160	183	ns
		4.5	20	25	32	37	
		6.0	17	21	27	32	
t_{PHL}		2.0	100	126	160	183	ns
		4.5	20	25	32	37	
		6.0	17	21	27	32	
t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$ (Figures 2 and 4)	2.0	126	155	191	250	ns
		4.5	25	31	39	47	
		6.0	22	26	33	40	
t_{PHL}		2.0	126	155	191	250	ns
		4.5	25	31	39	47	
		6.0	22	26	33	40	
t_{PLH}	Maximum Propagation Delay, Set to Q or $\overline{Q}$ (Figures 2 and 4)	2.0	137	165	210	240	ns
		4.5	28	33	41	50	
		6.0	23	28	35	40	
t_{PHL}		2.0	137	165	210	240	ns
		4.5	28	33	41	50	
		6.0	23	28	35	40	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	30	75	95	110	ns
		4.5	8	15	19	22	
		6.0	7	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (per Flip-Flop)		80	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	77	100	125	150	ns
		4.5	15	20	25	30	
		6.0	13	17	21	25	
t_h	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	−20	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−3	0	0	0	
t_{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0	55	100	125	150	ns
		4.5	11	20	25	30	
		6.0	9	17	21	25	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

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SWITCHING WAVEFORMS

FIGURE 1

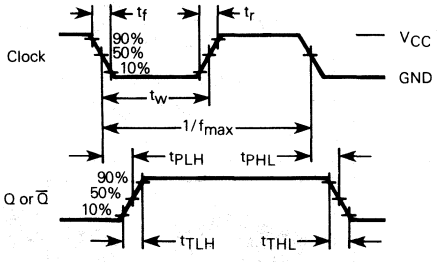


FIGURE 2

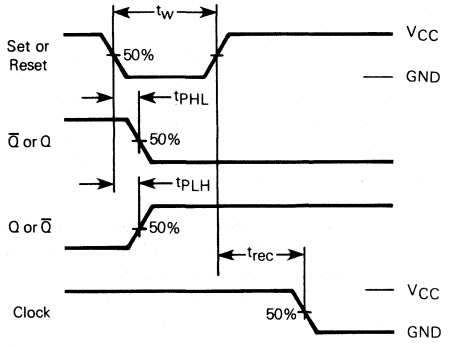


FIGURE 3

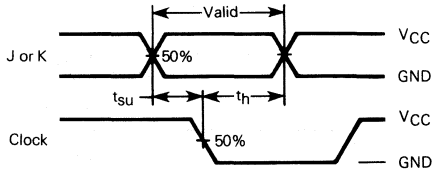
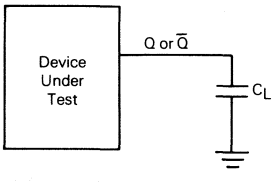
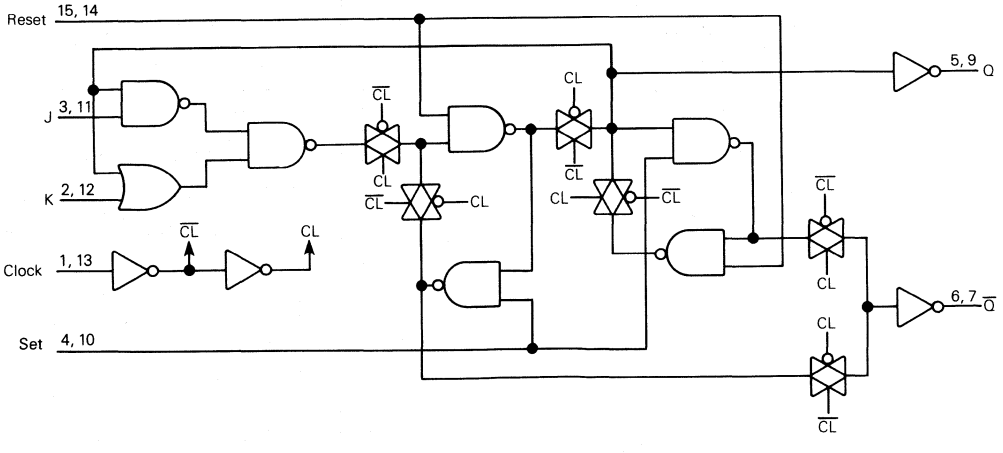


FIGURE 4



LOGIC DIAGRAM



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MOTOROLA

MC54/74HC113

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

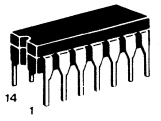
DUAL J-K FLIP-FLOP WITH SET

DUAL J-K FLIP-FLOP WITH SET

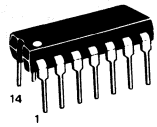
The MC54/74HC113 is identical in pinout to the LS113. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has an active-low asynchronous set input.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 40 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632



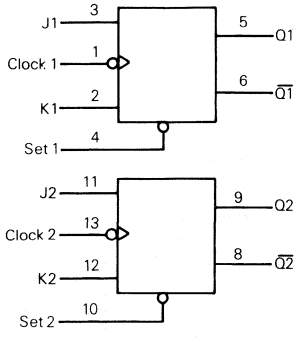
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

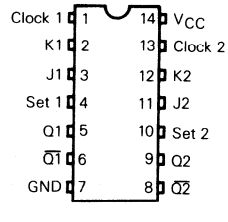
74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs	
Set	Clock	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	No Change	
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	H	H	Toggle	
H	H	X	X	No Change	
H	L	X	X	No Change	
H	↑	X	X	No Change	

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	4	40	80	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	50	30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$	16	21	ns
t_{PHL}	(Figures 1 and 4)	16	21	
t_{PLH}	Maximum Propagation Delay, Set to Q or $\overline{Q}$	21	26	ns
t_{PHL}	(Figures 2 and 4)	21	26	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	9	5	4	3	MHz
		4.5	45	27	21	18	
		6.0	53	31	24	20	
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	2.0	100	126	160	183	ns
		4.5	20	25	32	37	
		6.0	17	21	27	32	
t_{PHL}		2.0	100	126	160	183	ns
		4.5	20	25	32	37	
		6.0	17	21	27	32	
t_{PLH}	Maximum Propagation Delay, Set to Q or $\overline{Q}$ (Figures 2 and 4)	2.0	137	165	210	240	ns
		4.5	28	33	41	50	
		6.0	23	28	35	40	
t_{PHL}		2.0	137	165	210	240	ns
		4.5	28	33	41	50	
		6.0	23	28	35	40	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	30	75	95	110	ns
		4.5	8	15	19	22	
		6.0	7	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (per Flip-Flop)		80	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{su}	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	77	100	125	150	ns
		4.5	15	20	25	30	
		6.0	13	17	21	25	
t_h	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	−20	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−3	0	0	0	
t_{rec}	Minimum Recovery Time, Set Inactive to Clock (Figure 2)	2.0	55	100	125	150	ns
		4.5	11	20	25	30	
		6.0	9	17	21	25	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Set (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

SWITCHING WAVEFORMS

FIGURE 1

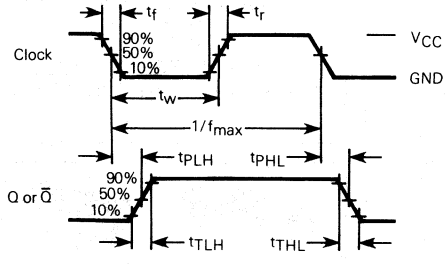


FIGURE 2

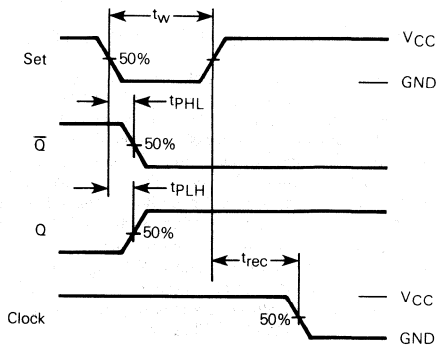


FIGURE 3

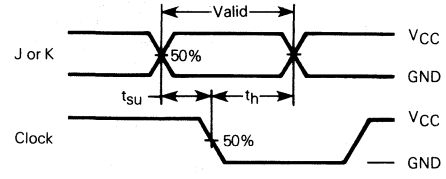
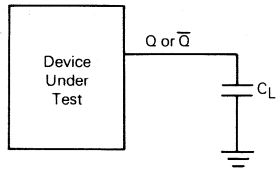
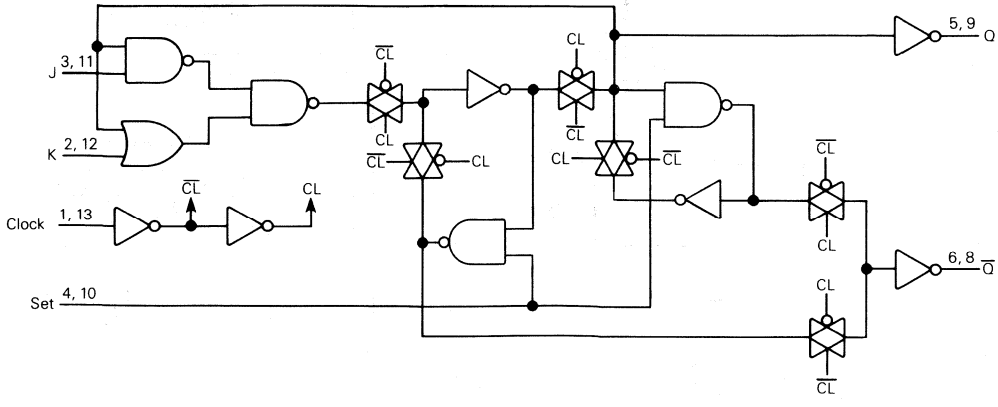


FIGURE 4 — TEST CIRCUIT



LOGIC DIAGRAM



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MOTOROLA

MC54/74HC123

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

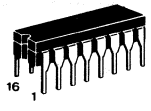
The MC54/74HC123 is identical in pinout to the LS123. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each multivibrator features an active-low asynchronous reset and both negative- and positive-edge triggered inputs, either of which can be used as an enable. The device may also be triggered by using the Reset pin. The output pulse width is dependent upon an external resistor and capacitor connection as shown in the block diagram.

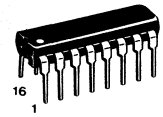
The HC123 has the same pinout as the HC221 and the HC423 monostable multivibrators. The HC221, however, is not retriggerable and the HC423 may not be triggered by using the Reset pin.

If more pulse-width accuracy is required, use the MC54/74HC4538 Precision Monostable Multivibrator.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620



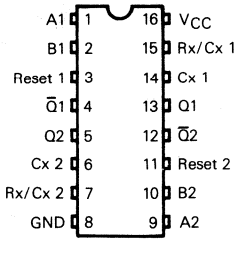
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

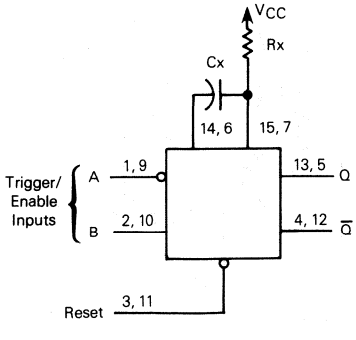
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

Inputs			Outputs	
A	B	Reset	Q	Q̄
X	X	L	L	H
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⎎
↓	H	H	⎍	⎎
L	H	↑	⎍	⎎

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MOTOROLA

MC54/74HC125
MC54/74HC126

Product Preview

QUAD 3-STATE NONINVERTING BUFFERS

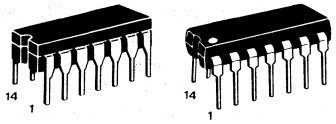
The MC54/74HC125 and MC54/74HC126 are identical in pinout to the LS125 an LS126. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC125 and HC126 noninverting buffers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The devices have four separate output enables that are active-low (HC125) or active-high (HC126).

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD 3-STATE NONINVERTING BUFFERS



J SUFFIX
CERAMIC PACKAGE
CASE 632

N SUFFIX
PLASTIC PACKAGE
CASE 646

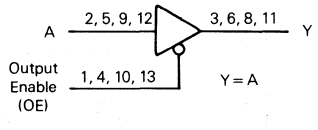
ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

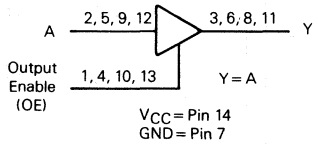
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

LOGIC DIAGRAMS

HC125
(¼ of the device)
Active-Low Output Enables

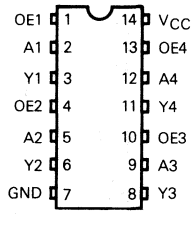


HC126
(¼ of the device)
Active-High Output Enables



V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



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MOTOROLA

MC54/74HC132

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

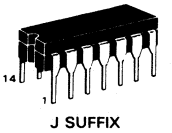
QUAD 2-INPUT
SCHMITT-TRIGGER NAND GATE

QUAD 2-INPUT SCHMITT-TRIGGER NAND GATE

The MC54/74HC132 is identical in pinout to the LS132. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC132 has hysteresis and can, therefore, be used to enhance noise immunity or to square up slowly changing waveforms.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632

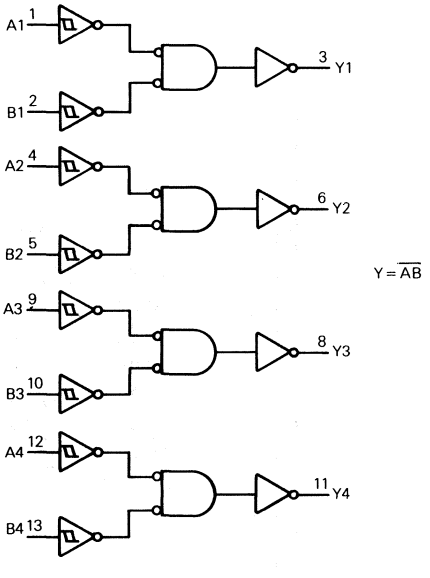
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

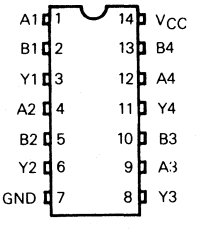
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

LOGIC DIAGRAM



$Y = \overline{AB}$

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	no limit	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed Limit		
V_{T+}	Maximum Positive-Going Threshold Voltage (Figure 3)	V_{out}=0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.40 2.70 3.40	1.50 3.15 4.20	1.50 3.15 4.20	1.50 3.15 4.20	V
V_{T+}	Minimum Positive-Going Threshold Voltage (Figure 3)	V_{out}=0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.40 2.70 3.40	1.00 2.30 3.00	0.95 2.25 2.95	0.95 2.25 2.95	V
V_{T-}	Maximum Negative-Going Threshold Voltage (Figure 3)	V_{out}=V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.5 1.50 2.10	0.90 2.00 2.60	0.95 2.05 2.65	0.95 2.05 2.65	V
V_{T-}	Minimum Negative-Going Threshold Voltage (Figure 3)	V_{out}=V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.5 1.50 2.10	0.30 0.90 1.20	0.30 0.90 1.20	0.30 0.90 1.20	V
V_H	Maximum Hysteresis Voltage (Figure 3)	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.90 1.20 1.30	1.20 2.25 3.00	1.20 2.25 3.00	1.20 2.25 3.00	V
V_H	Minimum Hysteresis Voltage (Figure 3)	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.90 1.20 1.30	0.2 0.4 0.6	0.2 0.4 0.6	0.2 0.4 0.6	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{T+}(Max) or V_{T-}(Min) I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{T+}(Max) or V_{T-}(Min) I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{T+}(Max) or V_{T-}(Min) I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{T+}(Max) or V_{T-}(Min) I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output Y	13	22	ns
t_{PHL}	(Figures 1 and 2)	13	22	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{PHL}		2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	20	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption (per gate):
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

SWITCHING WAVEFORMS

FIGURE 1

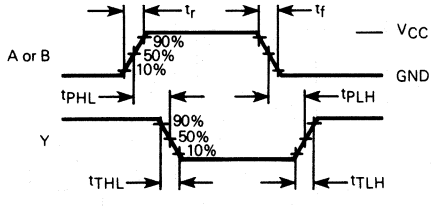

FIGURE 2 — TEST CIRCUIT

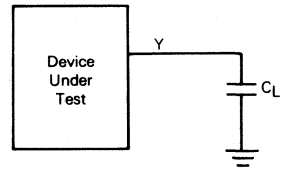

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FIGURE 3 — TYPICAL V_{T+}, V_{T-}, AND V_H VS. POWER SUPPLY VOLTAGE

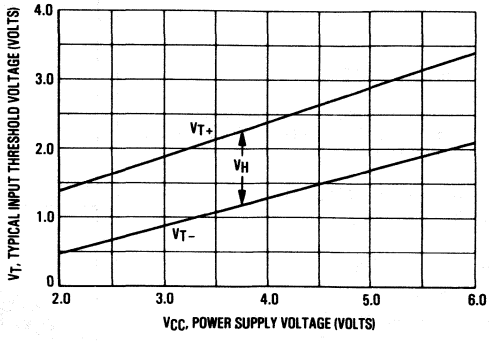
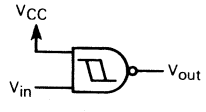
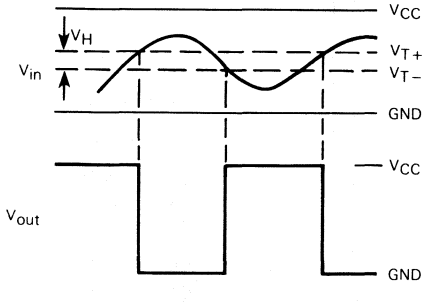


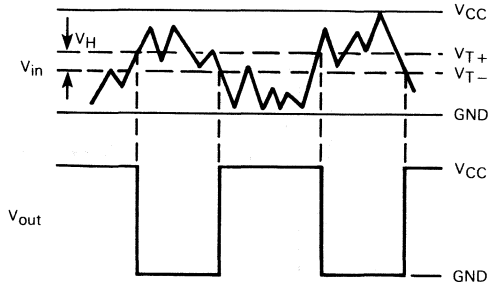
FIGURE 4 — TYPICAL SCHMITT TRIGGER APPLICATIONS



(a) A Schmitt Trigger Squares up inputs with slow rise and fall times



(b) A Schmitt trigger offers maximum noise immunity.



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MOTOROLA

MC54/74HC133

Product Preview

13-INPUT NAND GATE

The MC54/74HC133 is identical in pinout to the LS133. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
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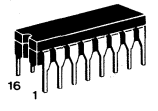
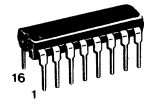
SILICON-GATE

13-INPUT NAND GATE



J SUFFIX
CERAMIC PACKAGE
CASE 620



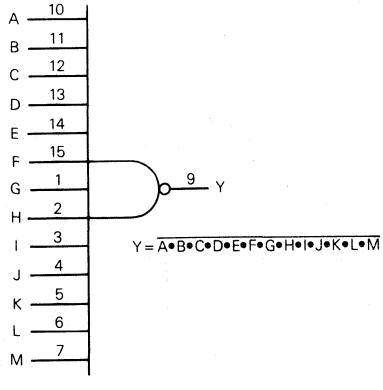
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

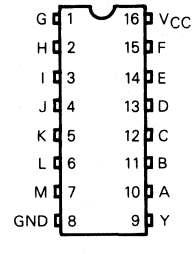
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



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This document contains information on a product under development. Motorola reserves the right to change or discontinue the product without notice.

MOTOROLA

MC54/74HC137

Advance Information

1-OF-8 DECODER/DEMULTIPLEXER, WITH ADDRESS LATCH

The MC54/74HC137 is identical in pinout to the LS137. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

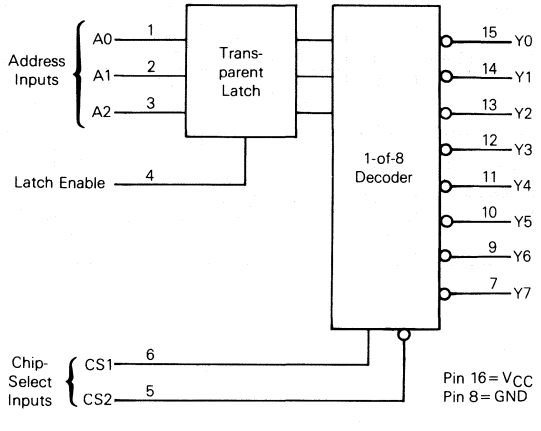
The HC137 decodes a three-bit Address to one-of-eight active-low outputs. The device has a transparent latch for storage of the Address. Two Chip Selects, one active-low and one active-high, are provided to facilitate the demultiplexing, cascading, and chip-selecting functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the other one active.

The HC137 is the inverting version of the HC237.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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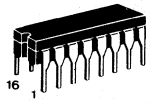
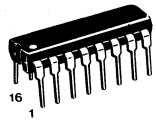
1-OF-8 DECODER/DEMULTIPLEXER, WITH ADDRESS LATCH



J SUFFIX
CERAMIC PACKAGE
CASE 620



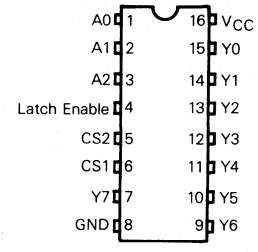
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

PIN ASSIGNMENT



TRUTH TABLE

Inputs						Outputs							
LE	CS1	CS2	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	*							

* = Depends upon the Address previously applied while LE was at a logic low.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 2)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A to Output Y	14	29	ns
t_{PHL}	(Figures 1 and 6)	20	42	
t_{PLH}	Maximum Propagation Delay, CS2 to Output Y	12	22	ns
t_{PHL}	(Figures 2 and 6)	15	34	
t_{PLH}	Maximum Propagation Delay, CS1 to Output Y	13	25	ns
t_{PHL}	(Figures 3 and 6)	17	34	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Output Y	15	30	ns
t_{PHL}	(Figures 4 and 6)	22	44	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 6)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 6)	2.0	85	170	214	253	ns
		4.5	17	34	43	51	
		6.0	14	29	36	43	
t_{PHL}		2.0	120	240	302	358	ns
		4.5	24	48	60	72	
		6.0	20	41	51	61	
t_{PLH}	Maximum Propagation Delay, CS2 to Output Y (Figures 2 and 6)	2.0	65	130	164	194	ns
		4.5	13	26	33	39	
		6.0	11	22	28	33	
t_{PHL}		2.0	98	195	246	291	ns
		4.5	20	39	49	58	
		6.0	17	33	42	49	
t_{PLH}	Maximum Propagation Delay, CS1 to Output Y (Figures 3 and 6)	2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{PHL}		2.0	98	195	246	291	ns
		4.5	20	39	49	58	
		6.0	17	33	42	49	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Output Y (Figures 4 and 6)	2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PHL}		2.0	125	250	315	373	ns
		4.5	25	50	63	75	
		6.0	21	43	54	63	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 6)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*			–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, Input A to Latch Enable (Figure 5)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Latch Enable to Input A (Figure 5)	2.0	25	50	63	75	ns
		4.5	5	10	13	15	
		6.0	4	9	11	13	
t_w	Minimum Pulse Width, Latch Enable (Figure 4)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 2)	–	1000	500	500	500	ns

PIN DESCRIPTIONS

INPUTS

A0, A1, A2 (PINS 1, 2, 3) — Address inputs. These inputs, when the chip is enabled, determine which of the eight outputs is selected.

CONTROL INPUTS

CS1, CS2 (PINS 6, 5) — Chip-Select inputs. For CS1 at a logic high and CS2 at a logic low, the chip is enabled and the outputs will follow the address inputs (Latch Enable = L). For any other combination of CS1 and CS2, the outputs will be at a logic high.

LATCH ENABLE (PIN 4) — Latch-Enable input. A logic high at this input latches the Address. A logic low at this input allows the outputs to follow the data at the Address pins (CS1 = H and CS2 = L).

OUTPUTS

Y0-Y7 — Active-low outputs. One of these eight outputs is selected when the chip is enabled (CS1 = H and CS2 = L) and the data on the A0, A1, and A2 inputs correspond to that particular output. The selected output is at a logic low while all others remain at a logic high.

SWITCHING WAVEFORMS

FIGURE 1

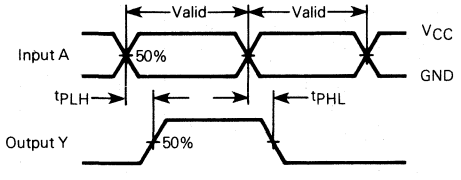


FIGURE 2

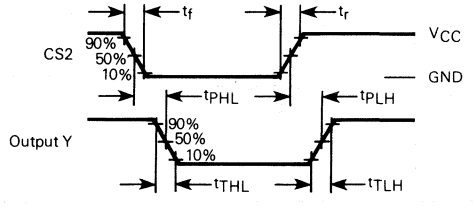


FIGURE 3

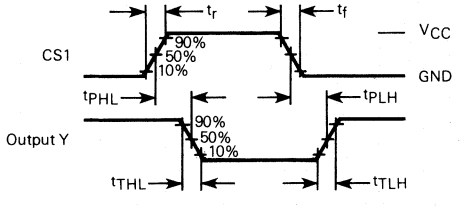


FIGURE 4

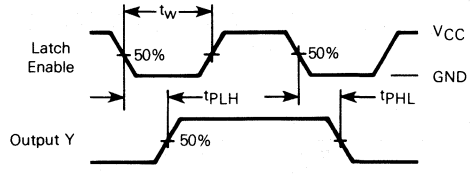


FIGURE 5

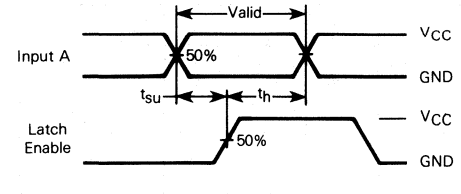
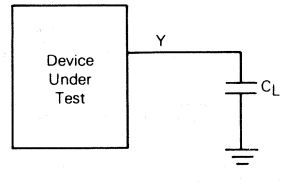
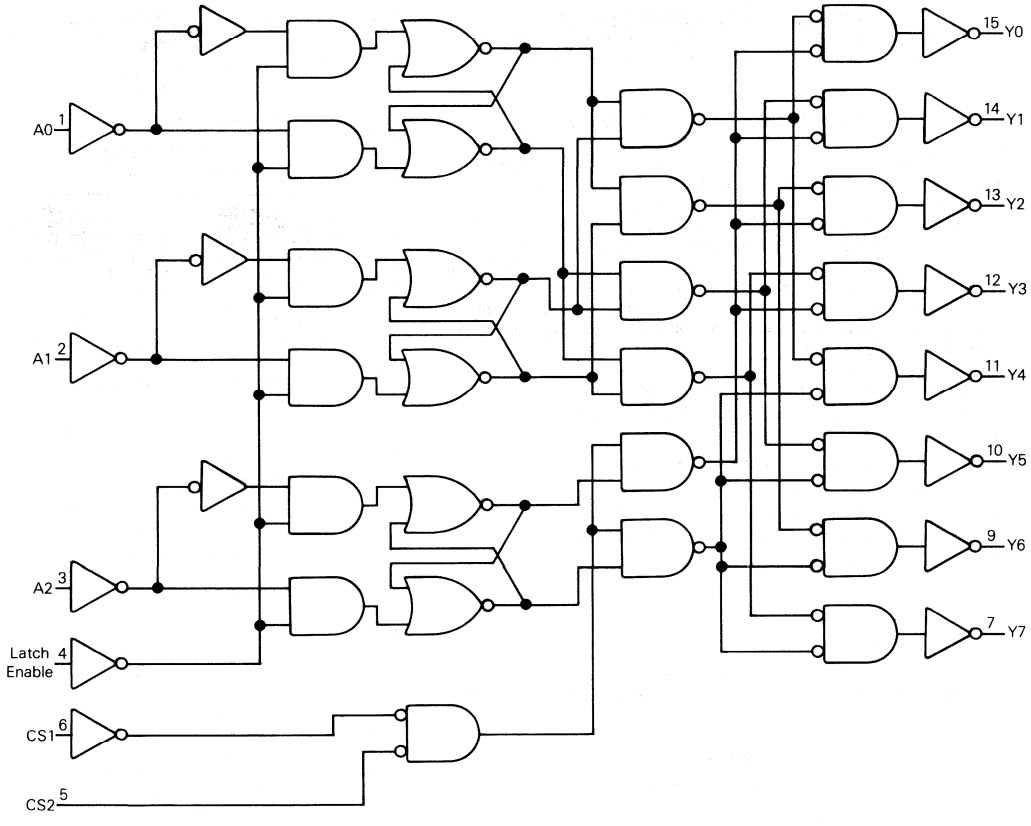


FIGURE 6 — TEST CIRCUIT



LOGIC DIAGRAM



MOTOROLA

MC54/74HC138

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

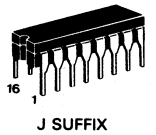
1-OF-8 DECODER/ DEMULTIPLEXER

1-OF-8 DECODER/DEMULTIPLEXER

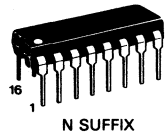
The MC54/74HC138 is identical in pinout to the LS138. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC138 decodes a three-bit Address to one-of-eight active-low outputs. This device features three chip select inputs, two active low and one active high to facilitate the demultiplexing, cascading, and chip-selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620



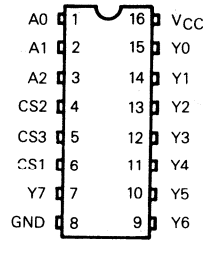
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

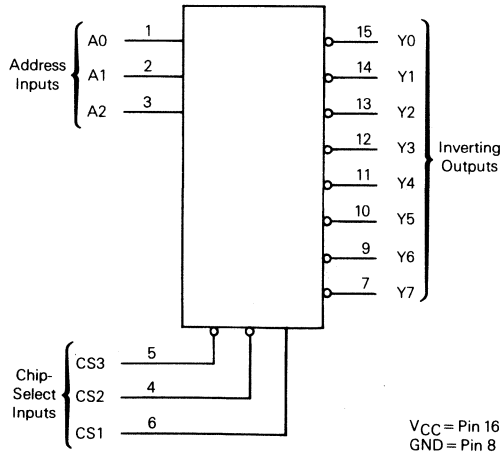
54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

PIN ASSIGNMENT



BLOCK DIAGRAM



TRUTH TABLE

Inputs						Outputs							
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level (steady state)
L = low level (steady state)
X = don't care

5

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise or Fall Time (Figure 2)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A to Output Y	13	25	ns
t_{PHL}	(Figures 1 and 4)	20	35	
t_{PLH}	Maximum Propagation Delay, CS1 to Y	13	25	ns
t_{PHL}	(Figures 2 and 4)	14	25	
t_{PLH}	Maximum Propagation Delay, CS2 and CS3 to Y	13	25	ns
t_{PHL}	(Figures 3 and 4)	17	30	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 4)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 4)	2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{PHL}		2.0	100	200	252	298	ns
		4.5	20	40	50	60	
		6.0	17	34	43	51	
t_{PLH}	Maximum Propagation Delay, CS1 to Y (Figures 2 and 4)	2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{PHL}		2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{PLH}	Maximum Propagation Delay, CS2 and CS3 to Y (Figures 3 and 4)	2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{PHL}		2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 4)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		60	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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PIN DESCRIPTIONS

INPUTS

A0, A1, A2 (PINS 1, 2, 3) – Address inputs. These inputs, when the chip is selected, determine which of the eight outputs is active-low.

Y0-Y7 (PINS 15, 14, 13, 12, 11, 10, 9, 7) – Active low Decoded outputs. These outputs assume a low level when addressed and the chip is selected. These outputs remain high when not addressed or the chip is not selected.

CONTROLS

CS1, CS2, CS3 (PINS 6, 4, 5) – Chip select inputs. For CS1 at a logic high and CS2, CS3 at a logic low, the chip is selected and the outputs will follow the Address inputs. For any other combination of CS1, CS2, and CS3, the outputs will be at a logic high.

SWITCHING WAVEFORMS

FIGURE 1

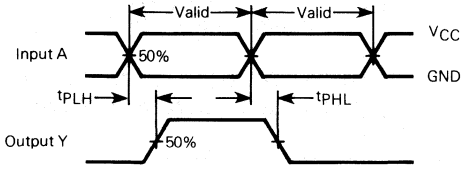


FIGURE 2

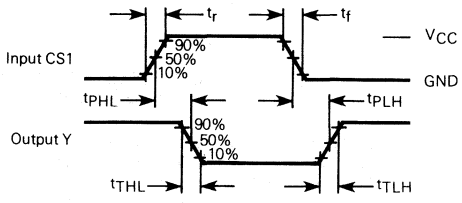


FIGURE 3

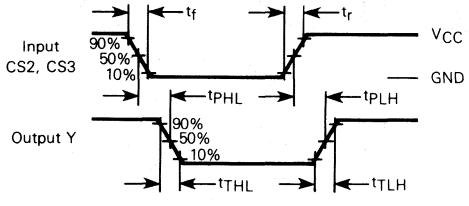
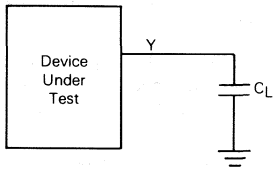
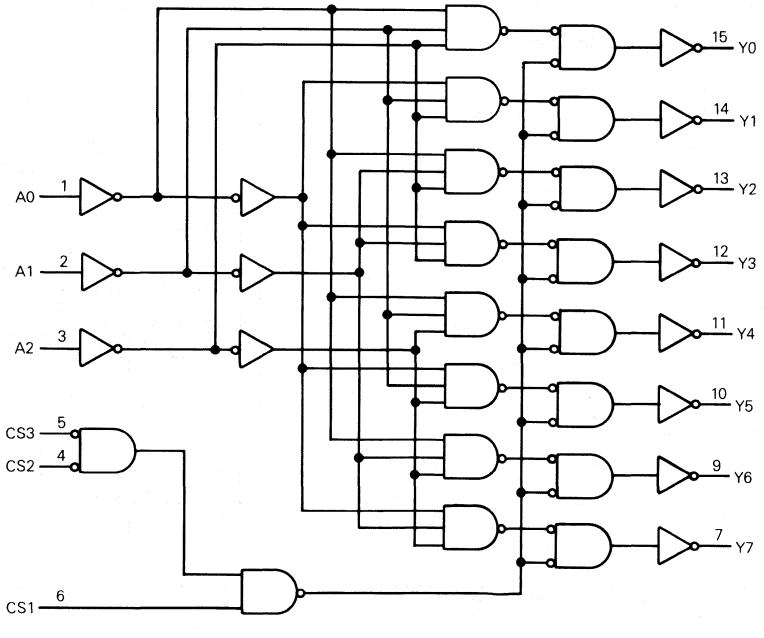


FIGURE 4 — TEST CIRCUIT



LOGIC DIAGRAM



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MOTOROLA

MC54/74HCT138

Product Preview

1-OF-8 DECODER/DEMULTIPLEXER (WITH LSTTL-COMPATIBLE INPUTS)

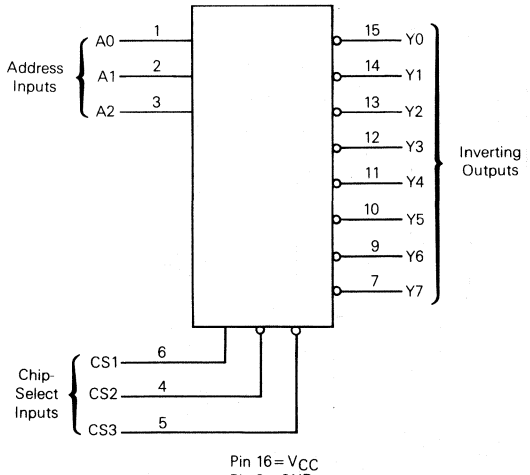
The HCT138 may be used as a level converter for interfacing LSTTL to High-Speed CMOS. The inputs of HCT devices are compatible with both LSTTL and CMOS output voltage levels.

The HCT138 is identical in pinout to the LS138.

The HCT138 selects one of eight active-low outputs, based on the data present at the Address pins. This device features three chip-select inputs, two active-low and one active-high, to facilitate the chip-select, demultiplexing, and cascading functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the others active.

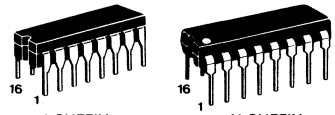
- Compatible with LSTTL Outputs — No Pullup Resistor Required
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Voltage Range: 4.5 to 5.5 Volts
- Low Quiescent Current Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM



HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

1-OF-8 DECODER/DEMULTIPLEXER (WITH LSTTL-COMPATIBLE INPUTS)



J SUFFIX
CERAMIC PACKAGE
CASE 620

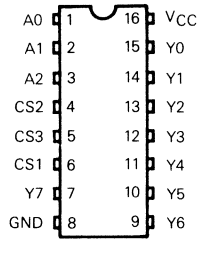
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCTXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCTXXXN (Plastic Package)
MC74HCTXXXJ (Ceramic Package)

PIN ASSIGNMENT



TRUTH TABLE

Inputs						Outputs							
Chip-Select			Address										
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

5

MOTOROLA

MC54/74HC139

Advance Information

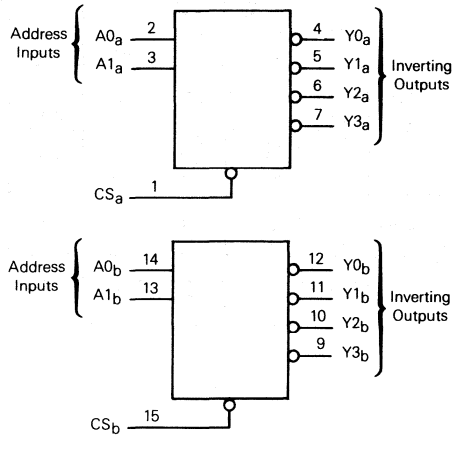
DUAL 1-OF-4 DECODER/DEMULTIPLEXER

The MC54/74HC139 is identical in pinout to the LS139. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 1-of-4 decoders, each of which decodes a two-bit address to one-of-four active-low outputs. Active-low Chip Selects are provided to facilitate the demultiplexing, cascading, and chip-selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and utilizing the Chip Select as a data input.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM

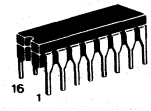


V_{CC} = Pin 16
GND = Pin 8

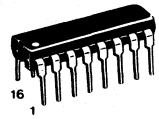
This document contains information on a new product. Specifications and information herein are subject to change without notice.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL 1-OF-4 DECODER/ DEMULTIPLEXER



J SUFFIX
CERAMIC PACKAGE
CASE 620



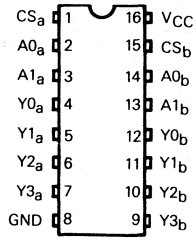
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



TRUTH TABLE

Inputs			Outputs			
CS	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X = Don't Care

5

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input CS to Output Y	19	30	ns
t_{PHL}	(Figures 1 and 3)	19	30	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y, 4 Levels of Delay	18	30	ns
t_{PHL}	(Figures 2 and 3)	18	30	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y, 5 Levels of Delay	28	38	ns
t_{PHL}	(Figures 2 and 3)	28	38	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input CS to Output Y (Figures 1 and 3)	2.0	115	175	219	254	ns
		4.5	23	35	44	51	
		6.0	19	30	38	44	
t_{PHL}		2.0	115	175	219	254	ns
		4.5	23	35	44	51	
		6.0	19	30	38	44	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y, 4 Levels of Delay (Figures 2 and 3)	2.0	110	175	219	254	ns
		4.5	22	35	44	51	
		6.0	18	30	38	44	
t_{PHL}		2.0	110	175	219	254	ns
		4.5	22	35	44	51	
		6.0	18	30	38	44	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y, 5 Levels of Delay (Figures 2 and 3)	2.0	165	220	275	320	ns
		4.5	33	44	55	64	
		6.0	28	38	47	54	
t_{PHL}		2.0	165	220	275	320	ns
		4.5	33	44	55	64	
		6.0	28	38	47	54	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	7	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (per Decoder)		75	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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PIN DESCRIPTIONS

INPUTS

$A0_a$, $A1_a$, $A0_b$, $A1_b$ (PINS 2, 3, 14, 13) – Address inputs. These inputs, when the respective 1-of-4 decoder is enabled, determine which of its four active-low outputs is selected.

OUTPUTS

$Y0_a$-$Y3_a$, $Y0_b$-$Y3_b$ (PINS 4-7, 12, 11, 10, 9) – Active-low outputs. These outputs assume a low level when addressed and the appropriate chip-select input is active. These outputs remain high when not addressed or the appropriate chip-select input is inactive.

CONTROL INPUTS

CS_a, CS_b (PINS 1, 15) – Active-low chip-select inputs. For a logic low on this input, the outputs for that particular decoder will follow the Address inputs. A logic high on this input will force all outputs to a logic high.

SWITCHING WAVEFORMS

FIGURE 1

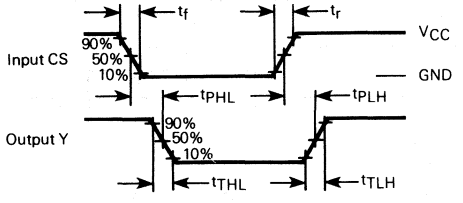


FIGURE 2

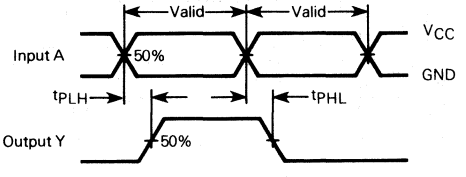
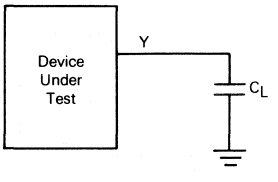
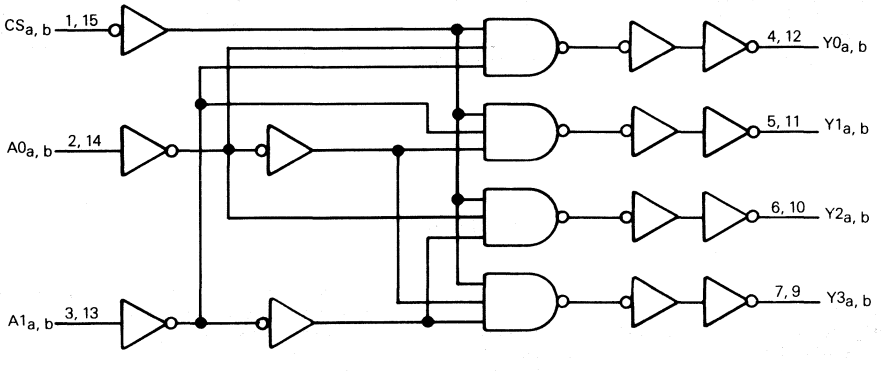


FIGURE 3 — TEST CIRCUIT



LOGIC DIAGRAM
(½ OF DEVICE)



MOTOROLA

MC54/74HC147

Product Preview

DECIMAL TO BCD PRIORITY ENCODER

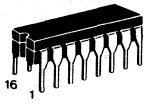
The MC54/74HC147 is identical in pinout to the LS147. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device encodes nine active-low data inputs to four active-low BCD Address Outputs, ensuring that only the highest order active data line is encoded. The implied decimal zero condition is encoded when all nine data inputs are at a high logic level (inactive).

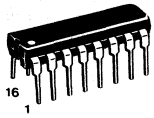
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DECIMAL TO BCD PRIORITY ENCODER



J SUFFIX
CERAMIC PACKAGE
CASE 620



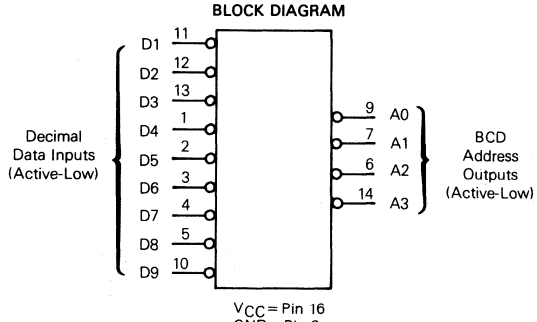
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

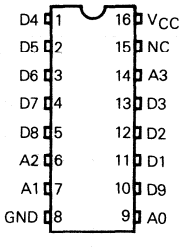
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs									Outputs			
D1	D2	D3	D4	D5	D6	D7	D8	D9	A3	A2	A1	A0
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

MC54/74HC151

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

8-INPUT DATA SELECTOR/ MULTIPLEXER

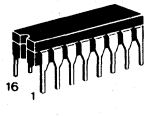
8-INPUT DATA SELECTOR/MULTIPLEXER

The MC54/74HC151 is identical in pinout to the LS151. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

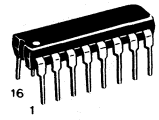
This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Output Enable pin must be at a low logic level for the selected data to appear at the outputs. If Output Enable is high, the Y output is forced to a low logic level and the $\overline{Y}$ output is forced to a high logic level.

The HC151 is similar in function to the HC251 which has 3-state outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs
- Selects One of Eight Binary Data Sources
- May Be Used In Parallel-to-Serial Conversion



J SUFFIX
CERAMIC PACKAGE
CASE 620



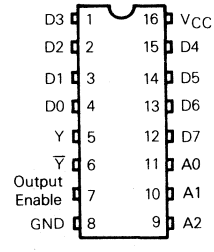
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

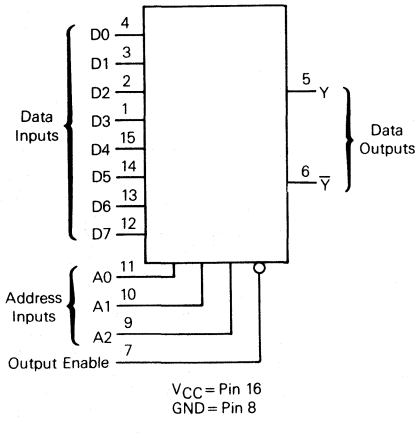
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



BLOCK DIAGRAM



FUNCTION TABLE

Inputs				Outputs	
A2	A1	A0	Output Enable	Y	$\overline{Y}$
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

D0, D1. . .D7 = the level of the respective D input

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input D to Output Y	22	29	ns
t_{PHL}	(Figures 1 and 6)	22	29	
t_{PLH}	Maximum Propagation Delay, Input D to Output $\overline{Y}$	24	32	ns
t_{PHL}	(Figures 3 and 6)	24	32	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y	26	43	ns
t_{PHL}	(Figures 2 and 6)	26	43	
t_{PLH}	Maximum Propagation Delay, Input A to Output $\overline{Y}$	27	35	ns
t_{PHL}	(Figures 2 and 6)	27	35	
t_{PLH}	Maximum Propagation Delay, Output Enable to Output Y	17	23	ns
t_{PHL}	(Figures 4 and 6)	17	23	
t_{PLH}	Maximum Propagation Delay, Output Enable to Output $\overline{Y}$	16	21	ns
t_{PHL}	(Figures 5 and 6)	16	21	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 6)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input D to Output Y	2.0	70	195	244	283	ns
	(Figures 1 and 6)	4.5	27	39	49	57	
		6.0	23	33	41	48	
t_{PHL}		2.0	70	195	244	283	ns
		4.5	27	39	49	57	
		6.0	23	33	41	48	
t_{PLH}	Maximum Propagation Delay, Input D to Output $\overline{Y}$	2.0	75	185	231	268	
	(Figures 3 and 6)	4.5	29	37	46	54	
		6.0	25	32	40	46	
t_{PHL}		2.0	75	185	231	268	ns
		4.5	29	37	46	54	
		6.0	25	32	40	46	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y	2.0	90	250	312	360	ns
	(Figures 2 and 6)	4.5	31	50	63	73	
		6.0	26	43	54	62	
t_{PHL}		2.0	90	250	312	360	ns
		4.5	31	50	63	73	
		6.0	26	43	54	62	
t_{PLH}	Maximum Propagation Delay, Input A to Output $\overline{Y}$	2.0	95	205	256	300	ns
	(Figures 2 and 6)	4.5	32	41	51	60	
		6.0	27	35	44	51	
t_{PHL}		2.0	95	205	256	300	ns
		4.5	32	41	51	60	
		6.0	27	35	44	51	
t_{PLH}	Maximum Propagation Delay, Output Enable to Output Y	2.0	50	140	175	203	ns
	(Figures 4 and 6)	4.5	21	28	35	41	
		6.0	18	24	30	35	
t_{PHL}		2.0	50	140	175	203	ns
		4.5	21	28	35	41	
		6.0	18	24	30	35	

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SWITCHING CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{PLH}	Maximum Propagation Delay, Output Enable to Output $\overline{Y}$ (Figures 5 and 6)	2.0	45	127	159	185	ns
		4.5	20	25	32	37	
		6.0	17	22	28	32	
t_{PHL}		2.0	45	127	159	185	ns
		4.5	20	25	32	37	
		6.0	17	22	28	32	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 6)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	7	13	16	19	
C_{in}	Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	110	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

PIN DESCRIPTIONS

INPUTS

D0, D1,. . ., D7 (Pins 4, 3, 2, 1, 15, 14, 13, 12) – Data inputs. Data on any one of these eight binary inputs may be selected to appear on the output.

CONTROL INPUTS

A0, A1, A2 (Pins 11, 10, 9) – Address inputs. The data on these pins are the binary address of the selected input (see the Function Table).

Output Enable (Pin 7) – Output Enable. This input pin must be at a low logic level for the selected data to appear at the outputs. If the Output Enable pin is high, the Y output is forced to a low logic level and the $\overline{Y}$ output is forced to a high logic level.

OUTPUTS

Y, $\overline{Y}$ (Pins 5, 6) – Data outputs. The selected data is presented at these pins in both true (Y output) and complemented ($\overline{Y}$ output) forms.

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SWITCHING WAVEFORMS

FIGURE 1

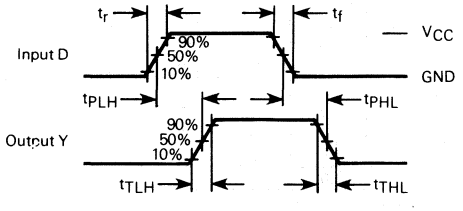


FIGURE 2

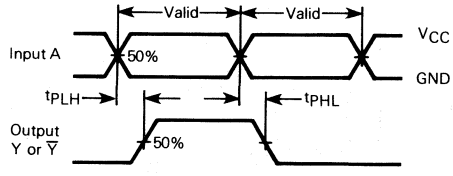


FIGURE 3

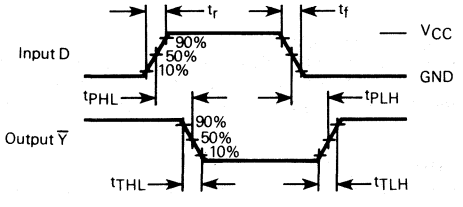


FIGURE 4

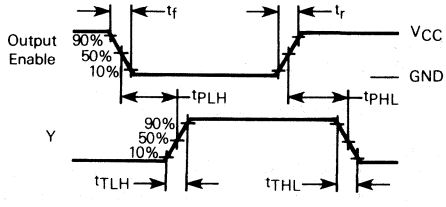


FIGURE 5

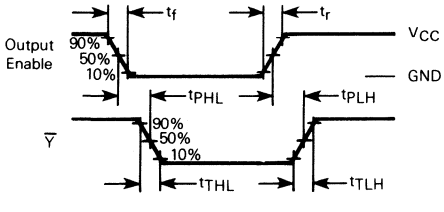
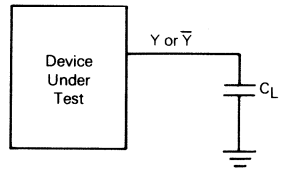
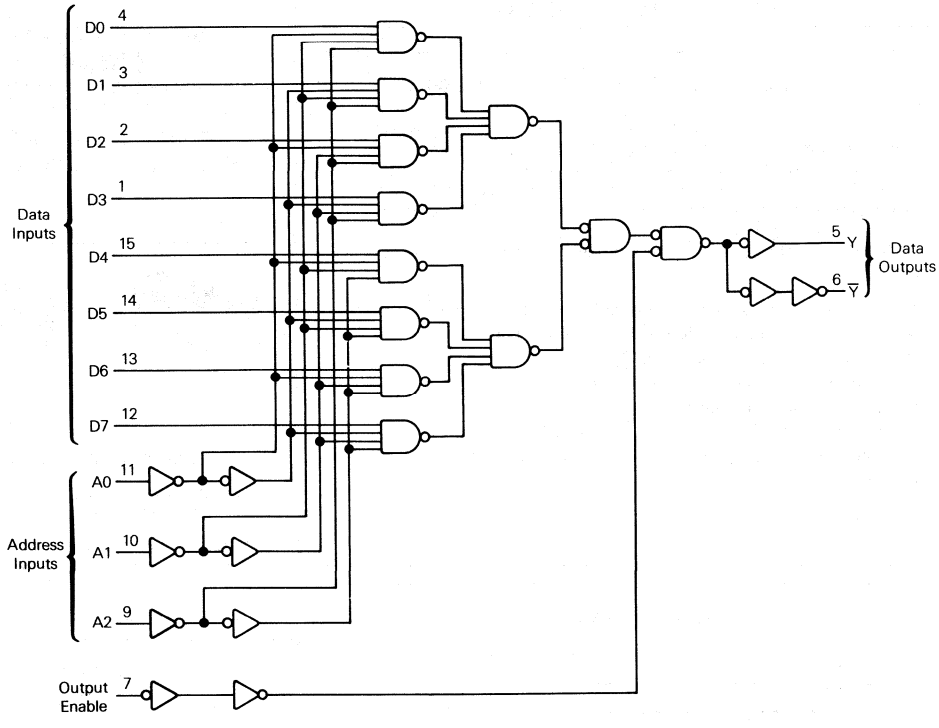


FIGURE 6 — TEST CIRCUIT



5

LOGIC DIAGRAM



MOTOROLA

MC54/74HC153

Advance Information

DUAL 4-INPUT DATA SELECTOR/MULTIPLEXER

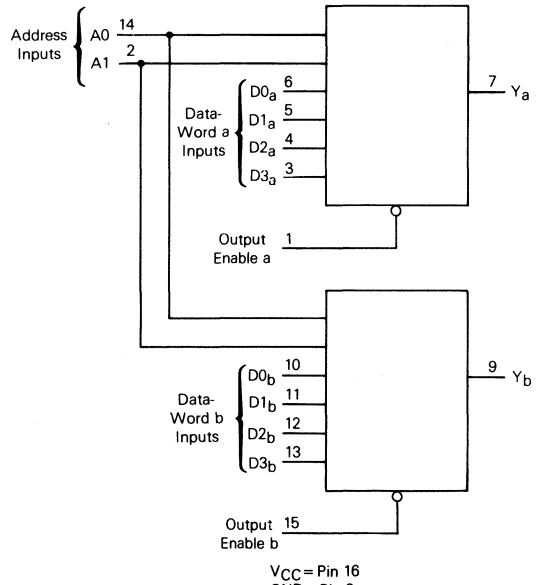
The MC54/74HC153 is identical in pinout to the LS153. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The Address Inputs select one of four Data Inputs from each multiplexer. Each multiplexer has an active low Output Enable control and a noninverting output.

The HC153 is similar in function to the HC253 which has 3-state outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

HIGH-PERFORMANCE
CMOS
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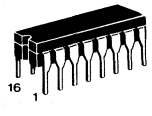
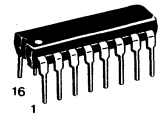
DUAL 4-INPUT DATA
SELECTOR/MULTIPLEXER



J SUFFIX
CERAMIC PACKAGE
CASE 620



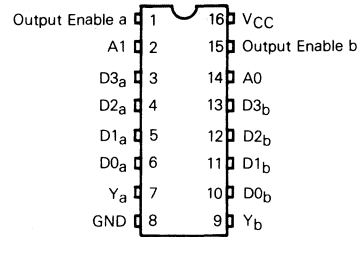
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
A1	A0	Output Enable	Y
X	X	H	L
L	L	L	D0
L	H	L	D1
H	L	L	D2
H	H	L	D3

D0, D1, D2, and D3 = the level of the respective Data Input

5

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

5

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input D to Output Y (Figures 1 and 4)	13	23	ns
t_{PHL}		13	23	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 4)	16	30	ns
t_{PHL}		16	30	
t_{PLH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 4)	8	15	ns
t_{PHL}		8	15	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input D to Output Y (Figures 1 and 4)	2.0	98	126	158	189	ns
		4.5	20	28	35	42	
		6.0	18	23	29	35	
t_{PHL}		2.0	98	126	158	189	ns
		4.5	20	28	35	42	
		6.0	18	23	29	35	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 4)	2.0	130	158	198	237	ns
		4.5	28	35	44	52	
		6.0	24	30	38	45	
t_{PHL}		2.0	130	158	198	237	ns
		4.5	28	35	44	52	
		6.0	24	30	38	45	
t_{PLH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 4)	2.0	48	95	120	142	ns
		4.5	10	19	24	28	
		6.0	8	16	20	24	
t_{PHL}		2.0	48	95	120	142	ns
		4.5	10	19	24	28	
		6.0	8	16	20	24	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		90	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

5

PIN DESCRIPTIONS

DATA INPUTS

$D0_a$-$D3_a$, $D0_b$-$D3_b$ (PINS 3, 4, 5, 6, 10, 11, 12, 13) – Data Inputs. With the outputs enabled, the addressed Data Inputs appear at the Y outputs.

CONTROL INPUTS

A0, A1 (PINS 2, 14) – Address Inputs. These inputs address the pair of Data Inputs which appear at the corresponding outputs.

OUTPUT ENABLE (PINS 1, 15) – Active-Low Output Enables. A low logic level applied to these pins enables the corresponding outputs.

OUTPUTS

Y_a, Y_b (PINS 7, 9) – Noninverting data outputs.

SWITCHING WAVEFORMS AND TEST CIRCUIT

FIGURE 1

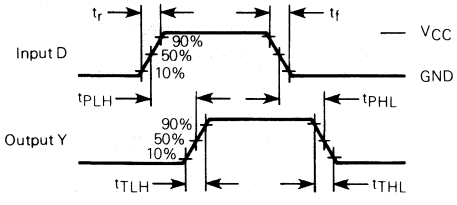


FIGURE 2

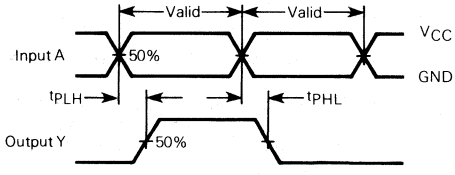


FIGURE 3

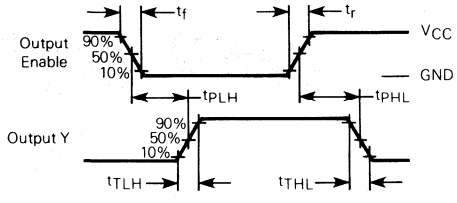
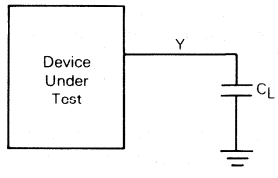
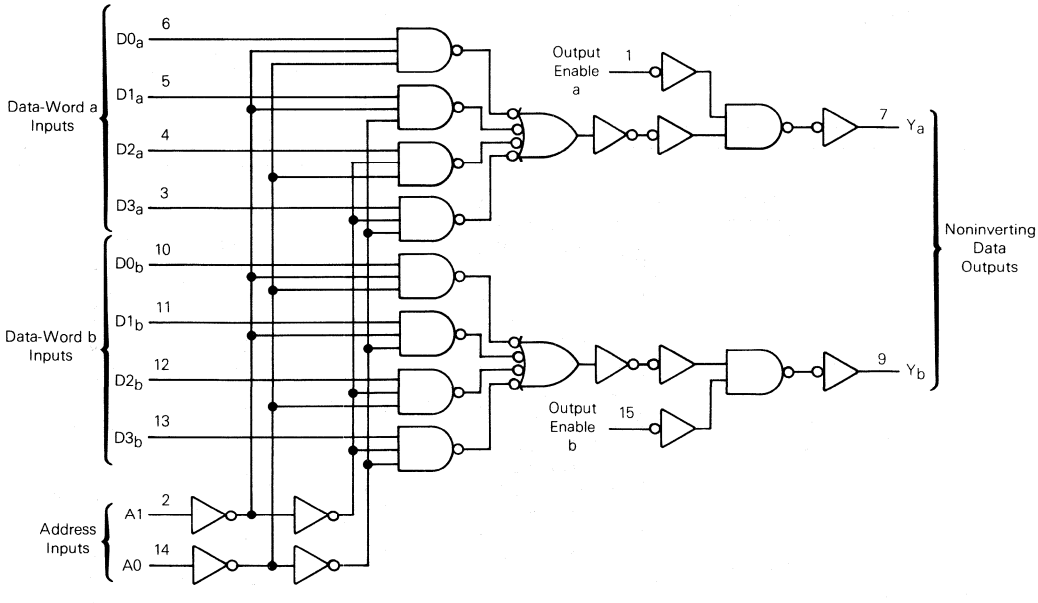


FIGURE 4 — TEST CIRCUIT



LOGIC DIAGRAM



5

MOTOROLA

MC54/74HC154

Product Preview

1-OF-16 DECODER/DEMULTIPLEXER

The MC54/74HC154 is identical in pinout to the LS154, but is in a narrow 300-mil, 24-pin DIP. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device, when enabled, selects one of 16 active-low outputs. Two active-low Chip Selects are provided to facilitate the chip-select, demultiplexing, and cascading functions. When either Chip Select is high, all outputs are high. The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the other one low.

The HC154 is primarily used for memory address decoding and data routing applications.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
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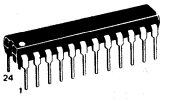
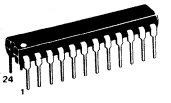
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

1-OF-16
DECODER/DEMULTIPLEXER



J SUFFIX
CERAMIC PACKAGE
CASE 758



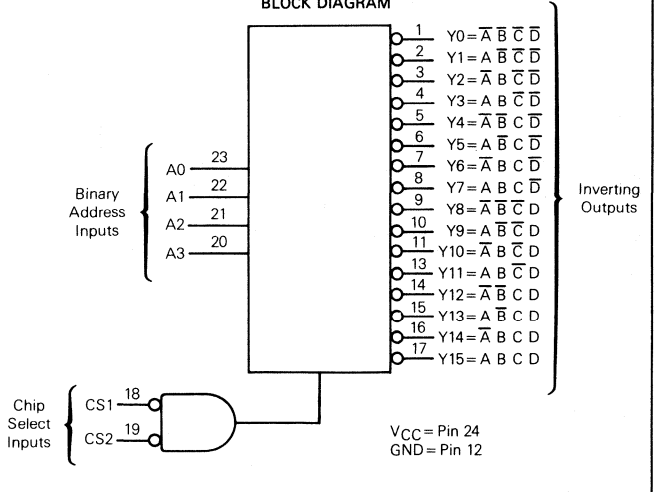
N SUFFIX
PLASTIC PACKAGE
CASE 724

ORDERING INFORMATION

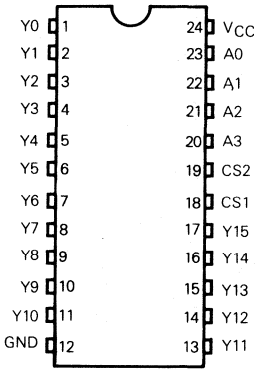
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



MOTOROLA

MC54/74HC157
MC54/74HC158

Advance Information

QUAD 2-INPUT DATA SELECTORS/MULTIPLEXERS

The MC54/74HC157 and HC158 are identical in pinout to the LS157 and LS158. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

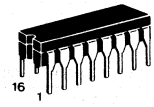
These devices select a 4-bit word from either the A or B inputs, determined by the Select input, and route it to the outputs. The data is presented at the outputs in noninverted form for the HC157 and inverted form for the HC158. A logic one on the Output Enable input will set all four Y outputs to a logic zero for the HC157 and to a logic one for the HC158.

The HC157 and HC158 are similar in function to the HC257 which has 3-state outputs.

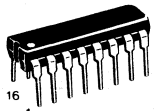
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD 2-INPUT DATA SELECTORS/ MULTIPLEXERS



J SUFFIX
CERAMIC PACKAGE
CASE 620



N SUFFIX
PLASTIC PACKAGE
CASE 648

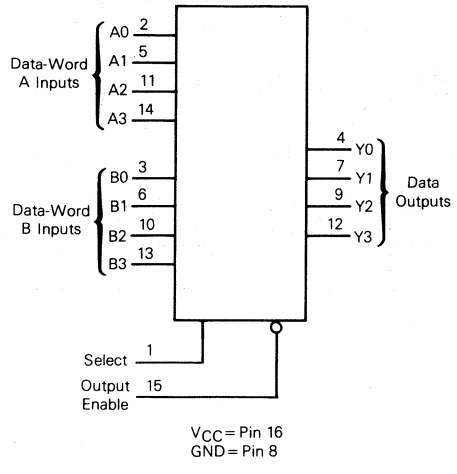
ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

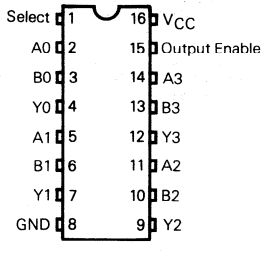
BLOCK DIAGRAM

MC54/74HC157 – Noninverting Outputs
MC54/74HC158 – Inverting Outputs



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs Y0-Y3	
Output Enable	Select	HC157	HC158
H	X	L	H
L	L	A0-A3	$\overline{A0}$-$\overline{A3}$
L	H	B0-B3	$\overline{B0}$-$\overline{B3}$

X = don't care
A0-A3, B0-B3 = the levels of the respective Data-Word Inputs.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

5

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Data to Output Y		20	ns
t_{PHL}	(Figures 1, 2, and 7)		20	
t_{PLH}	Maximum Propagation Delay, Select to Output Y		20	ns
t_{PHL}	(Figures 3, 4, and 7)		20	
t_{PLH}	Maximum Propagation Delay, Output Enable to Output Y		18	ns
t_{PHL}	(Figures 5, 6, and 7)		18	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1, 2, and 7)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Data to Output Y (Figures 1, 2, and 7)	2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{PHL}		2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{PLH}	Maximum Propagation Delay, Select to Output Y (Figures 3, 4, and 7)	2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{PHL}		2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{PLH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 5, 6, and 7)	2.0	58	115	145	171	ns
		4.5	12	23	29	34	
		6.0	10	20	25	29	
t_{PHL}		2.0	58	115	145	171	ns
		4.5	12	23	29	34	
		6.0	10	20	25	29	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1, 2, and 7)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		20	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

PIN DESCRIPTIONS

INPUTS

A0, A1, A2, A3 (PINS 2, 5, 11, 14) – Data-Word A inputs. The logic data present on these pins is transferred to the outputs when the Select input is at a logic low and the Output Enable input is at a logic low. The data is presented to the outputs in noninverted form for the HC157 and inverted form for the HC158.

B0, B1, B2, B3 (PINS 3, 6, 10, 13) – Data-Word B inputs. The logic data present on these pins is transferred to the outputs when the Select input is at a logic high and the Output Enable input is at a logic low. The data is presented to the outputs in noninverted form for the HC157 and inverted form for the HC158.

OUTPUTS

Y0, Y1, Y2, Y3 (PINS 4, 7, 9, 12) – Data outputs. The selected input data word is presented at these outputs when the Output Enable input is at a logic low. The data present on these pins is in its noninverted form for the HC157 and inverted form for the HC158. For the Output Enable input at a logic high, the outputs are at a logic low for the HC157 and at a logic high for the HC158.

CONTROL INPUTS

SELECT (PIN 1) – Data-word select. This input determines the data word to be transferred to the outputs. A logic low on this input selects the A inputs and a logic high selects the B inputs.

OUTPUT ENABLE (PIN 15) – Output Enable input. A logic low on this input allows the selected input data to be presented at the outputs. A logic high on this input sets all outputs to a logic low for the HC157 and to a logic high for the HC158.

SWITCHING WAVEFORMS

FIGURE 1 — HC157

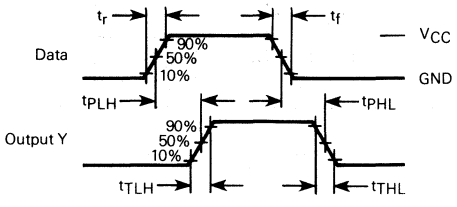


FIGURE 2 — HC158

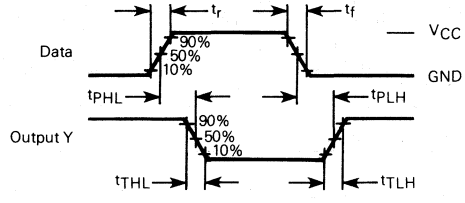


FIGURE 3 — Y vs SELECT, NON-INVERTED

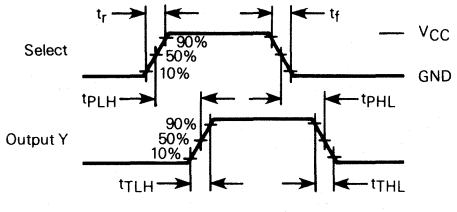


FIGURE 4 — Y vs SELECT, INVERTED

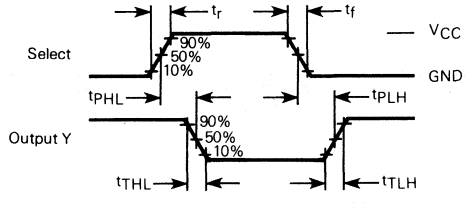


FIGURE 5 — HC157

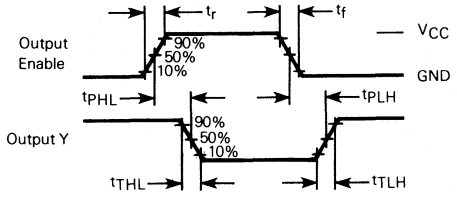


FIGURE 6 — HC158

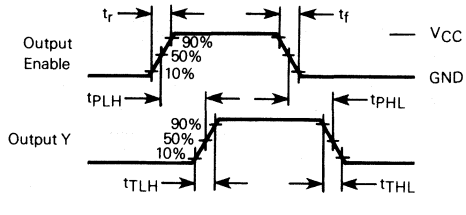
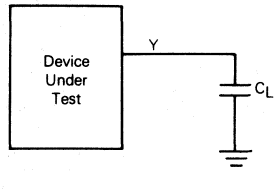
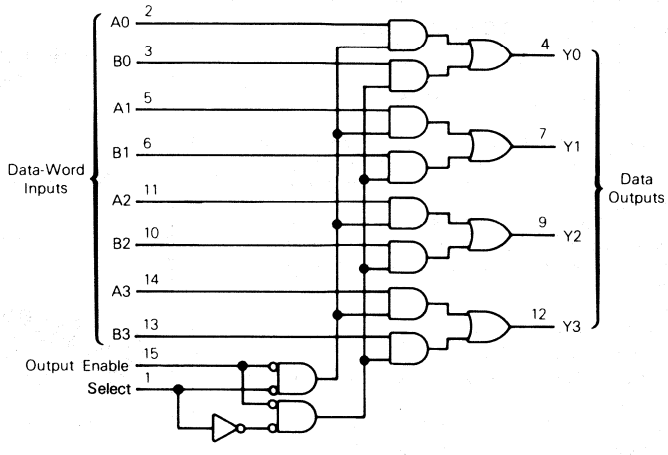


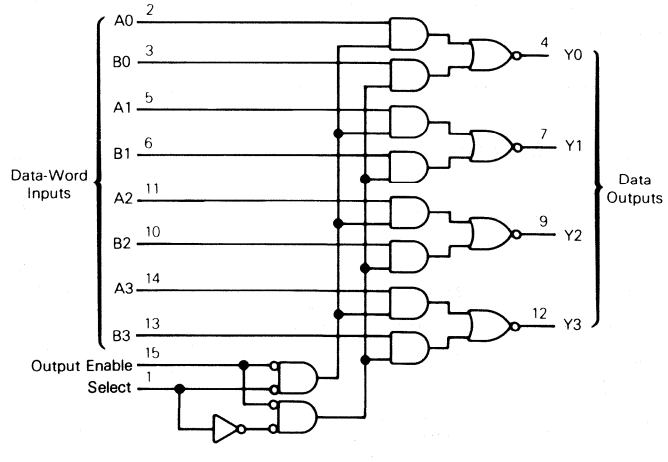
FIGURE 7 — TEST CIRCUIT



LOGIC DIAGRAMS



HC157



HC158

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MOTOROLA

MC54/74HC160
MC54/74HC161
MC54/74HC162
MC54/74HC163

Advance Information

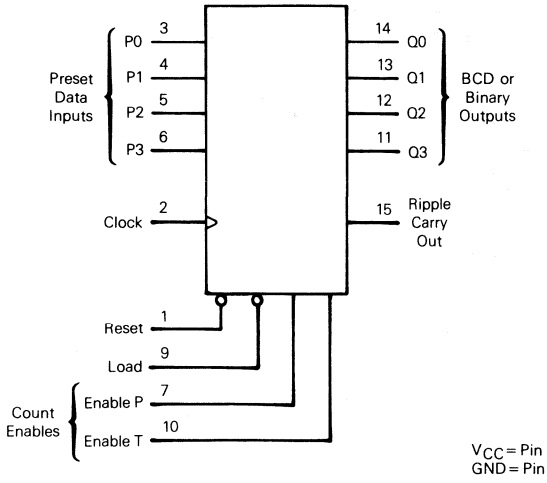
PRESETTABLE COUNTERS

The MC54/74HC160 through HC163 are identical in pinout to the LS160 through LS163, respectively. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC160 and HC162 are programmable BCD counters with asynchronous and synchronous Reset inputs, respectively. The HC161 and HC163 are programmable 4-bit binary counters with asynchronous and synchronous Reset, respectively.

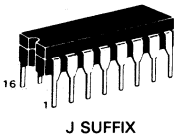
- Synchronous or Asynchronous Reset
- Synchronous Counting and Loading
- Two Count-Enable Inputs for High-Speed Synchronous Cascading
- Rising-Edge-Triggered Operation
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM

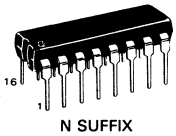


HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

PRESETTABLE COUNTERS



J SUFFIX
CERAMIC PACKAGE
CASE 620



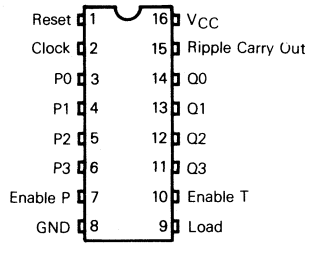
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



Device	Count Mode	Reset Mode
HC160	BCD	Asynchronous
HC161	Binary	Asynchronous
HC162	BCD	Synchronous
HC163	Binary	Synchronous

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)**	43	30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q	21	28	ns
t_{PHL}	(Figures 1 and 7)	29	34	
t_{PHL}	Maximum Propagation Delay, Reset to Q (HC160 and HC161 only) (Figure 2 and 7)	27	36	ns
t_{PLH}	Maximum Propagation Delay, Enable T to Ripple Carry Out	15	26	ns
t_{PHL}	(Figures 3 and 7)	18	32	
t_{PLH}	Maximum Propagation Delay, Clock to Ripple Carry Out	20	30	ns
t_{PHL}	(Figures 1 and 7)	24	36	
t_{PHL}	Maximum Propagation Delay, Reset to Ripple Carry Out (HC160 and HC161 only) (Figures 2 and 7)	29	38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 7)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)**	2.0	14	5	4	4	MHz
		4.5	40	27	21	18	
		6.0	44	32	25	21	
t_{PLH}	Maximum Propagation Delay, Clock to Q (Figures 1 and 7)	2.0	85	170	214	253	ns
		4.5	17	34	43	51	
		6.0	14	29	36	43	
t_{PHL}		2.0	103	205	258	305	ns
		4.5	21	41	52	61	
		6.0	17	35	44	52	
t_{PHL}	Maximum Propagation Delay, Reset to Q (HC160 and HC161 only) (Figures 2 and 7)	2.0	105	210	265	313	ns
		4.5	21	42	53	63	
		6.0	18	36	45	53	
t_{PLH}	Maximum Propagation Delay, Enable T to Ripple Carry Out (Figures 3 and 7)	2.0	80	160	202	238	ns
		4.5	16	32	40	48	
		6.0	14	27	34	41	
t_{PHL}		2.0	98	195	246	291	ns
		4.5	20	39	49	58	
		6.0	17	33	42	49	
t_{PLH}	Maximum Propagation Delay, Clock to Ripple Carry Out (Figures 1 and 7)	2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PHL}		2.0	108	215	271	320	ns
		4.5	22	43	54	64	
		6.0	18	37	46	54	
t_{PHL}	Maximum Propagation Delay, Reset to Ripple Carry Out (HC160 and HC161 only) (Figures 2 and 7)	2.0	110	220	277	328	ns
		4.5	22	44	55	66	
		6.0	19	37	47	55	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 7)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		57	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

** Applies to noncascaded configuration, only. With cascaded counters, (1) Clock to Ripple Carry Out Propagation Delays, (2) Enable T or Enable P to Clock Setup Times, and (3) Clock to Enable T or Enable P Hold Times determine f_{max}.

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{su}	Minimum Setup Time, Preset Data Inputs to Clock (Figure 5)	2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{su}	Minimum Setup Time, Load to Clock (Figure 5)	2.0	68	135	170	201	ns
		4.5	14	27	34	40	
		6.0	11	23	29	34	
t_{su}	Minimum Setup Time, Reset to Clock (HC162 and HC163 only) (Figure 4)	2.0	80	160	202	238	ns
		4.5	16	32	40	48	
		6.0	14	27	34	41	
t_{su}	Minimum Setup Time, Enable T or Enable P to Clock (Figure 6)	2.0	100	200	250	300	ns
		4.5	20	40	50	60	
		6.0	17	34	43	51	
t_h	Minimum Hold Time, Clock to Preset Data Inputs (Figure 5)	2.0	25	50	63	75	ns
		4.5	5	10	13	15	
		6.0	4	9	11	13	
t_h	Minimum Hold Time, Clock to Load (Figure 5)	2.0	−35	0	0	0	ns
		4.5	−7	0	0	0	
		6.0	−5	0	0	0	
t_h	Minimum Hold Time, Clock to Reset (HC162 and HC163 only) (Figure 4)	2.0	−40	0	0	0	ns
		4.5	−8	0	0	0	
		6.0	−6	0	0	0	
t_h	Minimum Hold Time, Clock to Enable T or Enable P (Figure 6)	2.0	−50	0	0	0	ns
		4.5	−10	0	0	0	
		6.0	−8	0	0	0	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{rec}	Minimum Recovery Time, Load Inactive to Clock (Figure 5)	2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Reset (HC160 and HC161 only) (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

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FUNCTION TABLE

Inputs					Outputs
Clock	Reset*	Load	Enable P	Enable T	Q
↑	L	X	X	X	Reset
↑	H	L	X	X	Load Preset Data
↑	H	H	H	H	Count
↑	H	H	L	X	No Count
↑	H	H	X	L	No Count

*HC162 and HC163 only. HC160 and HC161 are Asynchronous-Reset Devices

H = high level
L = low level
X = don't care

FUNCTION DESCRIPTION

The HC160/161/162/163 are programmable 4-bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading, and count-enable controls.

The HC160 and HC162 are BCD counters with asynchronous Reset, and synchronous Reset, respectively. The HC161 and HC163 are binary counters with asynchronous Reset and synchronous Reset, respectively.

INPUTS

Clock (Pin 2) — The internal flip-flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as Resetting (HC162 and HC163) and loading occur with the rising edge of the Clock input.

Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6) — These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip-flops and appear at the counter outputs. P0 (pin 3) is the least-significant bit and P3 (pin 6) is the most-significant bit.

OUTPUTS

Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11) — These are the counter outputs (BCD or binary). Q0 (pin 14) is the least-significant bit and Q3 (pin 11) is the most-significant bit.

Ripple Carry Out (Pin 15) — When the counter is in its maximum state (1001 for the BCD counters or 1111 for the binary counters), this output goes high, providing an external look-ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equations for this output are:

$$\text{Ripple Carry Out} = \text{Enable T} \bullet Q0 \bullet \overline{Q1} \bullet \overline{Q2} \bullet Q3$$
for BCD counters HC160 and HC162

$$\text{Ripple Carry Out} = \text{Enable T} \bullet Q0 \bullet Q1 \bullet Q2 \bullet Q3$$
for binary counters HC161 and HC163

CONTROL FUNCTIONS

Resetting — A logic zero on the Reset pin (pin 1) resets the internal flip-flops and sets the outputs (Q0 through Q3) to logic zero. The HC160 and HC161 reset asynchronously, and the HC162 and HC163 reset with the rising edge of the Clock input (synchronous reset).

Loading — With the rising edge of the Clock, a logic zero on Load (pin 9) loads the data from the Preset Data Input pins (P0, P1, P2, P3) into the internal flip-flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

Although the HC160 and HC162 are BCD counters, they may be programmed to any state. If they are loaded with a state disallowed in BCD code, they will return to their normal count sequence within two clock pulses (see the Output State Diagram).

Count Enable/Disable — These devices have two count-enable control pins: Enable P (pin 7) and Enable T (pin 10). The devices will count when these two pins and the Load pin are high. The logic equation is:

$$\text{Count Enable} = \text{Enable P} \bullet \text{Enable T} \bullet \text{Load}$$

The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count-enable control; Enable T is both a count-enable and a Ripple-Carry Output control.

TABLE 1. COUNT ENABLE/DISABLE

Control Inputs			Result at Outputs	
Load	Enable P	Enable T	Q0-Q3	Ripple Carry Out
H	H	H	Count	High when Q0-Q3 are maximum*
L	H	H	No Count	
X	L	H	No Count	High when Q0—Q3 are maximum*
X	X	L	No Count	L

*Q0 through Q3 are maximum for the HC160 and HC162 when Q3 Q2 Q1 Q0 = 1001.
Q0 through Q3 are maximum for the HC161 and HC163 when Q3 Q2 Q1 Q0 = 1111.

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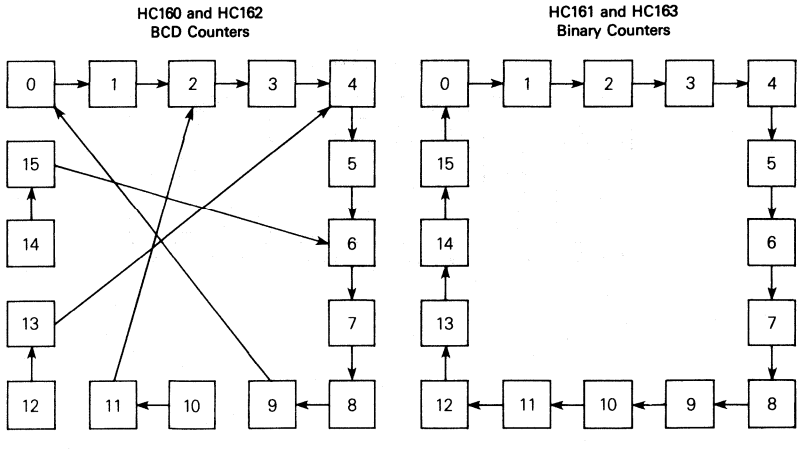
OUTPUT STATE DIAGRAM



SWITCHING WAVEFORMS

FIGURE 1

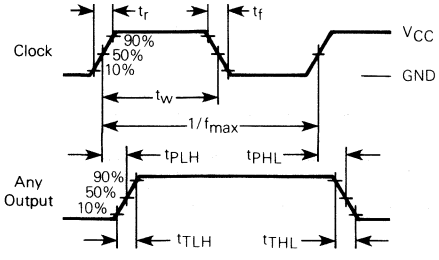


FIGURE 2

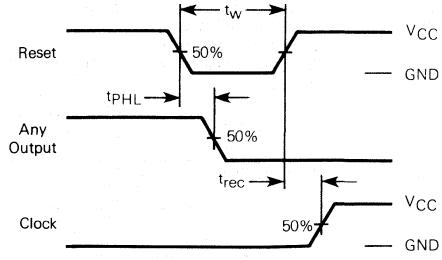


FIGURE 3

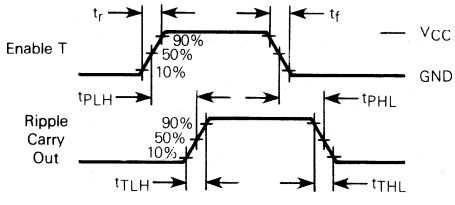


FIGURE 4

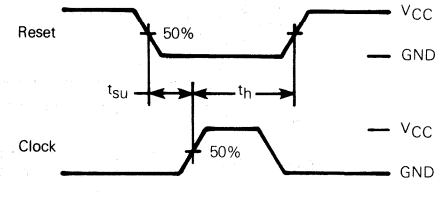


FIGURE 5

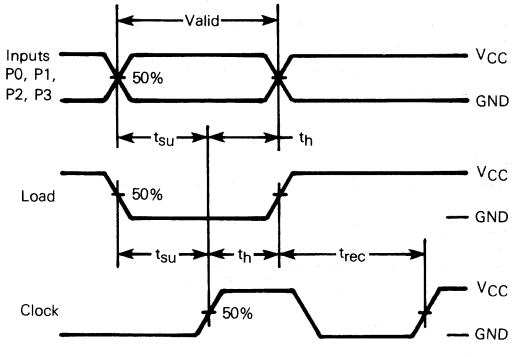


FIGURE 6

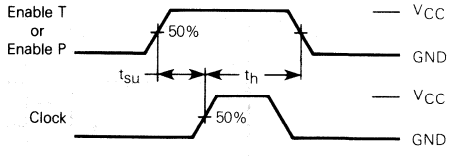
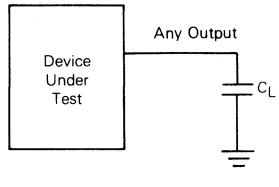


FIGURE 7 — TEST CIRCUIT



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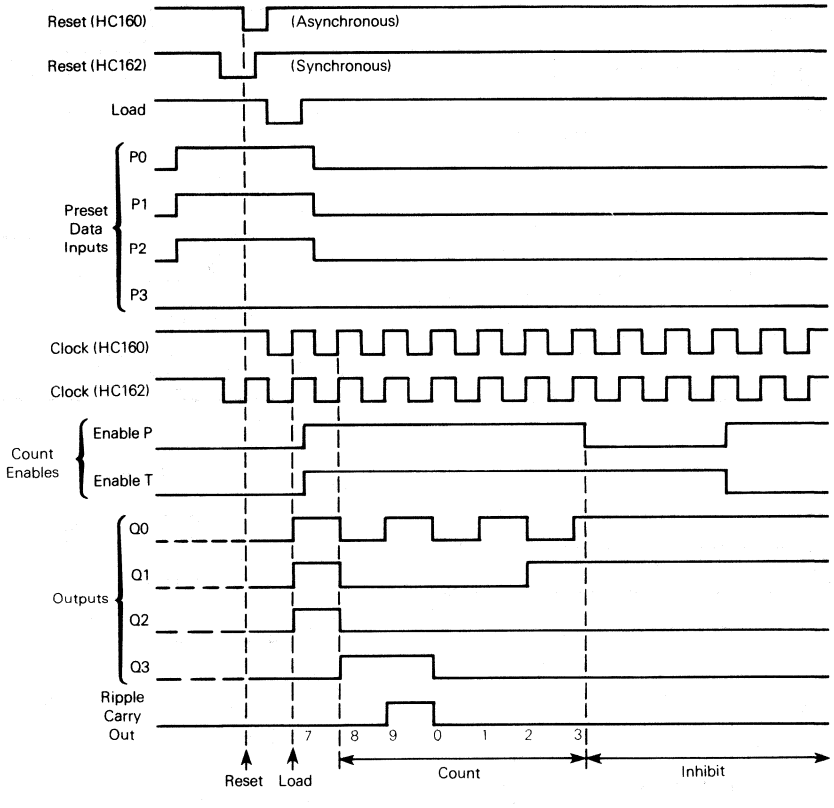
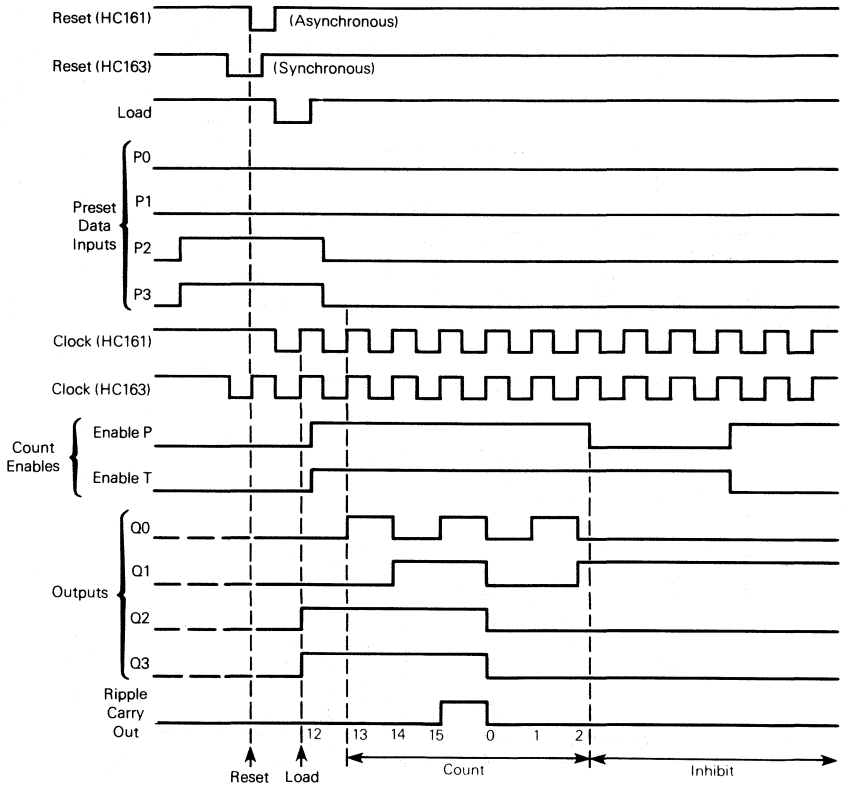
HC160, HC162 TIMING DIAGRAM

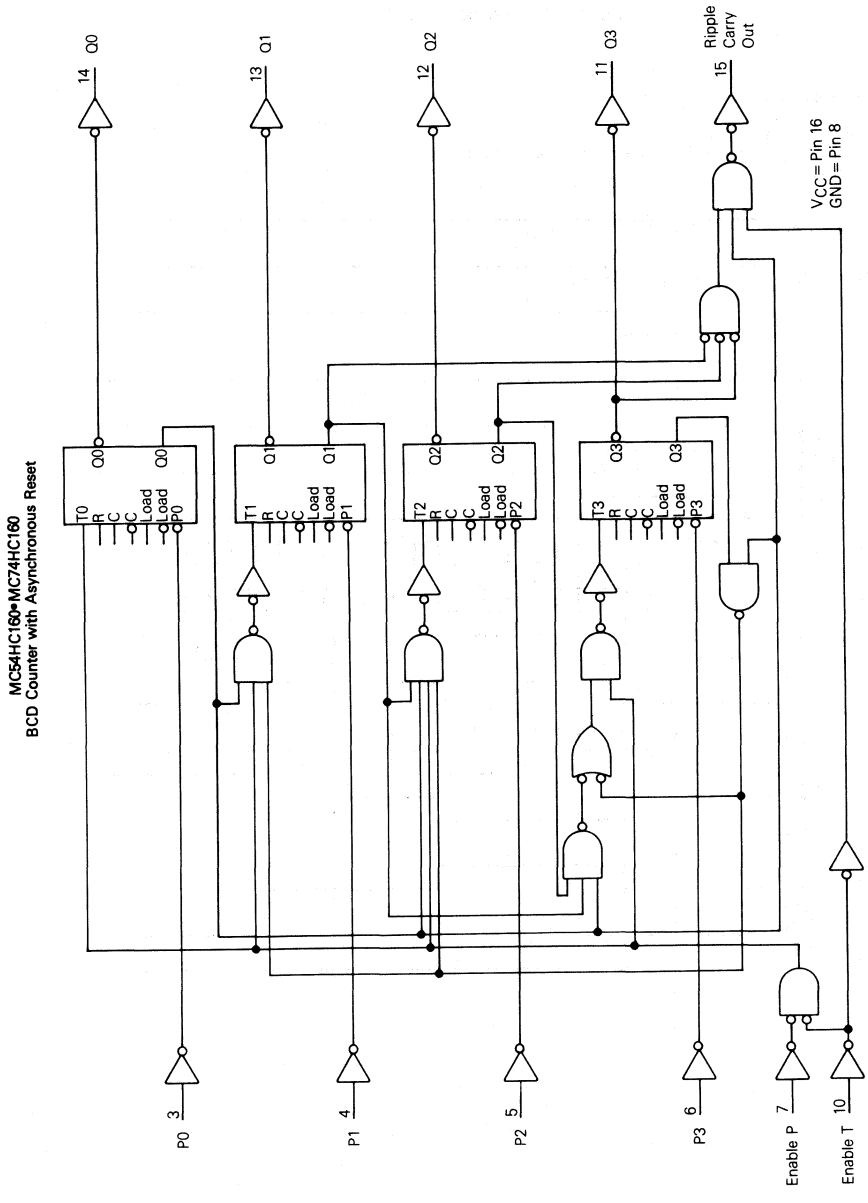
Sequence illustrated in waveforms:
1. Reset outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit.



HC161, HC163 TIMING DIAGRAM

Sequence illustrated in waveforms:
1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

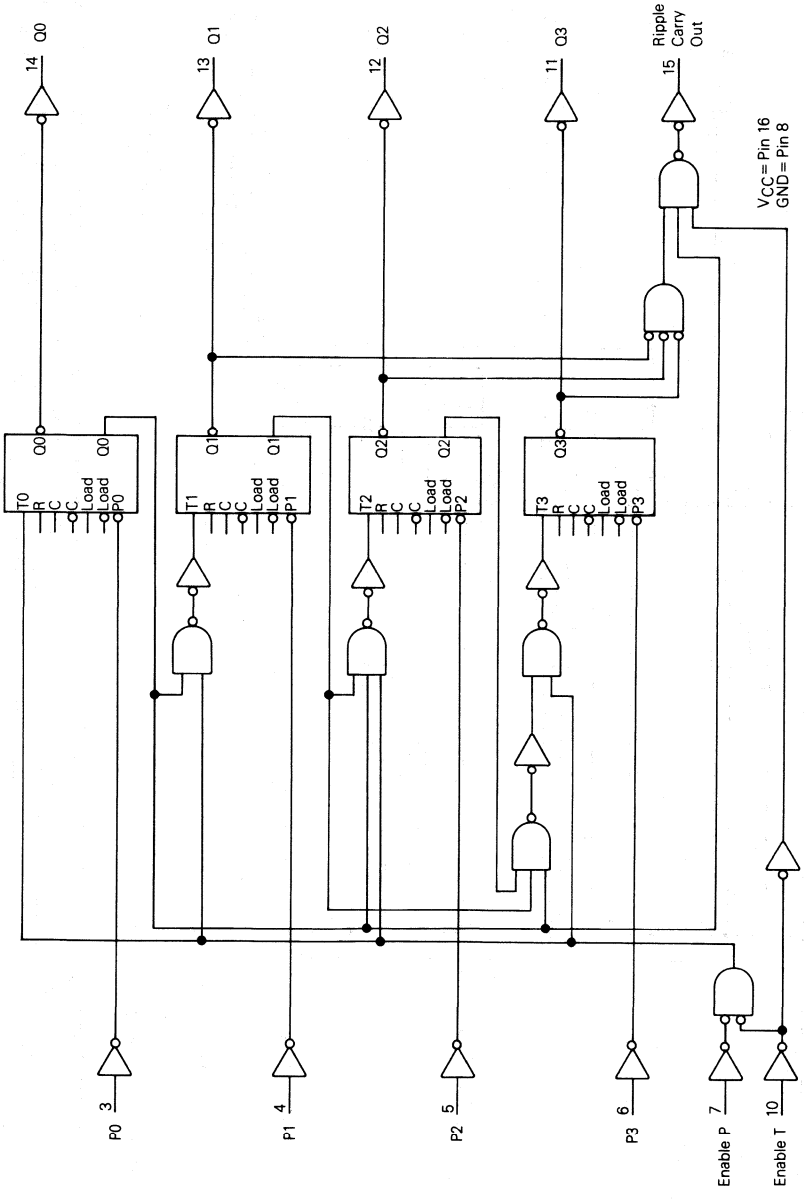




The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

MC54HC161•MC74HC161
4-Bit Binary Counter with Asynchronous Reset



The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

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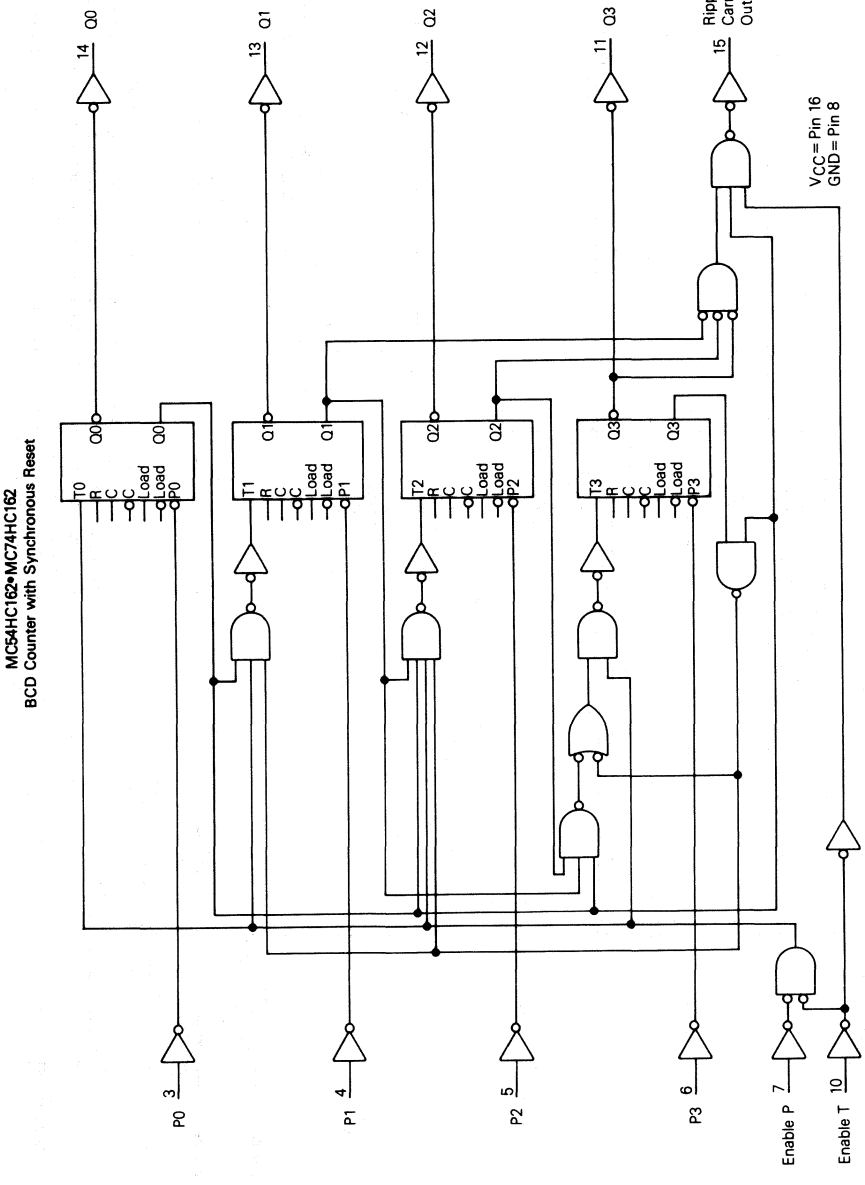
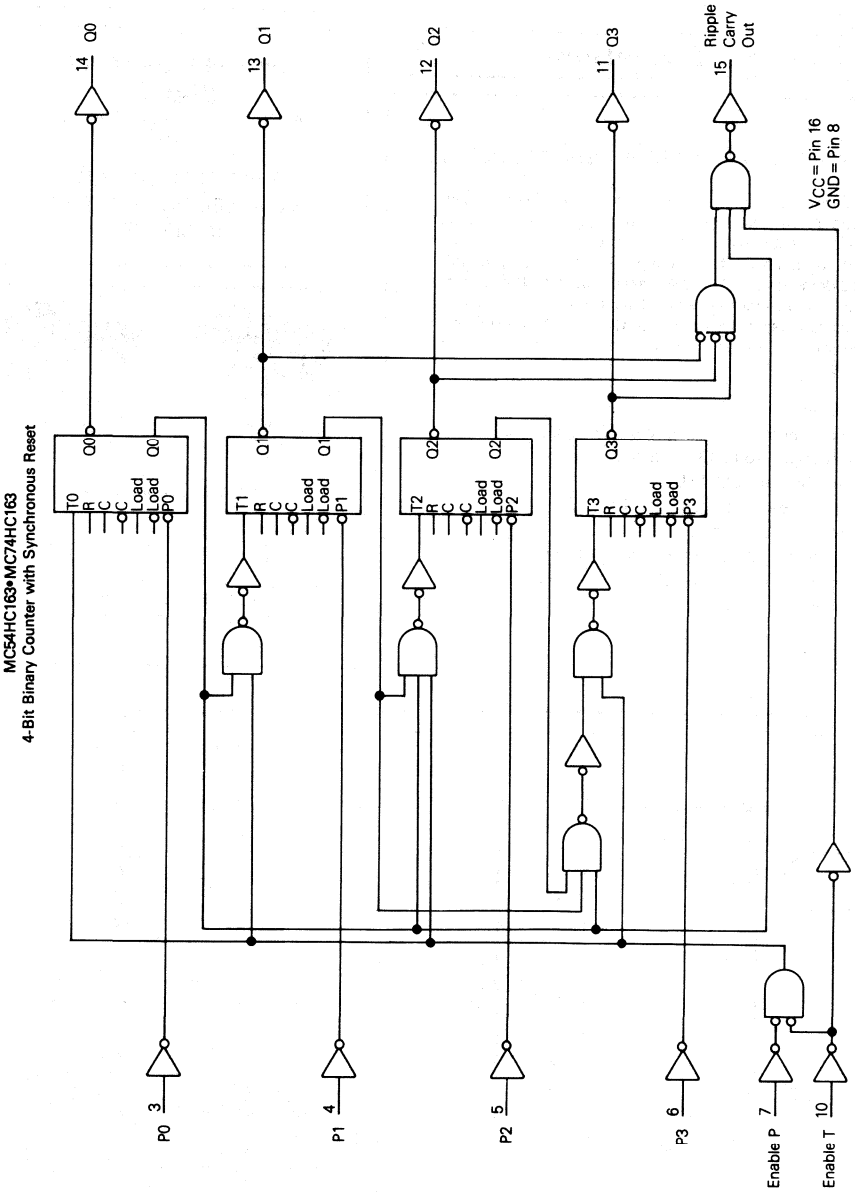


The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.



The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

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MOTOROLA

MC54/74HC164

Advance Information

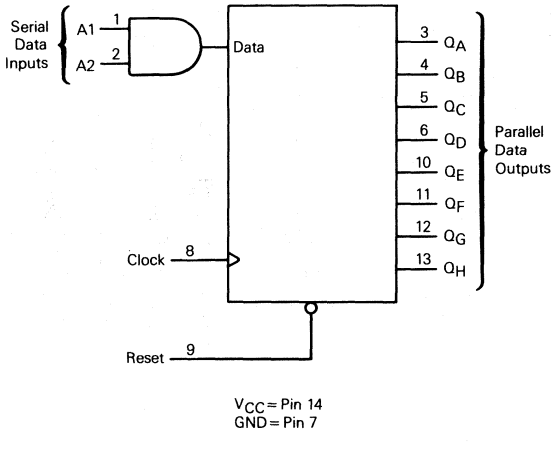
8-BIT SERIAL-INPUT/PARALLEL-OUTPUT SHIFT REGISTER

The MC54/74HC164 is identical in pinout to the LS164. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The MC54/74HC164 is an 8-bit, serial-input to parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. An asynchronous reset is provided, which is activated when a low level is present at its input. The Reset input is independent of the clock or data inputs.

- Asynchronous Reset
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM

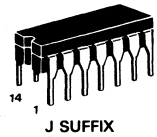


V_{CC} = Pin 14
GND = Pin 7

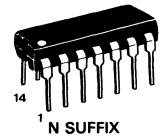
This document contains information on a new product. Specifications and information herein are subject to change without notice.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

8-BIT SERIAL-INPUT/ PARALLEL-OUTPUT SHIFT REGISTER



J SUFFIX
CERAMIC PACKAGE
CASE 632



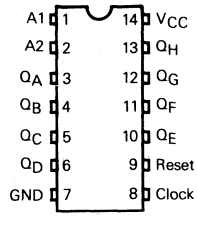
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs
Reset	Clock	A1 A2	Q_A Q_B . . . Q_H
L	X	X X	L L . . . L
H	↓	X X	no change
H	↑	L X	L Q_{An} . . . Q_{Gn}
H	↑	X L	L Q_{An} . . . Q_{Gn}
H	↑	H H	H Q_{An} . . . Q_{Gn}

Q_{An} − Q_{Gn} = Data shifted from the previous stage on a rising edge at the clock input.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	60	30	MHz
t_{PLH} t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	19 19	30 30	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	23	35	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	10 54 62	5 27 31	4 21 24	3 18 20	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	115 23 20	175 35 30	218 44 38	254 51 44	ns
t_{PHL}		2.0 4.5 6.0	115 23 20	175 35 30	218 44 38	254 51 44	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0 4.5 6.0	140 28 24	205 41 35	256 51 44	297 59 51	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	38 8 6	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		150	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, A1 or A2 to Clock (Figure 3)	2.0 4.5 6.0	25 5 4	50 10 9	65 13 11	75 15 13	ns
t_h	Minimum Hold Time, Clock to A1 or A2 (Figure 3)	2.0 4.5 6.0	−7 −2 −2	5 5 5	5 5 5	5 5 5	ns
t_{rec}	Minimum Recovery Time, Reset-Inactive to Clock (Figure 2)	2.0 4.5 6.0	−6 −2 −2	5 5 5	5 5 5	5 5 5	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	40 8 7	80 16 14	100 20 18	120 24 21	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	40 8 7	80 16 14	100 20 18	120 24 21	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

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PIN DESCRIPTIONS

INPUTS

A1, A2 (PINS 1, 2) — Serial Data Inputs. Data at these inputs determine the data to be entered into the first stage of the shift register. For a high logic level to be entered into the shift register, both A1 and A2 inputs must be high, thereby allowing one input to be used as a data-enable input. When only one serial input is used, the other must be connected to V_{CC}.

CLOCK (PIN 8) — Shift Register Clock. A positive-going voltage on this pin shifts the data at each stage to the next stage.

OUTPUTS

Q_A — Q_H (PINS 3, 4, 5, 6, 10, 11, 12, 13) — Parallel Shift Register Outputs. The shifted data is presented at these outputs in its true, or noninverted, form.

CONTROL INPUT

RESET (PIN 9) — Active Low, Asynchronous Reset Input. A low voltage applied to this input resets all internal flip-flops and produces low logic levels on the output, $Q_A - Q_H$.

FIGURE 1

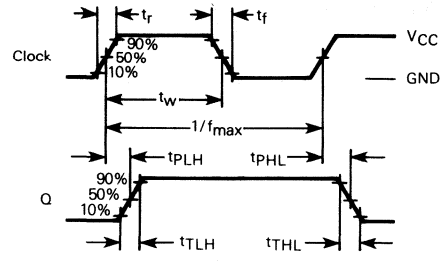


FIGURE 2

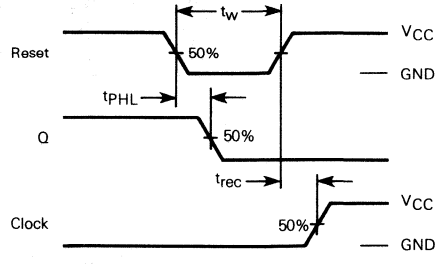


FIGURE 3

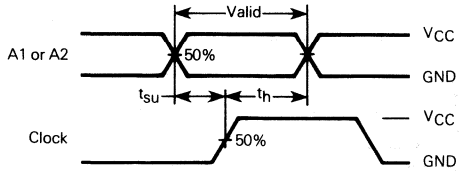
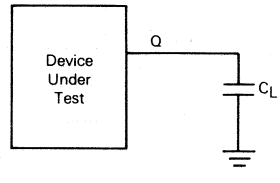


FIGURE 4 — TEST CIRCUIT



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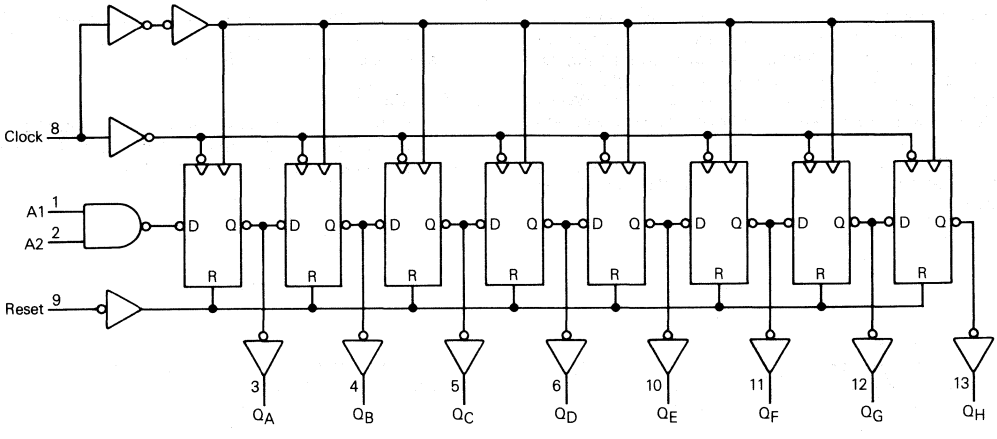
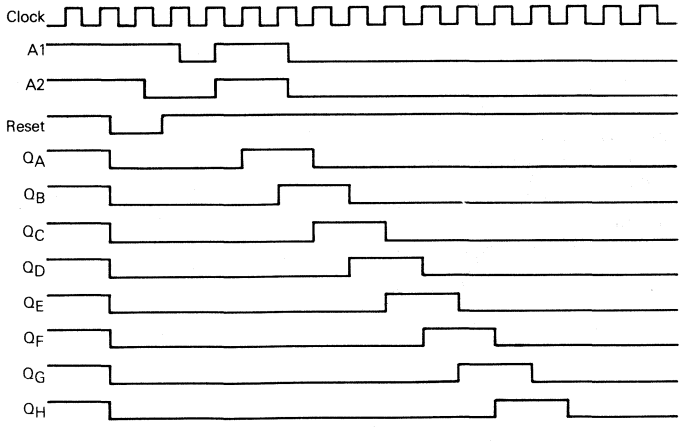
LOGIC DIAGRAM



TIMING DIAGRAM



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MOTOROLA

MC54/74HC165

Advance Information

8-BIT SERIAL- OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER

The MC54/74HC165 is identical in pinout to the LS165. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

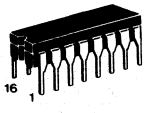
This device is an 8-bit shift register with complementary outputs from the last stage. Data may be loaded into the register either in parallel or in serial form. When the Serial Shift/Parallel Load input is low, the data is loaded asynchronously in parallel. When the Serial Shift/Parallel Load input is high, the data is loaded serially on the rising edge of either Clock 1 or Clock 2 (see the Function Table).

The 2-input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

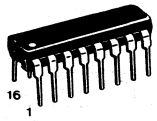
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

8-BIT SERIAL- OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER



J SUFFIX
CERAMIC PACKAGE
CASE 620



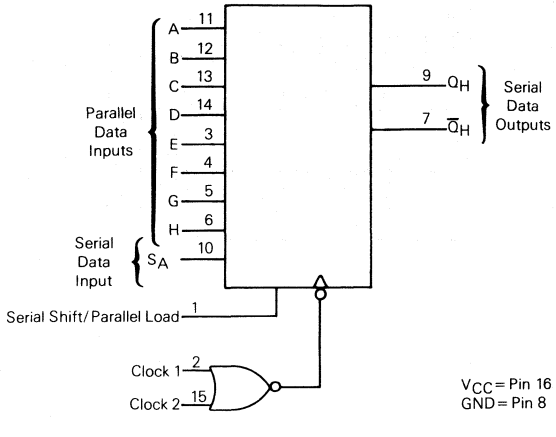
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

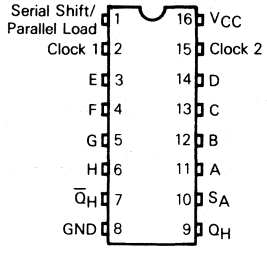
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74XXXN (Plastic Package)
MC74XXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 8)		30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q_H or $\overline{Q}_H$		25	ns
t_{PHL}	(Figures 1 and 8)		25	
t_{PLH}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q_H or $\overline{Q}_H$		30	ns
t_{PHL}	(Figures 2 and 8)		30	
t_{PLH}	Maximum Propagation Delay, H to Q_H or $\overline{Q}_H$		25	ns
t_{PHL}	(Figures 3 and 8)		25	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 8)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 8)	2.0	11	5	4	4	MHz
		4.5	54	27	21	18	
		6.0	64	32	25	21	
t_{PLH}	Maximum Propagation Delay, Clock to Q_H or $\overline{Q}_H$ (Figures 1 and 8)	2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{PHL}		2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{PLH}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q_H or $\overline{Q}_H$ (Figures 2 and 8)	2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PHL}		2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PLH}	Maximum Propagation Delay, H to Q_H or $\overline{Q}_H$ (Figures 3 and 8)	2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{PHL}		2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*			–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{su}	Minimum Setup Time, Parallel Data Inputs to Serial Shift/Parallel Load (Figure 4)	2.0 4.5 6.0	50 10 9	100 20 17	126 25 21	149 30 25	ns
t_{su}	Minimum Setup Time, S_A to Clock (Figure 5)	2.0 4.5 6.0	50 10 9	100 20 17	126 25 21	149 30 25	ns
t_{su}	Minimum Setup Time, Serial Shift/Parallel Load to Clock (Figure 6)	2.0 4.5 6.0	50 10 9	100 20 17	126 25 21	149 30 25	ns
t_{su}	Minimum Setup Time, Clock 1 (Clock Inhibit) to Clock 2 (or Clock 2 (Clock Inhibit) to Clock 1) (Figure 7)	2.0 4.5 6.0	50 10 9	100 20 17	126 25 21	149 30 25	ns
t_h	Minimum Hold Time, Serial Shift/Parallel Load to Parallel Data Input (Figure 4)	2.0 4.5 6.0	−20 −5 −3	0 0 0	0 0 0	0 0 0	ns
t_h	Minimum Hold Time, Clock to S_A (Figure 5)	2.0 4.5 6.0	−20 −5 −3	0 0 0	0 0 0	0 0 0	
t_h	Minimum Hold Time, Clock to Serial Shift/Parallel Load (Figure 6)	2.0 4.5 6.0	−20 −5 −3	0 0 0	0 0 0	0 0 0	ns
t_{rec}	Minimum Recovery Time, Clock 1 (Clock Inhibit) to Clock 2 (or Clock 2 (Clock Inhibit) to Clock 1) (Figure 7)	2.0 4.5 6.0	50 10 9	100 20 17	126 25 21	149 30 25	ns
t_w	Minimum Clock Pulse Width (Figure 1)	2.0 4.5 6.0	40 8 7	80 16 14	101 20 17	119 24 20	ns
t_w	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 2)	2.0 4.5 6.0	40 8 7	80 16 14	101 20 17	119 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

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FUNCTION TABLE

Inputs: Serial Shift/ Parallel Load	Clock 1	Clock 2	S_A	A-H	Internal Stages Q_A Q_B	Output Q_H	Operation
L	X	X	X	a...h	a b	h	Asynchronous Parallel Load
H	↑	L	L	X	L Q_{An}	Q_{Gn}	Serial Shift via Clock 1
H	↑	L	H	X	H Q_{An}	Q_{Gn}	
H	L	↑	L	X	L Q_{An}	Q_{Gn}	Serial Shift via Clock 2
H	L	↑	H	X	H Q_{An}	Q_{Gn}	
H	X	H	X	X	no change		Inhibited Clock
H	H	X	X	X			
H	L	L	X	X	no change		No Clock

X = don't care
↑ = transition from low to high
Q_{An}-Q_{Gn} = Data shifted from the preceding stage

PIN DESCRIPTIONS

INPUTS

A, B, C, D, E, F, G, H (PINS 11, 12, 13, 14, 3, 4, 5, 6) — Parallel Data Inputs. Data on these inputs are asynchronously entered in parallel into the internal flip flops when the Serial Shift/Parallel Load input is low.

S_A (PIN 10) — Serial Data Input. When the Serial Shift/Parallel Load input is high, data on this pin is serially entered into the first stage of the shift register with the rising edge of the clock.

CONTROL INPUTS

SERIAL SHIFT/PARALLEL LOAD (PIN 1) — Data-entry control input. When a high voltage level is applied to this pin, data at the Serial Data Input, S_A, are shifted into the register with the rising edge of the clock. When a low voltage level is applied to this pin, data at the Parallel Data inputs are asynchronously loaded into each of the eight internal stages.

CLOCK 1, CLOCK 2 (PINS 2, 15) — Clock inputs. These two clock inputs function identically. Either may be used as an active-high clock inhibit. However, to avoid double clocking, the inhibit input should go high only while the clock input is high.

OUTPUTS

Q_H, $\overline{Q}_H$ (PINS 9, 7) — Complementary Shift Register outputs. These pins are the noninverted and inverted outputs of the eighth stage of the shift register.

SWITCHING WAVEFORMS

FIGURE 1 — SERIAL-SHIFT MODE

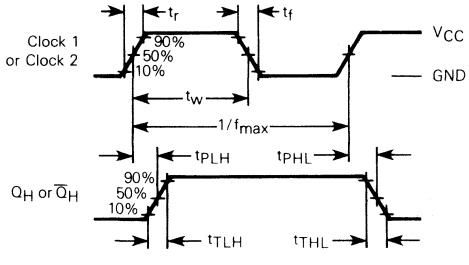

FIGURE 2 — PARALLEL-LOAD MODE

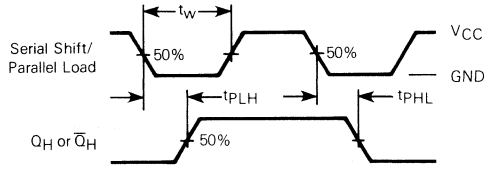

FIGURE 3 — PARALLEL-LOAD MODE

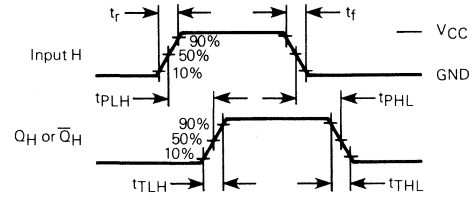

FIGURE 4 — PARALLEL-LOAD MODE

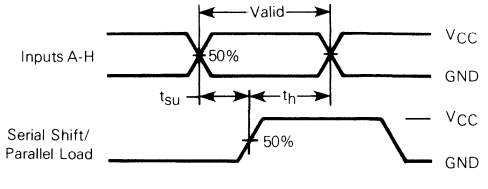

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FIGURE 5 — SERIAL-SHIFT MODE

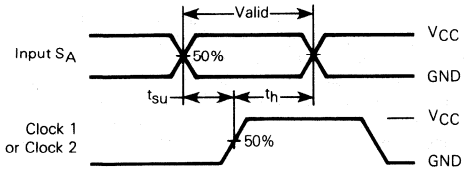


FIGURE 6 — SERIAL-SHIFT MODE

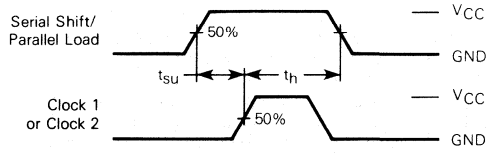


FIGURE 7 — SERIAL-SHIFT, CLOCK-INHIBIT MODE

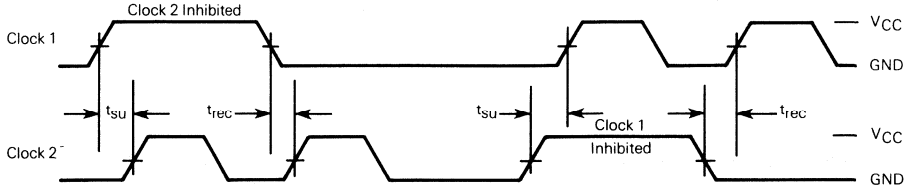
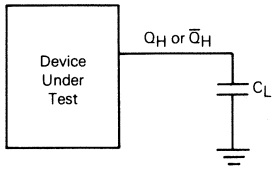


FIGURE 8 — TEST CIRCUIT



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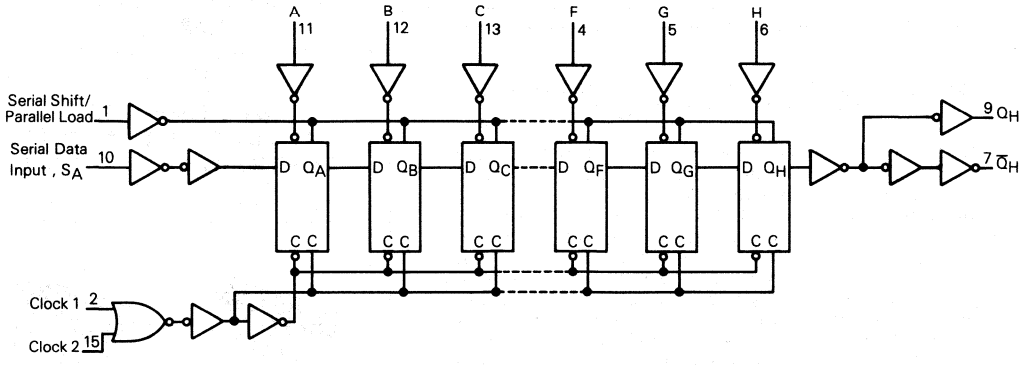
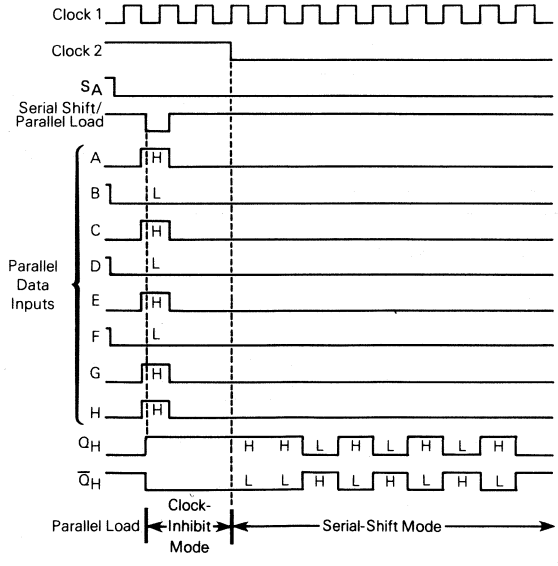
LOGIC DIAGRAM



TIMING DIAGRAM



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MOTOROLA

MC54/74HC166

Product Preview

8-BIT SERIAL- OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH RESET

The MC54/74HC166 is identical in pinout to the LS166. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

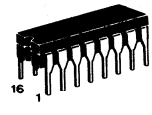
This device is an 8-bit shift register with an output from the last stage. Data may be loaded into the register either in parallel or in serial form. When the Serial Shift/Parallel Load input is low, the data is loaded asynchronously in parallel. When the Serial Shift/Parallel Load input is high, the data is loaded serially on the rising edge of either Clock 1 or Clock 2 (see the Function Table). Reset is asynchronous and active-low.

The 2-input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

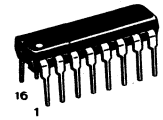
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

8-BIT SERIAL- OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH RESET



J SUFFIX
CERAMIC PACKAGE
CASE 620



N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74XXXN (Plastic Package)
MC74XXXJ (Ceramic Package)

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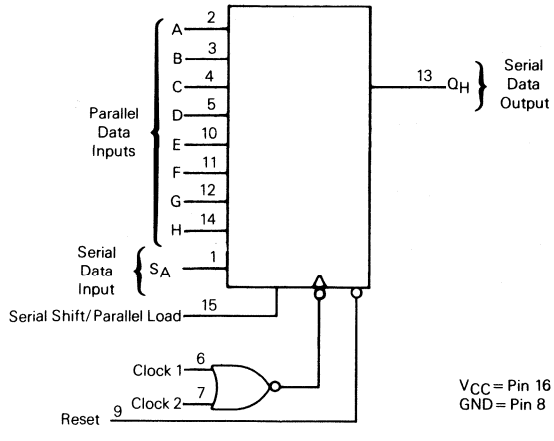
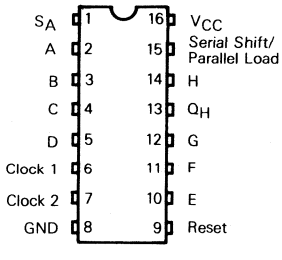
BLOCK DIAGRAM



PIN ASSIGNMENT



This document contains information on a product under development. Motorola reserves the right to change or discontinue this production without notice.

FUNCTION TABLE

Inputs						Internal Stages		Output	
Reset	Serial Shift/ Parallel Load	Clock 1	Clock 2	S_A	A-H	Q_A	Q_B	Q_H	Operation
H	L	X	X	X	a. . .h	a	b	h	Asynchronous Parallel Load
H	H	↑	L	L	X	L	Q_{An}	Q_{Gn}	Serial Shift via Clock 1
H	H	↑	L	H	X	H	Q_{An}	Q_{Gn}	
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}	Serial Shift via Clock 2
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}	
H	H	X	H	X	X	no change			Inhibited Clock
H	H	H	X	X	X				
H	H	L	L	X	X	no change			No Clock
L	X	X	X	X	X	L	L	L	Asynchronous Reset

X = don't care

↑ = transition from low to high

Q_{An}-Q_{Gn} = Data shifted from the preceding stage

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MOTOROLA

MC54/74HC173

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

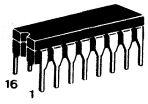
QUAD 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

QUAD 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

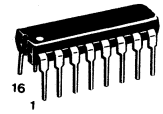
The MC54/74HC173 is identical in pinout to the LS173. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data, when enabled, are clocked into the four D flip-flops with the rising edge of the common clock. When either or both of the Output Enable Controls is high, the outputs are in a high-impedance state. This feature allows the HC173 to be used in bus-oriented systems. The reset feature is asynchronous and active high.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620



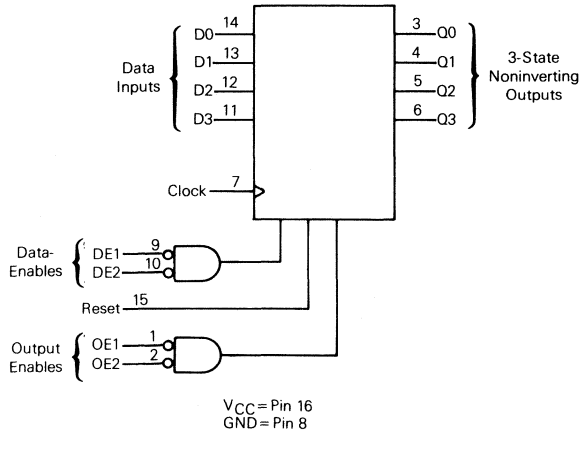
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

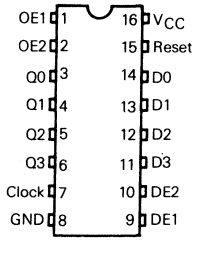
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\|$ = 20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\|$ = 20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{out} = −20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} I_{out} = −6.0 mA I_{out} = −7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{out} = 20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{out} = 6.0 mA I_{out} = 7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable = V_{IH} V_{out} = V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC		Unit
			Typical	Guaranteed Limit	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	C_L = 50 pF		30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q	C_L = 50 pF	17	31	ns
t_{PHL}	(Figures 1 and 5)		18	31	
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 5)	C_L = 50 pF	15	27	ns
t_{PLZ}	Maximum Propagation Delay, Output Enable to Q	C_L = 5 pF	11	25	ns
t_{PHZ}	(Figures 3 and 6)		13	25	
t_{PZL}	Maximum Propagation Delay, Output Enable to Q	C_L = 50 pF	10	28	ns
t_{PZH}	(Figures 3 and 6)		10	28	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	C_L = 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed Limit		
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	C_L = 50 pF	2.0	11	5	4	4	MHz
			4.5	54	27	21	18	
			6.0	64	32	25	21	
t_{PLH}	Maximum Propagation Delay, Clock to Q (Figures 1 and 5)	C_L = 50 pF	2.0	88	175	221	261	ns
		C_L = 150 pF		113	225	284	335	
		C_L = 50 pF	4.5	18	35	44	52	
		C_L = 150 pF		23	45	57	67	
		C_L = 50 pF	6.0	15	30	37	44	
		C_L = 150 pF		19	38	48	57	
t_{PHL}		C_L = 50 pF	2.0	88	175	221	261	ns
		C_L = 150 pF		113	225	284	335	
		C_L = 50 pF	4.5	18	35	44	52	
		C_L = 150 pF		23	45	57	67	
		C_L = 50 pF	6.0	15	30	37	44	
		C_L = 150 pF		19	38	48	57	
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 5)	C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	

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SWITCHING CHARACTERISTICS (Input $t_r = t_f = 6$ ns) (Continued)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{PLZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	$C_L = 50$ pF	2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PHZ}			2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PZL}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	$C_L = 50$ pF	2.0	75	150	189	224	ns
		$C_L = 150$ pF		100	200	252	298	
		$C_L = 50$ pF	4.5	15	30	38	45	
		$C_L = 150$ pF		20	40	50	60	
		$C_L = 50$ pF	6.0	13	26	32	38	
		$C_L = 150$ pF		17	34	43	51	
t_{PZH}		$C_L = 50$ pF	2.0	75	150	189	224	ns
		$C_L = 150$ pF		100	200	252	298	
		$C_L = 50$ pF	4.5	15	30	38	45	
		$C_L = 150$ pF		20	40	50	60	
		$C_L = 50$ pF	6.0	13	26	32	38	
		$C_L = 150$ pF		17	34	43	51	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	$C_L = 50$ pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{out}	Three-State Output Capacitance (Output Enable = V_{CC})		–					pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		–		–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{su}	Minimum Setup Time, Input D or DE to Clock (Figure 4)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Clock to Input D or DE (Figure 4)	2.0	−20	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−3	0	0	0	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	45	90	113	134	ns
		4.5	9	18	23	27	
		6.0	8	15	19	23	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

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SWITCHING WAVEFORMS

FIGURE 1

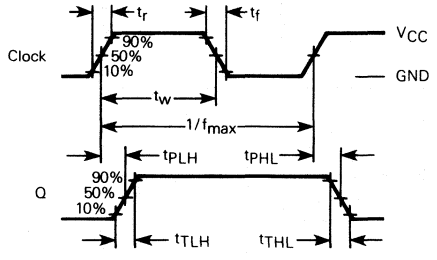

FIGURE 2

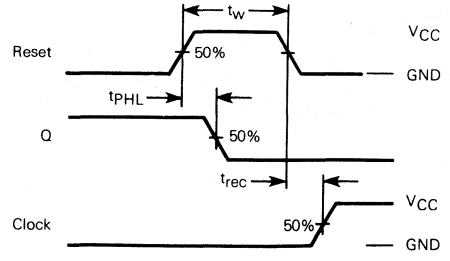

FIGURE 3

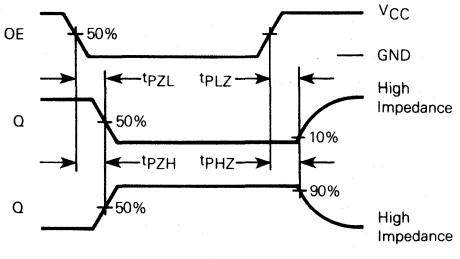

FIGURE 4

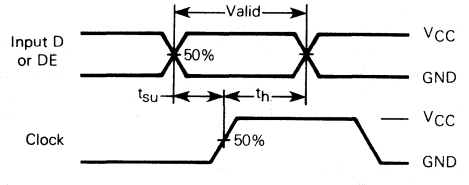

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FIGURE 5 — TEST CIRCUIT

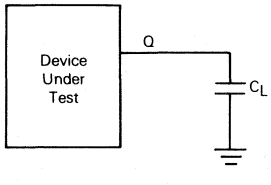
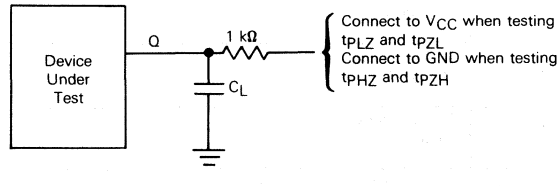


FIGURE 6 — TEST CIRCUIT



FUNCTION TABLE

Inputs							Output
Output Enables				Data Enables		Data	
OE1	OE2	Reset	Clock	DE1	DE2	D	Q
L	L	H	X	X	X	X	L
L	L	L	L	X	X	X	no change
L	L	L	H	X	X	X	no change
L	L	L	↑	H	X	X	no change
L	L	L	↑	X	H	X	no change
L	L	L	↑	L	L	L	L
L	L	L	↑	L	L	H	H
L	L	L	↓	X	X	X	no change
L	H	X	X	X	X	X	high impedance
H	L	X	X	X	X	X	high impedance
H	H	X	X	X	X	X	high impedance

PIN DESCRIPTIONS

INPUTS

D0, D1, D2, D3 (PINS 14, 13, 12, 11) — 4-bit data inputs. Data on these pins, when enabled by the Data-Enable Controls, are entered into the flip-flops on the rising edge of the clock.

CLOCK (PIN 7) — Clock input.

OUTPUTS

Q0, Q1, Q2, Q3 (PINS 3, 4, 5, 6) — 3-state register outputs. During normal operation of the device, the outputs of the D-type flip-flops appear at these pins. During 3-state operation, these outputs assume a high-impedance state.

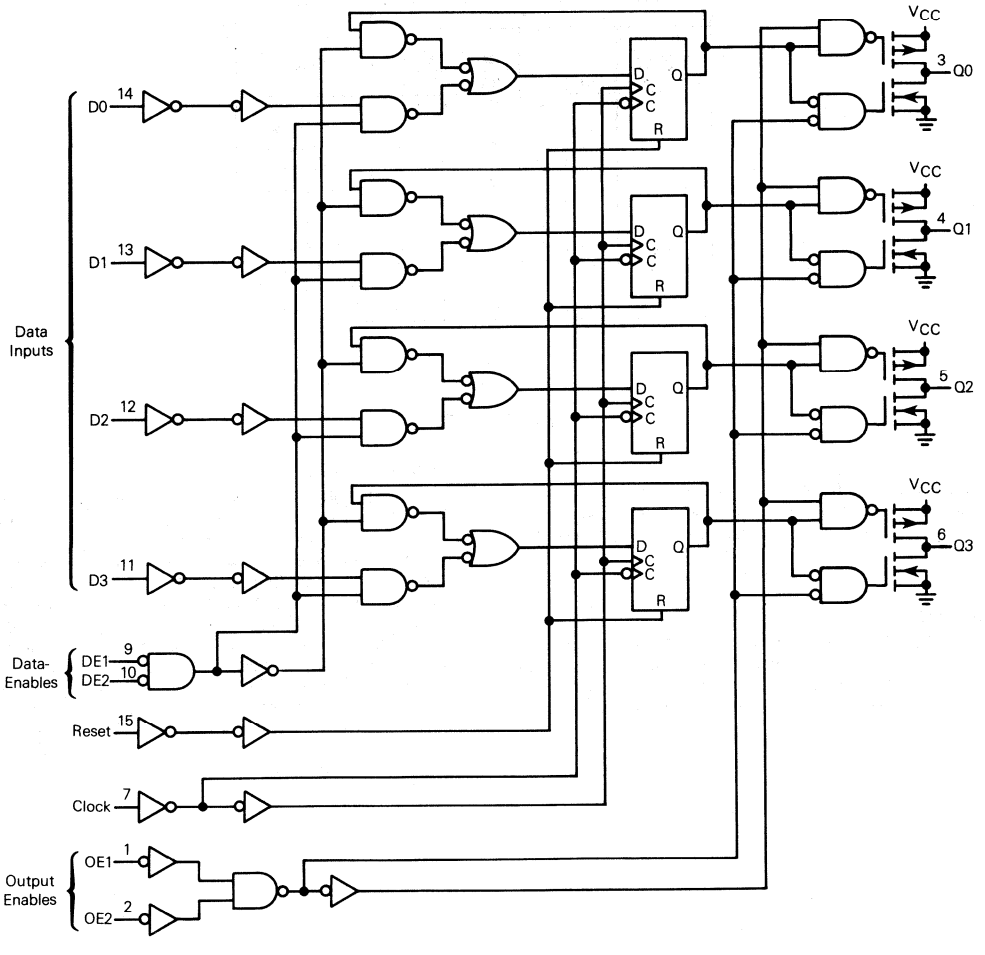
CONTROL INPUTS

RESET (PIN 15) — Asynchronous reset input. A high voltage level on this pin resets all flip-flops and forces the Q outputs low, if they are not already in high-impedance state.

DE1, DE2 (Pins 9, 10) — Active-low Data Enable Control inputs. When both Data Enable Controls are low, data at the D inputs are loaded into the flip-flops with the rising edge of the Clock input. When either or both of these controls are high, there is no change in the state of the flip-flops, regardless of any changes at the D or Clock inputs.

OE1, OE2 (Pins 1, 2) — Output Enable Control inputs. When either or both of the Output Enable Controls are high, the Q outputs of the device are in the high-impedance state. When both controls are low, the device outputs display the data in the flip-flops.

LOGIC DIAGRAM



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MOTOROLA

MC54/74HC174

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

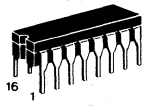
HEX D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

HEX D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

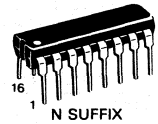
The MC54/74HC174 is identical in pinout to the LS174. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six D-type flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active-low.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum Range (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620



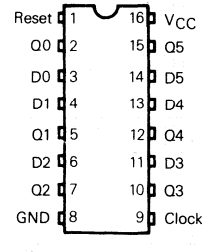
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

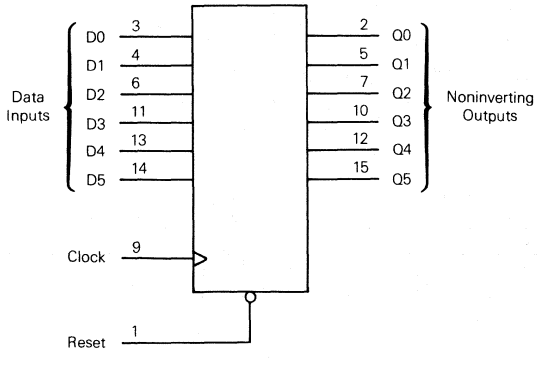
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40° to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

Inputs			Outputs
Reset	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	no change
H	↓	X	no change

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	60	30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q	16	30	ns
t_{PHL}	(Figures 1 and 4)	16	30	
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	16	30	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	10	5	4	3	MHz
		4.5	54	27	21	18	
		6.0	62	31	24	20	
t_{PLH}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	55	165	206	248	ns
		4.5	18	33	41	49	
		6.0	16	28	35	42	
t_{PHL}		2.0	55	165	206	248	ns
		4.5	18	33	41	49	
		6.0	16	28	35	42	
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0	55	165	206	248	ns
		4.5	18	33	41	49	
		6.0	16	28	35	42	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		136	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0	50	100	125	150	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Clock to Data (Figure 3)	2.0	−10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	−10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	106	120	ns
		4.5	8	16	20	24	
		6.0	7	14	18	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	40	80	106	120	ns
		4.5	8	16	20	24	
		6.0	7	14	18	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

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SWITCHING WAVEFORMS

FIGURE 1

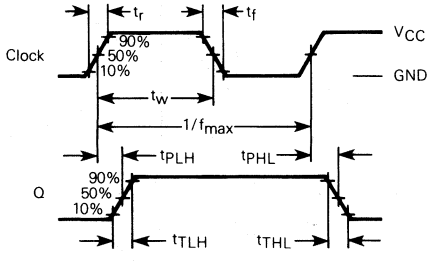


FIGURE 2

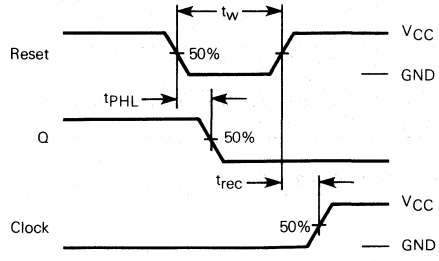


FIGURE 3

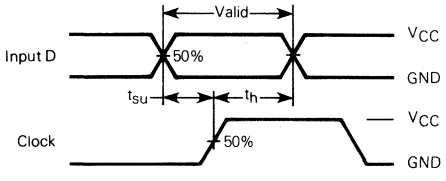
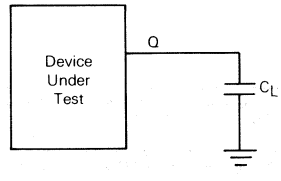
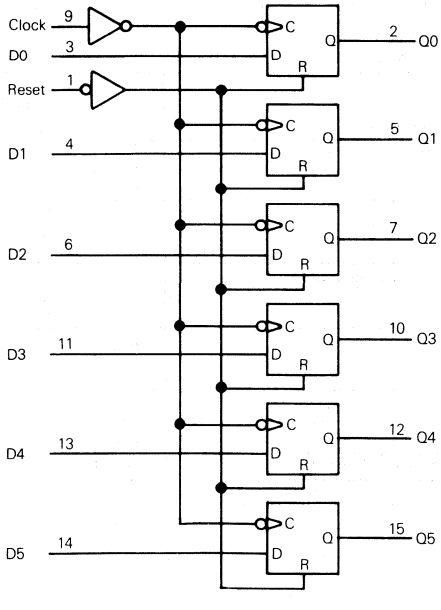


FIGURE 4 — TEST CIRCUIT



LOGIC DIAGRAM



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MOTOROLA

MC54/74HC175

Advance Information

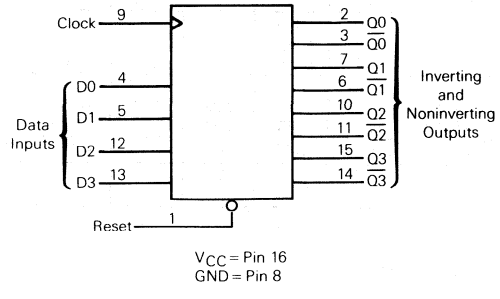
QUAD D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

The MC54/74HC175 is identical in pinout to the LS175. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of four D-type flip-flops with common Reset and Clock inputs, and separate D inputs. Reset (active low) is asynchronous and occurs when a low voltage is applied to the Reset input. Information at a D input is transferred to the corresponding Q output on the next positive-going edge of the Clock input.

- Asynchronous Reset
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

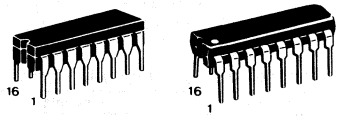
BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET



J SUFFIX
CERAMIC PACKAGE
CASE 620

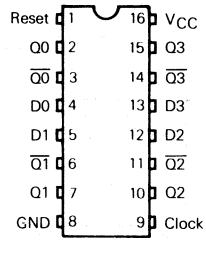
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC54HCXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs	
Reset	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	no change	

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)		35	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		25	ns
t_{PHL}	(Figures 1 and 4)		25	
t_{PHL}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$ (Figures 3 and 4)		20	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	12	6	5	4	MHz
		4.5	60	30	24	20	
		6.0	71	35	28	24	
t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{PHL}		2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{PHL}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$ (Figures 3 and 4)	2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		60	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
			Typical	Guaranteed Limit			
t_{su}	Minimum Setup Time, Data to Clock (Figure 2)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Clock to Data (Figure 2)	2.0	−20	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−3	0	0	0	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 3)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Reset (Figure 3)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

SWITCHING WAVEFORMS

FIGURE 1

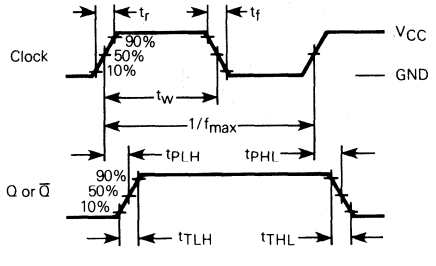


FIGURE 3

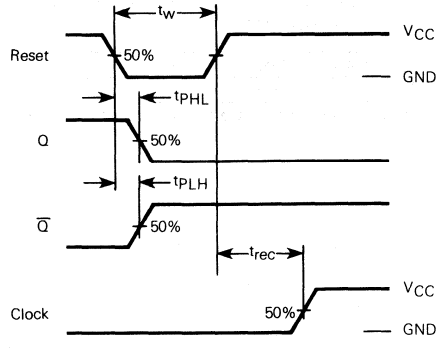


FIGURE 2

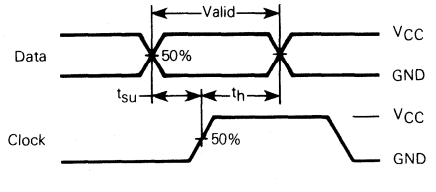
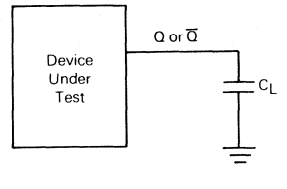


FIGURE 4 — TEST CIRCUIT



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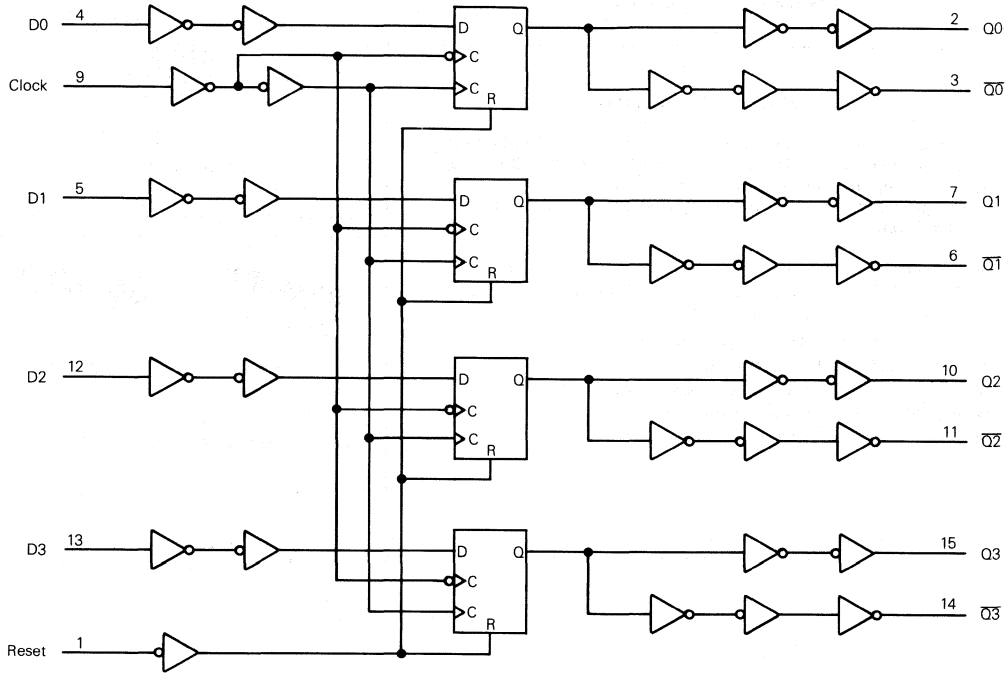
LOGIC DIAGRAM



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MOTOROLA

MC54/74HC181

Product Preview

4-BIT ARITHMETIC LOGIC UNIT

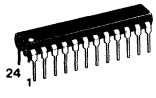
The MC54/74HC181 is identical in pinout to the LS181. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device can perform all 16 logic operations and a variety of arithmetic operations on two 4-Bit words.

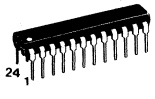
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

4-BIT ARITHMETIC LOGIC UNIT



J SUFFIX
CERAMIC PACKAGE
CASE 758



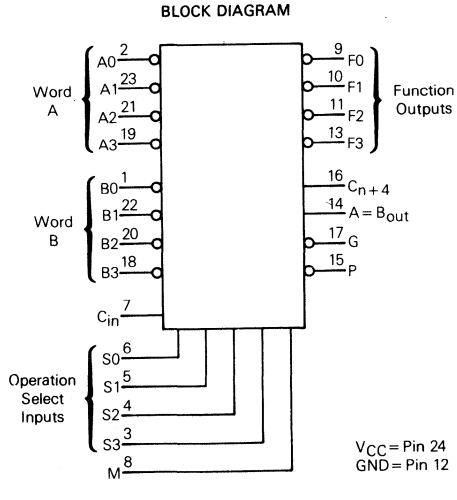
N SUFFIX
PLASTIC PACKAGE
CASE 724

ORDERING INFORMATION

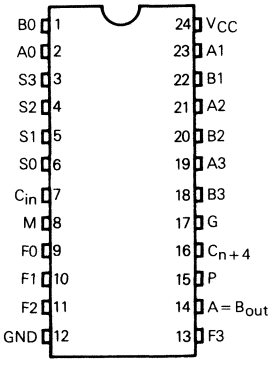
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

MC54/74HC182

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

CARRY LOOKAHEAD GENERATOR

CARRY LOOKAHEAD GENERATOR

The MC54/74HC182 is identical in pinout to the LS182. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC182 is a high-speed Carry Lookahead Generator. It is used with the HC181 or LS181 4-Bit Arithmetic Logic Unit to provide high speed lookahead over word lengths of more than four bits. The device accepts up to four pairs of active-low Carry Propagate (P0, P1, P2, P3) and Carry Generate (G0, G1, G2, G3) signals and an active-high Carry Input and provides anticipated active-high carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The HC182 also has active-low Carry Propagate (P) and Carry Generate (G) outputs which may be used for further levels of lookahead.

The logic equations provided at the outputs are:

$P = P3 + P2 + P1 + P0$

$G = G3 \bullet P3 + G3 \bullet G2 \bullet P2 + G3 \bullet G2 \bullet G1 \bullet P1 + G3 \bullet G2 \bullet G1 \bullet G0$

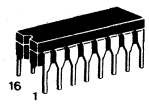
$C_{n+x} = \overline{G0} + \overline{P0} \bullet$ Carry In

$C_{n+y} = \overline{G1} + \overline{P1} \bullet \overline{G0} + \overline{P0} \bullet$ Carry In

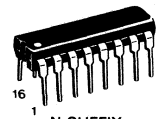
$C_{n+z} = \overline{G2} + \overline{P2} \bullet \overline{G1} + \overline{P2} \bullet \overline{P1} \bullet \overline{G0} + \overline{P2} \bullet \overline{P1} \bullet \overline{P0} \bullet$ Carry In

Also, the HC182 can be used with binary ALUs in an active-low or active-high input operand mode. The connections to and from the ALU to the carry lookahead generator are identical in both cases.

- Provides Carry Lookahead Across a Group of Four ALUs
- Multi-Level Lookahead for High-Speed Arithmetic Operation Over Long Word Lengths
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620



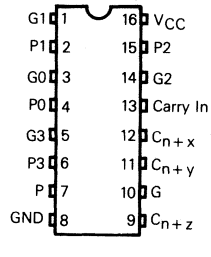
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



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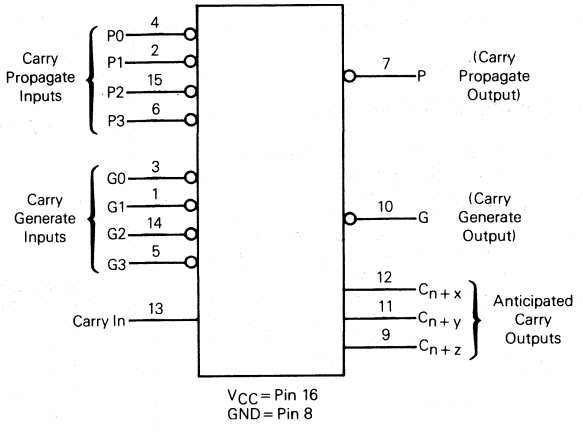
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



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MOTOROLA

MC54/74HC190

Product Preview

PRESETTABLE BCD UP/DOWN COUNTER

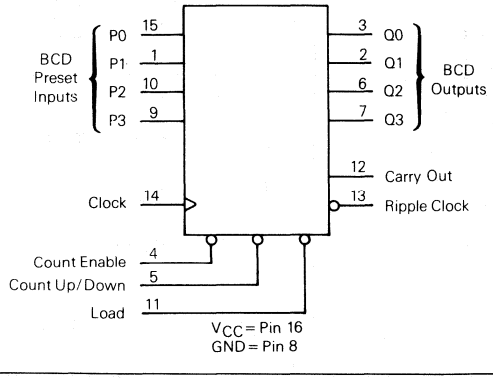
The MC54/74HC190 is identical in pinout to the LS190. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This counter can be preset by applying the desired value in BCD to the Preset Inputs and then bringing the Load input low. Counting is achieved when the Load input is high, the Count Enable pin is low, and the Count Up/Down pin is either low (for up-counting) or high (for down-counting). The state of the counter changes on the positive transition of the Clock input.

Two outputs have been made available to perform the cascading function: Ripple Clock and Carry Out. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The Ripple Clock output produces a low-level output pulse equal in width to the low-level portion of the Clock when an overflow or underflow condition exists. The counters can be cascaded by feeding the Ripple Clock output to the Count Enable input of the succeeding counter if parallel clocking is used, or to the Clock input if parallel enabling is used. Carry Out can be used to accomplish look-ahead for high-speed operation.

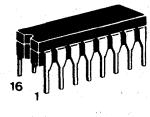
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM

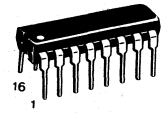


HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

PRESETTABLE BCD UP/DOWN COUNTER



J SUFFIX
CERAMIC PACKAGE
CASE 620



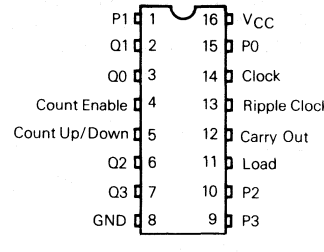
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs				
Load	Count Enable	Count Up/Down	Clock	Function
H	L	L	⎍	Count Up
H	L	H	⎍	Count Down
L	X	X	X	Preset (Asynch.)
H	H	X	X	No Change

5

MOTOROLA

MC54/74HC191

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

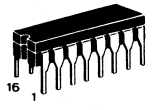
PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

The MC54/74HC191 is identical in pinout to the LS191. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

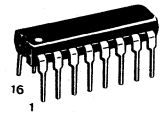
This counter can be preset by applying the desired value in 4-bit binary to the Preset Inputs and then bringing the Load input low. Counting is achieved when the Load input is high, the Count Enable pin is low, and the Count Up/Down pin is either low (for up-counting) or high (for down-counting). The state of the counter changes on the positive transition of the Clock input.

Two outputs have been made available to perform the cascading function: Ripple Clock and Carry Out. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The Ripple Clock output produces a low-level pulse equal in width to the low-level portion of the Clock when an overflow or underflow condition exists. The counters can be cascaded by feeding the Ripple Clock output to the Count Enable input of the succeeding counter if parallel clocking is used, or to the Clock input if parallel enabling is used. The Carry Out can be used to accomplish look-ahead for high-speed operation.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620



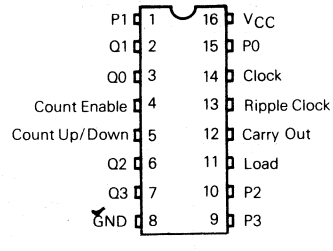
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



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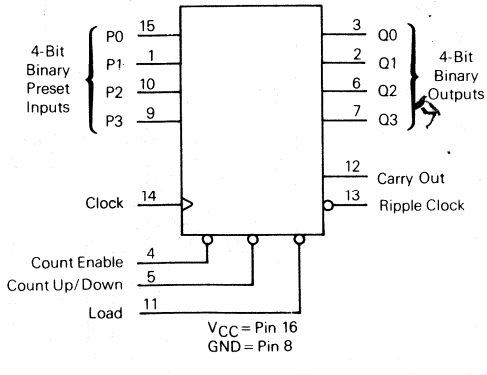

FUNCTION TABLE

Inputs				
Load	Count Enable	Count Up/Down	Clock	Function
H	L	L	⌐¬	Count Up
H	L	H	⌐¬	Count Down
L	X	X	X	Preset (Asynch.)
H	H	X	X	No Change

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MOTOROLA

MC54/74HC192

Product Preview

PRESETTABLE BCD UP/DOWN COUNTER WITH RESET

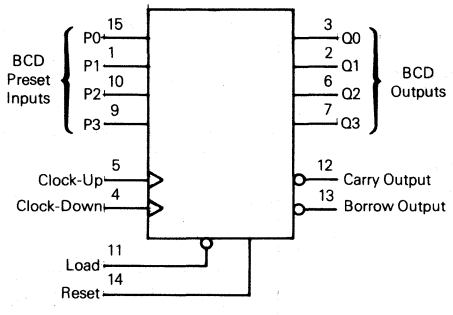
The MC54/74HC192 is identical in pinout to the LS192. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This counter can be preset by applying the desired value in BCD to the preset inputs and then bringing the Load input low. Up or down counting is achieved by bringing the Load input high and clocking the appropriate clock input. The state of the counter changes on the positive transition of the appropriate clock input. In the count-up mode, Carry goes low half a clock period before the zero state is reached and returns high when the zero state is reached. In the count-down mode, Borrow goes low half a clock period before the nine state is reached and returns high when the nine state is reached. Reset is active high and forces Q0 thru Q3 low.

These counters can be cascaded by connecting Carry and Borrow of the least-significant counter to Clock-up and Clock-down respectively, of the next more-significant counter.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

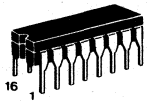
BLOCK DIAGRAM



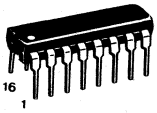
V_{CC} = Pin 16
GND = Pin 8

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

PRESETTABLE BCD UP/DOWN COUNTER WITH RESET



J SUFFIX
CERAMIC PACKAGE
CASE 620



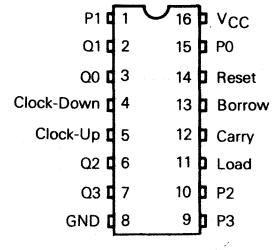
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Clock Up	Clock Down	Reset	Load	Function
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Reset
X	X	L	L	Load Preset Inputs

MOTOROLA

MC54/74HC193

Product Preview

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER WITH RESET

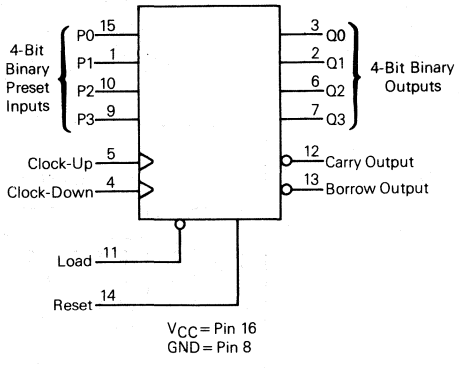
The MC54/74HC193 is identical in pinout to the LS193. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This counter can be preset by applying the desired value in 4-bit binary to the preset inputs and then bringing the Load input low. Up or down counting is achieved by bringing the Load input high and clocking the appropriate clock input. The state of the counter changes on the positive transition of the appropriate clock input. In the count-up mode, Carry goes low half a clock period before the zero state is reached and returns high when the zero state is reached. In the count-down mode, Borrow goes low half a clock period before the fifteen state is reached and returns high when the fifteen state is reached. Reset is active high and forces Q0 thru Q3 low.

These counters can be cascaded by connecting Carry and Borrow of the least significant counter to Clock-up and Clock-down, respectively, of the next more significant counter.

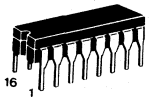
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM

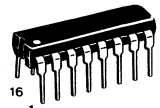


HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER WITH RESET



J SUFFIX
CERAMIC PACKAGE
CASE 620



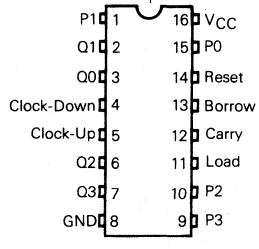
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Clock Up	Clock Down	Reset	Load	Function
↓	H	L	H	Count Up
H	↓	L	H	Count Down
X	X	H	X	Reset
X	X	L	L	Load Preset Inputs

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MOTOROLA

MC54/74HC194

Advance Information

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

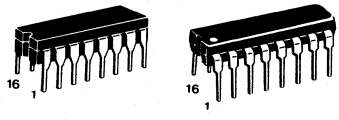
The MC54/74HC194 is identical in pinout to the LS194 and the MC14194B metal gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

This static shift register features parallel load, serial load (shift right and shift left), hold, and reset modes of operation. These modes are tabulated in the Function Table, and further explanation can be found in the Pin Description section.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER



J SUFFIX
CERAMIC PACKAGE
CASE 620

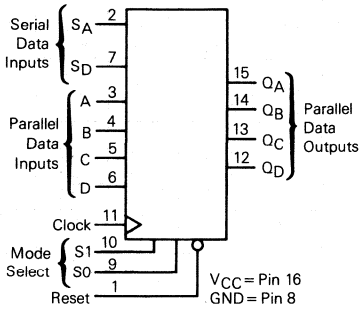
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

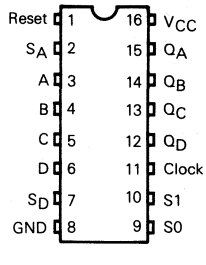
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\|$ = 20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\|$ = 20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{out} = −20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} I_{out} = −4.0 mA I_{out} = −5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{out} = 20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{out} = 4.0 mA I_{out} = 5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC		Unit
		Typical	Guaranteed Limit	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	–	35	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q	–	24	ns
t_{PHL}	(Figures 1 and 4)	–	24	
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	–	25	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
			Typical	Guaranteed Limit			
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	12	6	5	4	MHz
		4.5	60	30	24	20	
		6.0	71	35	28	24	
t_{PLH}	Maximum Propagation Delay, Clock to Q	2.0	73	145	183	216	ns
	(Figures 1 and 4)	4.5	15	29	37	43	
		6.0	12	25	31	37	
t_{PHL}		2.0	73	145	183	216	ns
		4.5	15	29	37	43	
		6.0	12	25	31	37	
t_{PHL}	Maximum Propagation Delay, Reset to Q	2.0	75	150	189	224	ns
	(Figures 2 and 4)	4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	2.0	38	75	95	110	ns
	(Figures 1 and 4)	4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*			–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, A, B, C, D to Clock (Figure 3)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_{su}	Minimum Setup Time, S1, S0 to Clock (Figure 3)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_{su}	Minimum Setup Time, S_A or S_D to Clock (Figure 3)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Clock to any Input (except Reset) (Figure 3)	2.0	−20	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−3	0	0	0	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	−10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

FUNCTION TABLE

Inputs									Outputs				
	Mode Select			Serial Data		Parallel Data							
Reset	S1	S0	Clock	S_D	S_A	A	B	C	D	Q_A	Q_B	Q_C	Q_D	Operating Mode
L	X	X	X	X	X	X	X	X	X	L	L	L	L	Reset
H	H	H	↑	X	X	a	b	c	d	a	b	c	d	Parallel Load
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Shift Right
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H	Shift Left
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L	
H	L	L	X	X	X	X	X	X	X	no change				Hold
H	X	X	L	X	X	X	X	X	X	no change				
H	X	X	H	X	X	X	X	X	X	no change				

H = high level (steady state)
L = low level (steady state)
X = don't care
↑ = transition from low to high level.

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↑ transition of the clock.

PIN DESCRIPTION

DATA INPUTS

A, B, C, D (PINS 3, 4, 5, 6) — Parallel data inputs.

S_A (PIN 2) — Serial-data input when using shift-right mode.

S_D (PIN 7) — Serial-data input when using shift-left mode.

OUTPUTS

Q_A, Q_B, Q_C, Q_D (PINS 15, 14, 13, 12) — Parallel data outputs.

CONTROL INPUTS

CLOCK (PIN 11) — Clock Input.

RESET (PIN 1) — A low logic level applied to this pin resets all stages and forces all outputs low.

S0, S1 (PINS 9, 10) — Mode-select inputs. These inputs control the mode of operation as described in the function table and below.

Parallel Load Mode (S1 = H, S0 = H) — Data is loaded into the device with a positive transition of the Clock input.

Shift Right Mode (S1 = L, S0 = H) — With a positive transition of the Clock input, each bit is shifted right (in the direction Q_A toward Q_D) one stage and data on the S_A Serial Data Input is shifted into stage A.

Shift Left Mode (S1 = H, S0 = L) — With a positive transition of the clock input, each bit is shifted left (in the direction Q_D toward Q_A) one stage and data on the S_D Serial Data Input is shifted into stage D.

Hold Mode (S1 = L, S0 = L) — Outputs are held.

SWITCHING WAVEFORMS

FIGURE 1

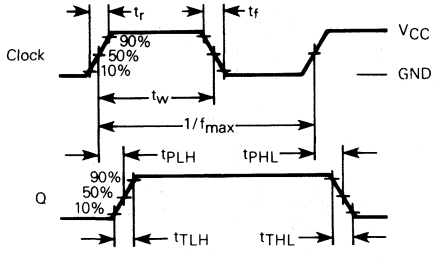


FIGURE 2

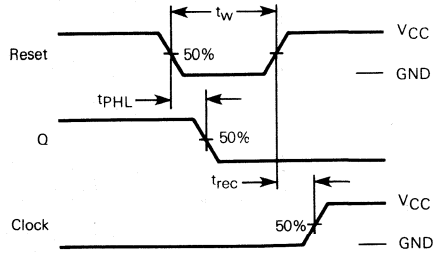


FIGURE 3

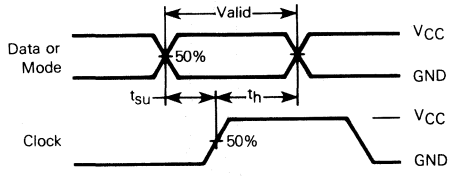
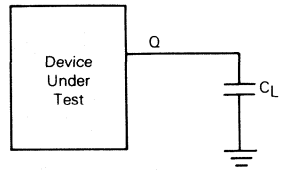


FIGURE 4 — TEST CIRCUIT



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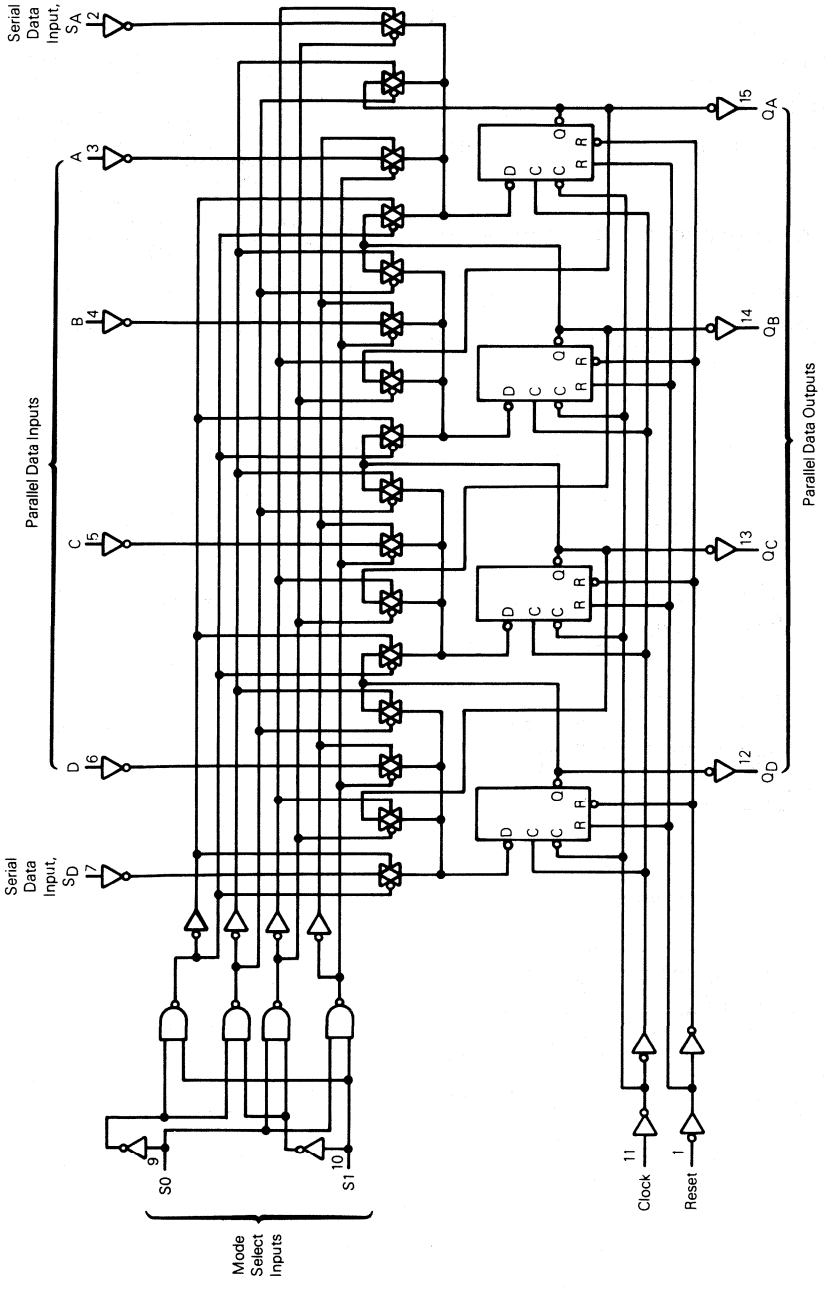
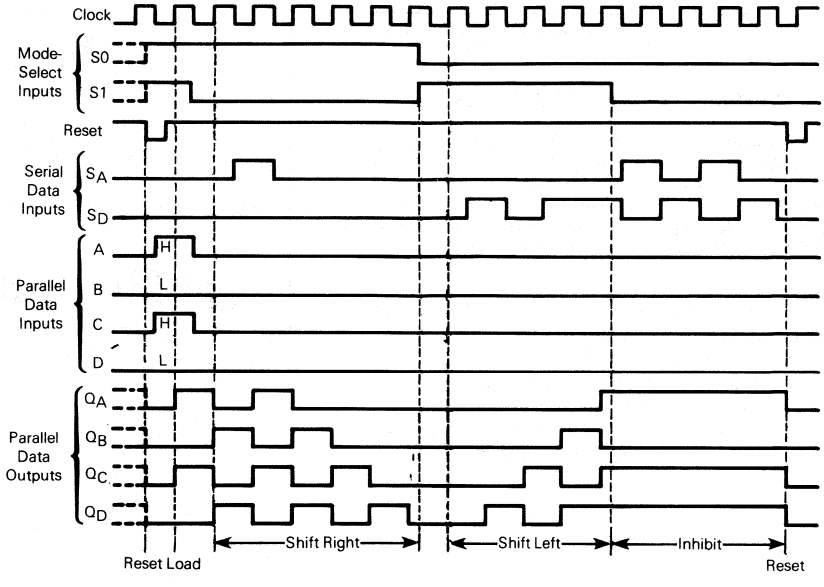
LOGIC DIAGRAM



TIMING DIAGRAM



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MOTOROLA

MC54/74HC195

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

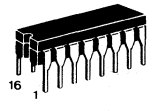
4-BIT UNIVERSAL SHIFT REGISTER

4-BIT UNIVERSAL SHIFT REGISTER

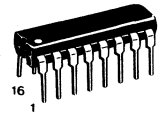
The MC54/74HC195 is identical in pinout to the LS195. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

This static shift register features parallel load, serial load (shift right), hold, and reset modes of operation. These modes are tabulated in the function table, and further explanation can be found in the Pin Description section.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620



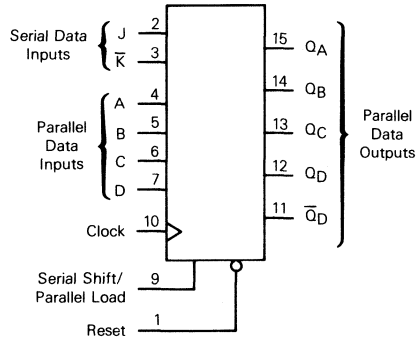
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

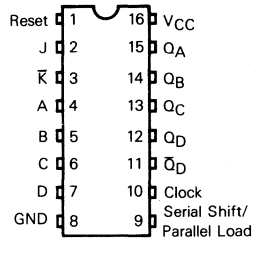
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)		35	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q		24	ns
t_{PHL}	(Figures 1 and 5)		24	
t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}_D$		24	ns
t_{PHL}	(Figures 1 and 5)		24	
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 5)		25	ns
t_{PLH}	Maximum Propagation Delay, Reset to $\overline{Q}_D$ (Figures 2 and 5)		25	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0	12	6	5	4	MHz
		4.5	60	30	24	20	
		6.0	71	35	28	24	
t_{PLH}	Maximum Propagation Delay, Clock to Q (Figures 1 and 5)	2.0	73	145	183	216	ns
		4.5	15	29	37	43	
		6.0	12	25	31	37	
t_{PHL}		2.0	73	145	183	216	ns
		4.5	15	29	37	43	
		6.0	12	25	31	37	
t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}_D$ (Figures 1 and 5)	2.0	73	145	183	216	ns
		4.5	15	29	37	43	
		6.0	12	25	31	37	
t_{PHL}		2.0	73	145	183	216	ns
		4.5	15	29	37	43	
		6.0	12	25	31	37	
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 5)	2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{PLH}	Maximum Propagation Delay, Reset to $\overline{Q}_D$ (Figures 2 and 5)	2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*			–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, A, B, C, D, J, or $\overline{K}$ to Clock (Figure 3)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_{su}	Minimum Setup Time, Serial Shift/Parallel Load to Clock (Figure 4)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Clock to A, B, C, D, J, or $\overline{K}$ (Figure 3)	2.0	−20	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−3	0	0	0	
t_h	Minimum Hold Time, Clock to Serial Shift/Parallel Load (Figure 4)	2.0	−20	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−3	0	0	0	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	−10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

FUNCTION TABLE

Inputs									Outputs					
			Serial		Parallel									
Reset	Shift/Load	Clock	J	$\overline{K}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$	Operating Mode
L	X	X	X	X	X	X	X	X	L	L	L	L	H	Reset
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$	Parallel Load
H	H	L	X	X	X	X	X	X	no change					Hold
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$	Retain First Stage (Serial Shift)
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$	Reset First Stage (Serial Shift)
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$	Set First Stage (Serial Shift)
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$	Toggle First Stage (Serial Shift)

H = high level (steady state)
L = low level (steady state)
X = don't care
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0} = the level of Q_A before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent ↑ transition of the clock.

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PIN DESCRIPTION

DATA INPUTS

A, B, C, D, (PINS 4, 5, 6, 7) — Parallel data inputs.

OUTPUTS

Q_A, Q_B, Q_C, Q_D, $\overline{Q_D}$ (PINS 15, 14, 13, 12, 11) — Parallel data outputs.

CONTROL INPUTS

CLOCK (PIN 10) — Clock input.

SERIAL SHIFT/ PARALLEL LOAD (PIN 9) — Shift or load control. A low logic level applied to this pin allows data to be loaded from the parallel inputs. Data is loaded with the positive transition of the clock input. A high logic level allows data to be shifted in the manner dictated by the J and $\overline{K}$ control inputs.

RESET (PIN 1) — A low logic level applied to this pin resets all stages and forces all outputs low.

J, $\overline{K}$ (PINS 2, 3) — Shift Control. With Serial Shift/ Parallel Load high, J and $\overline{K}$ control the mode of operation, as illustrated in the Function Table.

J = L, $\overline{K}$ = H — With a positive transition of the clock input, each bit is shifted to the right (in the direction Q_A toward Q_D) one stage and stage A maintains its previous state.

J = H, $\overline{K}$ = L — With a positive transition of the clock input, each bit is shifted right (in the direction of Q_A toward Q_D) one stage and the Q_A output is inverted.

J = $\overline{K}$ = L — With a positive transition of the clock input, each bit is shifted right (in the direction Q_A toward Q_D) one stage and a logic low is loaded into stage A.

J = $\overline{K}$ = H — With a positive transition of the clock input, each bit is shifted right (in the direction Q_A toward Q_D) one stage and a logic high is loaded into stage A.

SWITCHING WAVEFORMS

FIGURE 1

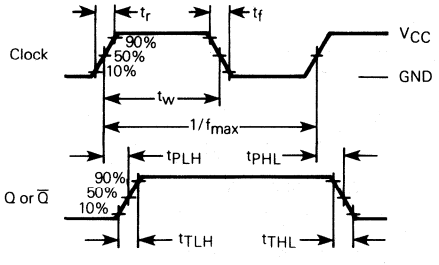

FIGURE 2

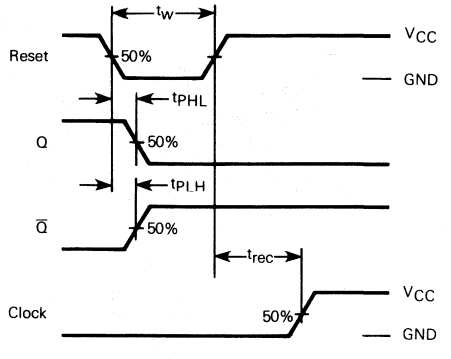

FIGURE 3

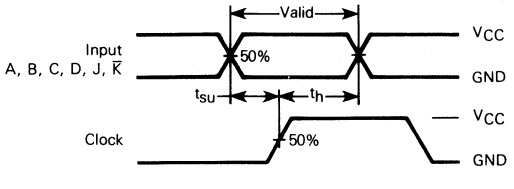

FIGURE 4

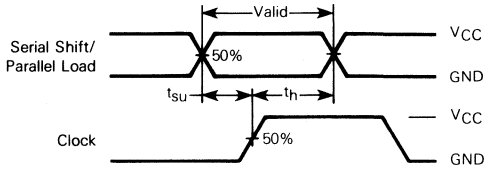

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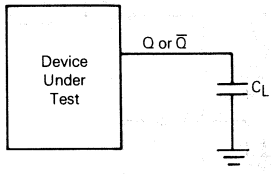
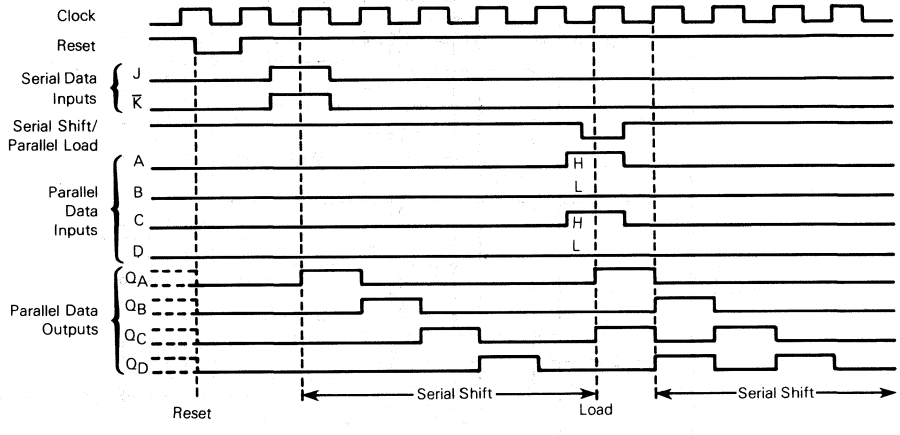
FIGURE 5 — TEST CIRCUIT



TIMING DIAGRAM



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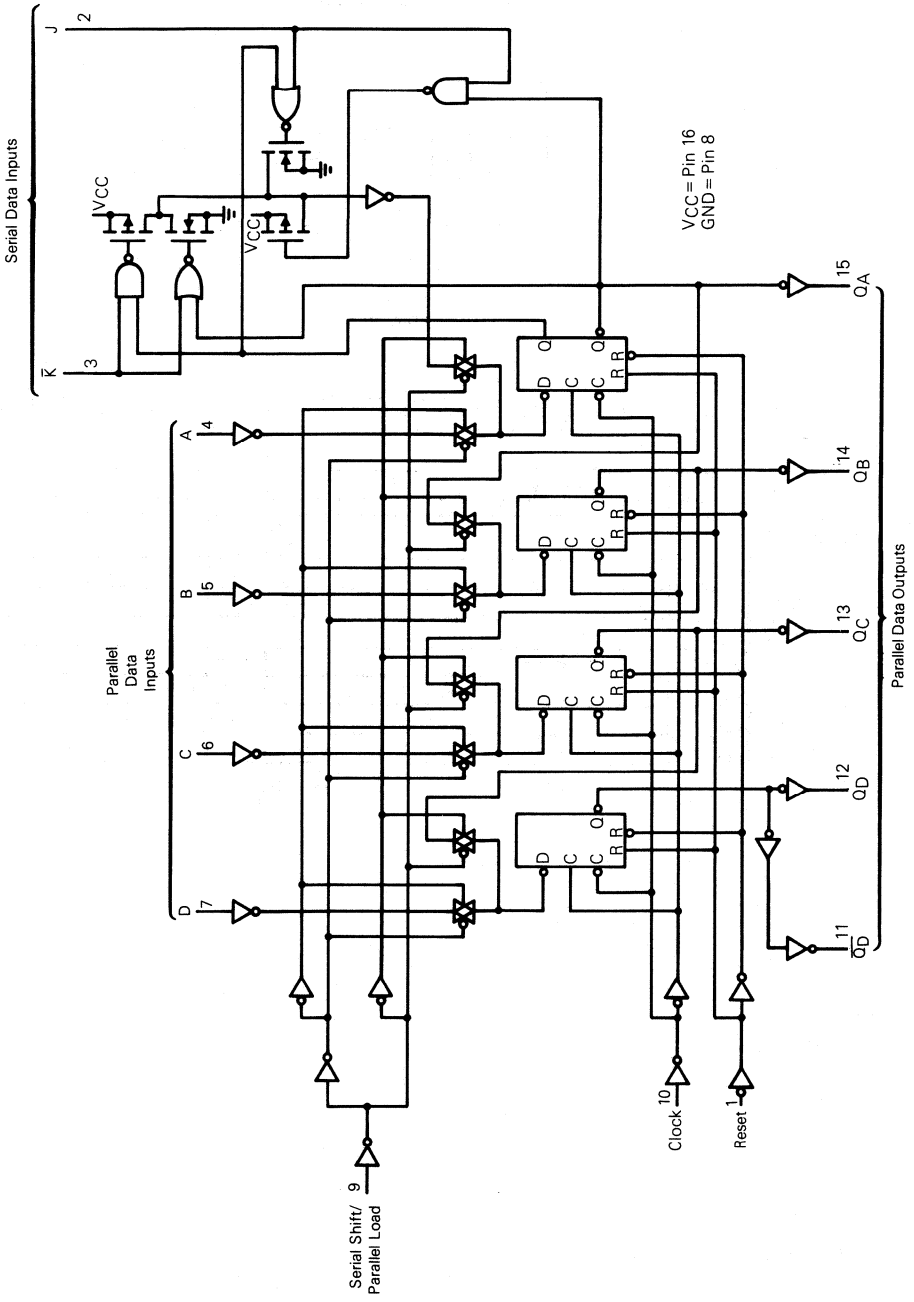
LOGIC DIAGRAM



MOTOROLA

MC54/74HC221

Product Preview

DUAL MONOSTABLE MULTIVIBRATOR

The MC54/74HC221 is identical in pinout to the LS221. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

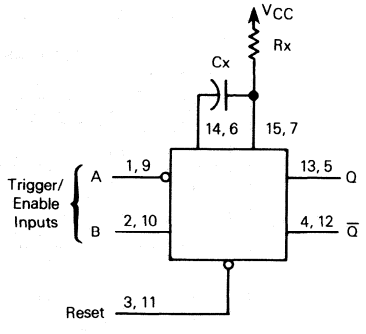
Each multivibrator features an active-low asynchronous reset and both negative- and positive-edge triggered inputs, either of which can be used as an enable. The device may also be triggered by using the Reset pin. The output pulse width is dependent upon an external resistor and capacitor connection as shown in the block diagram.

The HC221 has the same pinout as the HC123 and the HC423 monostable multivibrators. The HC123, however, is retriggerable and the HC423 may not be triggered by using the Reset pin.

If more pulse-width accuracy is required, use the MC54/74HC4538 Precision Monostable Multivibrator.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

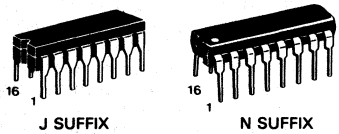
BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL MONOSTABLE MULTIVIBRATOR



J SUFFIX
CERAMIC PACKAGE
CASE 620

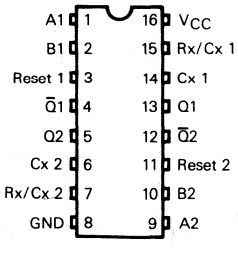
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs	
A	B	Reset	Q	Q̄
X	X	L	L	H
H	X	H	L	H
X	L	H	L	H
L	↓	H	⊓	⊔
↘	H	H	⊓	⊔
L	H	↓	⊓	⊔

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MOTOROLA

MC54/74HC237

Advance Information

1-OF-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

The MC54/74HC237 is identical in pinout to the LS137, but has noninverting outputs. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

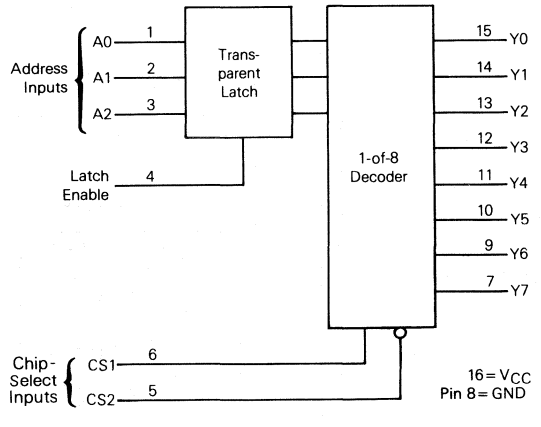
The HC237 decodes a three-bit Address to one-of-eight active-high outputs. The device has a transparent latch for storage of the Address. Two Chip Selects, one active-low and one active-high, are provided to facilitate the demultiplexing, cascading, and chip-selecting functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the other one active.

The HC237 is the noninverting version of the HC137.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

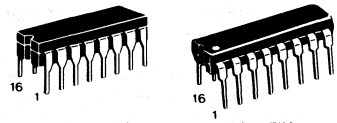
BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

1-OF-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH



J SUFFIX
CERAMIC PACKAGE
CASE 620

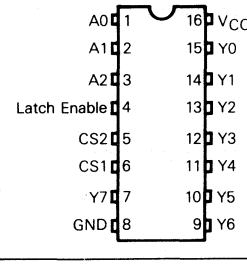
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

PIN ASSIGNMENT



TRUTH TABLE

Inputs						Outputs							
LE	CS1	CS2	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	*							

* = Depends upon the Address previously applied while LE was at a logic low.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 2)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A to Output Y	20	41	ns
t_{PHL}	(Figures 1 and 6)	16	32	
t_{PLH}	Maximum Propagation Delay, CS2 to Output Y	16	35	ns
t_{PHL}	(Figures 2 and 6)	13	25	
t_{PLH}	Maximum Propagation Delay, CS1 to Output Y	16	35	ns
t_{PHL}	(Figures 3 and 6)	14	27	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Output Y	22	44	ns
t_{PHL}	(Figures 4 and 6)	17	33	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 6)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 6)	2.0	118	235	296	350	ns
		4.5	24	47	59	70	
		6.0	20	40	50	60	
t_{PHL}		2.0	93	185	233	276	ns
		4.5	19	37	47	55	
		6.0	16	31	40	47	
t_{PLH}	Maximum Propagation Delay, CS2 to Output Y (Figures 2 and 6)	2.0	100	200	252	298	ns
		4.5	20	40	50	60	
		6.0	17	34	43	51	
t_{PHL}		2.0	73	145	183	216	ns
		4.5	15	29	37	43	
		6.0	12	25	31	37	
t_{PLH}	Maximum Propagation Delay, CS1 to Output Y (Figures 3 and 6)	2.0	100	200	252	298	ns
		4.5	20	40	50	60	
		6.0	17	34	43	51	
t_{PHL}		2.0	80	160	202	238	ns
		4.5	16	32	40	48	
		6.0	14	27	34	41	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Output Y (Figures 4 and 6)	2.0	125	250	315	373	ns
		4.5	25	50	63	75	
		6.0	21	43	54	63	
t_{PHL}		2.0	95	190	239	283	ns
		4.5	19	38	48	57	
		6.0	16	32	41	48	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 6)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*			–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
			Typical	Guaranteed Limit			
t_{su}	Minimum Setup Time, Input A to Latch Enable (Figure 5)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Latch Enable to Input A (Figure 5)	2.0	25	50	63	75	ns
		4.5	5	10	13	15	
		6.0	4	9	11	13	
t_w	Minimum Pulse Width, Latch Enable (Figure 4)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 2)	–	1000	500	500	500	ns

PIN DESCRIPTIONS

INPUTS

A0, A1, A2 (PINS 1, 2, 3) – Address inputs. These inputs, when the chip is enabled, determine which of the eight outputs is selected.

CONTROL INPUTS

CS1, CS2 (PINS 6, 5) – Chip select inputs. For CS1 at a logic high and CS2 at a logic low, the chip is enabled and the outputs will follow the data inputs (Latch Enable = L). For any other combination of CS1 and CS2, the outputs will be at a logic low.

LATCH ENABLE (PIN 4) – Latch-Enable input. A logic high at this input latches the Address. A logic low at this input allows the outputs to follow the Address (CS1 = H and CS2 = L).

OUTPUTS

Y0-Y7 – Active-high outputs. One of these eight outputs is selected when the chip is enabled (CS1 = H and CS2 = L) and the Address inputs correspond to that particular output. The selected output is at a logic high while all others remain at a logic low.

SWITCHING WAVEFORMS

FIGURE 1

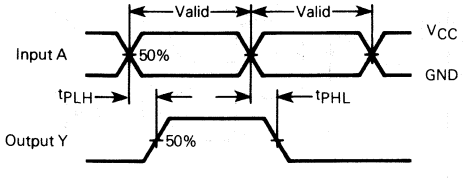


FIGURE 2

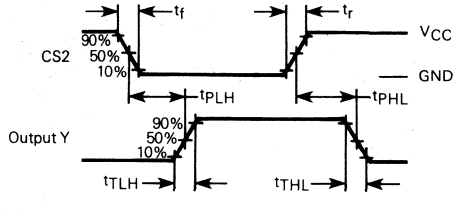


FIGURE 3

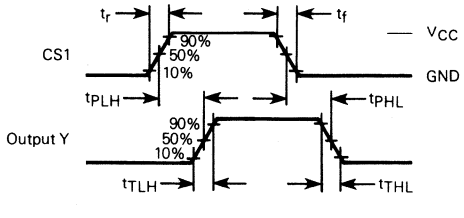


FIGURE 4

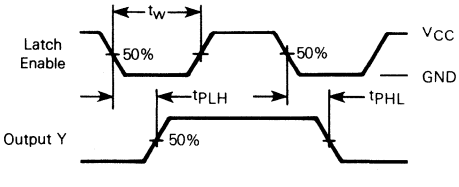


FIGURE 5

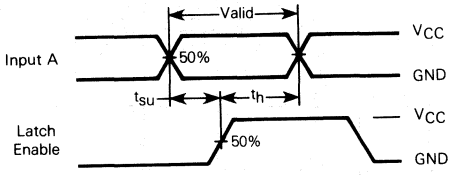
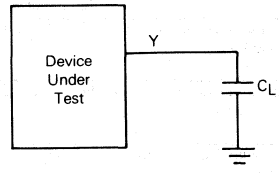
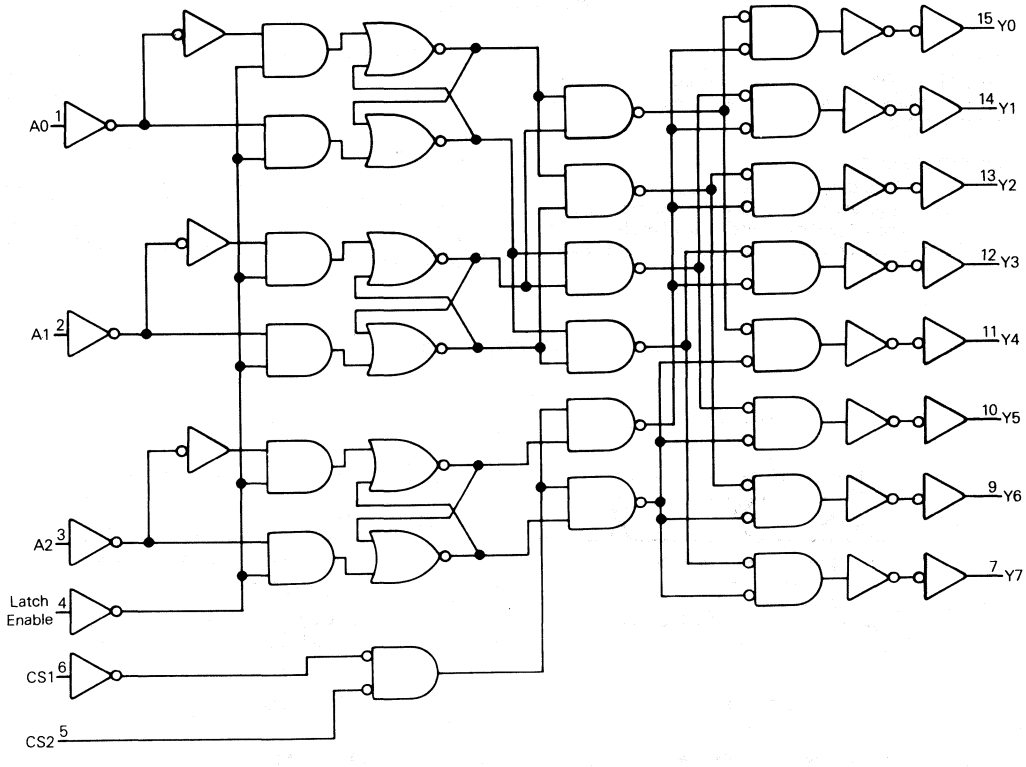


FIGURE 6



LOGIC DIAGRAM



5

MOTOROLA

MC54/74HC240

Advance Information

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/ LINE RECEIVER

The MC54/74HC240 is identical in pinout to the LS240. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

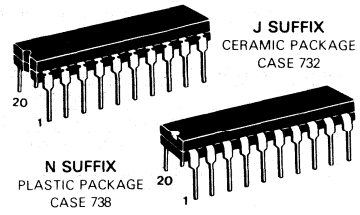
This octal inverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has inverting outputs and two active-low output enables.

The HC240 is similar in function to the HC241 and HC244.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/ LINE RECEIVER



J SUFFIX
CERAMIC PACKAGE
CASE 732

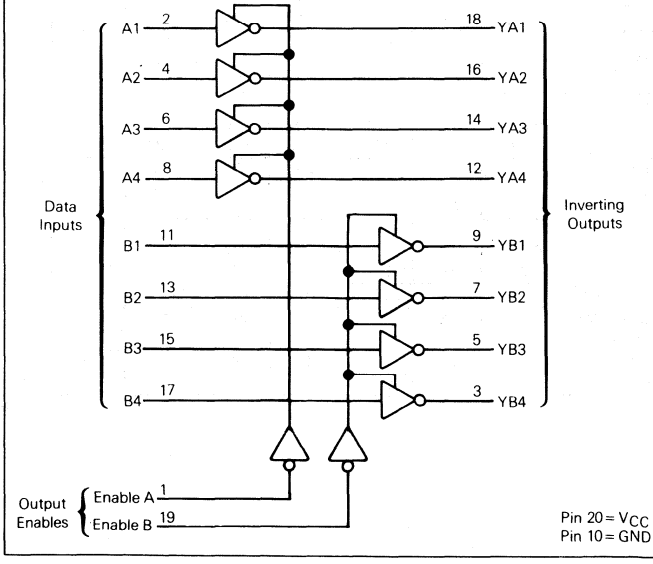
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

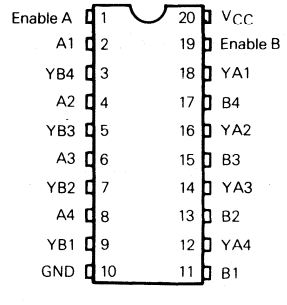
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	H
L	H	L
H	X	Z

Z = High Impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, A to YA or B to YB	C_L = 50 pF	10	18	ns
t_{PHL}	(Figures 1 and 3)		10	18	
t_{PLZ}	Maximum Propagation Delay, Output Enable to YA or YB	C_L = 5 pF	11	25	ns
t_{PHZ}	(Figures 2 and 4)		14	25	
t_{PZL}	Maximum Propagation Delay, Output Enable to YA or YB	C_L = 50 pF	11	28	ns
t_{PZH}	(Figures 2 and 4)		13	28	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L = 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	C_L = 50 pF	2.0	50	100	126	149	ns
		C_L = 150 pF		75	150	189	224	
		C_L = 50 pF	4.5	10	20	25	30	
		C_L = 150 pF		15	30	38	45	
		C_L = 50 pF	6.0	9	17	21	25	
		C_L = 150 pF		13	26	32	38	
t_{PHL}		C_L = 50 pF	2.0	50	100	126	149	ns
		C_L = 150 pF		75	150	189	224	
		C_L = 50 pF	4.5	10	20	25	30	
		C_L = 150 pF		15	30	38	45	
		C_L = 50 pF	6.0	9	17	21	25	
		C_L = 150 pF		13	26	32	38	
t_{PLZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	C_L = 50 pF	2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PHZ}			2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PZL}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{PZH}		C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L = 50 pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{out}	Three-State Output Capacitance (Output Enable = V_{CC})		–	7.5	15	15	15	pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (per Buffer)		–	50	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, B1, B2, B3, B4 (Pins 2, 4, 6, 8, 11, 13, 15, 17) — Data input pins. Data on these pins appear in inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

Enable A, Enable B (Pins 1, 19) — Output enables (active low). When a low voltage is applied to these pins, the outputs are enabled and the devices function as inverters. When a high voltage is applied, the outputs assume the high-impedance state.

OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (Pins 18, 16, 14, 12, 9, 7, 5, 3) — Device outputs. Depending upon the state of the output-enable pins, these outputs are either inverting outputs or high-impedance outputs.

SWITCHING WAVEFORMS

FIGURE 1

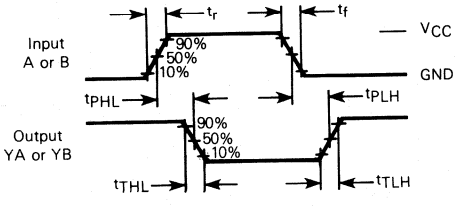


FIGURE 2

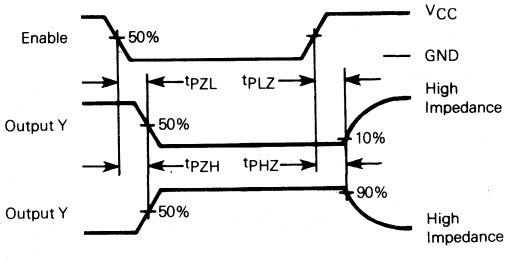


FIGURE 3 — TEST CIRCUIT

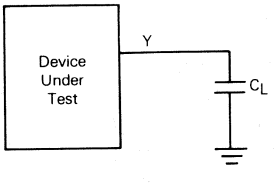
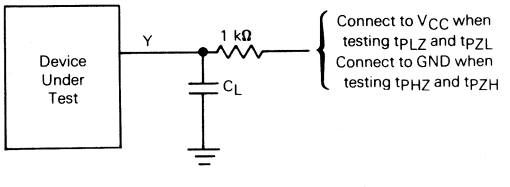


FIGURE 4 — TEST CIRCUIT



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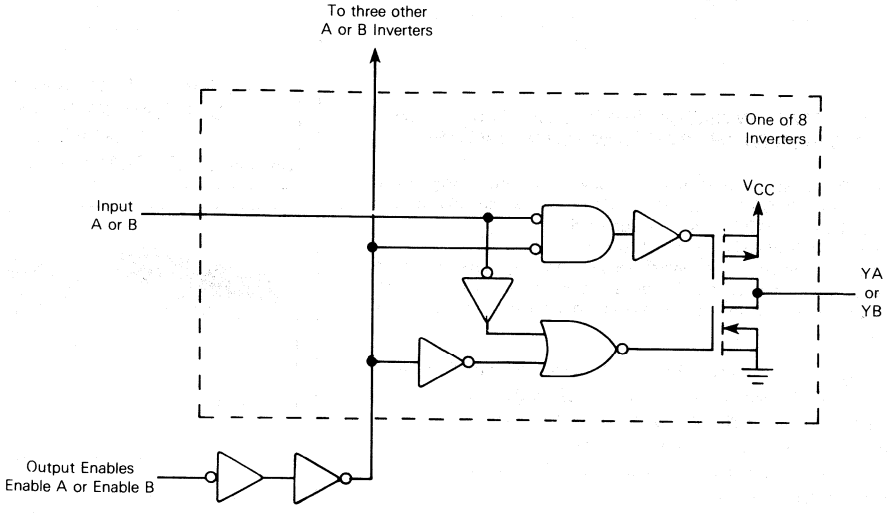
FUNCTION DIAGRAM



MOTOROLA

MC54/74HCT240

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/ LINE RECEIVER (WITH LSTTL-COMPATIBLE INPUTS)

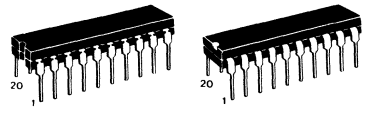
OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/ LINE RECEIVER (WITH LSTTL-COMPATIBLE INPUTS)

The HCT240 may be used as a level converter for interfacing LSTTL to High-Speed CMOS. The inputs of HCT devices are compatible with both LSTTL and CMOS output voltage levels.

The HCT240 is identical in pinout to the LS240.

This octal inverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has inverting outputs and two active-low output enables.

- Compatible with LSTTL Outputs — No Pullup Resistor Required
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Voltage Range: 4.5 to 5.5 Volts
- Low Quiescent Current Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 732

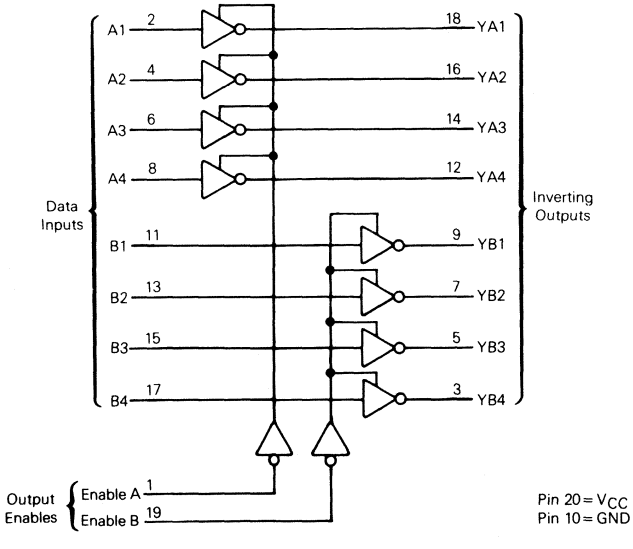
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

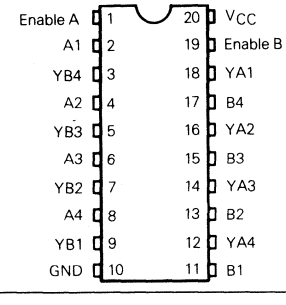
54 Series: −55°C to +125°C
MC54HCTXXXJ (Ceramic Package Only

74 Series: −40°C to +85°C
MC74HCTXXXN (Plastic Package)
MC74HCTXXXJ (Ceramic Package)

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	H
L	H	L
H	X	Z

Z = High Impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

MC54/74HC241

Advance Information

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/ LINE RECEIVER

The MC54/74HC241 is identical in pinout to the LS241. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

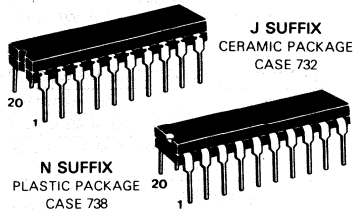
This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has noninverting outputs with one active-low output enable ("A" buffers) and one active-high output enable ("B" buffers).

The HC241 is similar in function to the HC240 and HC244.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER



J SUFFIX
CERAMIC PACKAGE
CASE 732

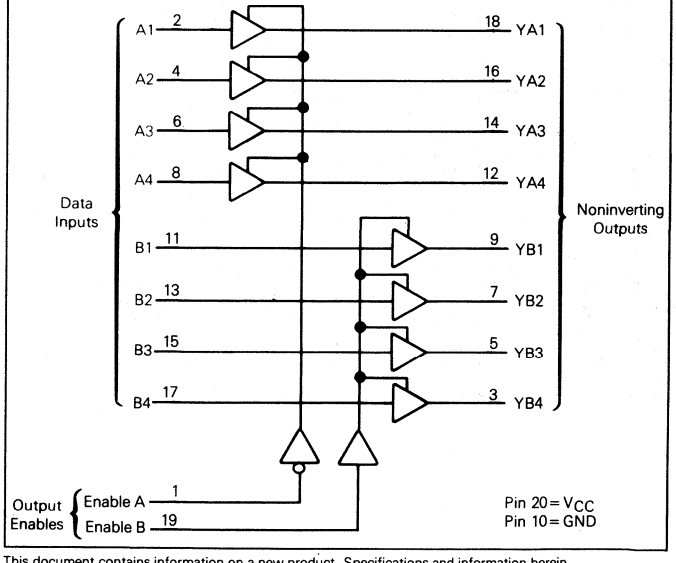
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

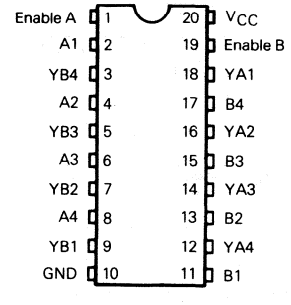
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output	Inputs		Output
Enable A	A	YA	Enable B	B	YB
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

Z = High Impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

5

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, A to YA or B to YB	C_L = 50 pF		20	ns
t_{PHL}	(Figures 1 and 3)			20	
t_{PLZ}	Maximum Propagation Delay, Output Enable to YA or YB	C_L = 5 pF		25	ns
t_{PHZ}	(Figures 2 and 4)			25	
t_{PZL}	Maximum Propagation Delay, Output Enable to YA or YB	C_L = 50 pF		28	ns
t_{PZH}	(Figures 2 and 4)			28	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L = 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	C_L = 50 pF	2.0	58	115	145	171	ns
		C_L = 150 pF		83	165	208	246	
		C_L = 50 pF	4.5	12	23	29	34	
		C_L = 150 pF		17	33	42	49	
		C_L = 50 pF	6.0	10	20	25	29	
		C_L = 150 pF		14	28	35	42	
t_{PHL}		C_L = 50 pF	2.0	58	115	145	171	ns
		C_L = 150 pF		83	165	208	246	
		C_L = 50 pF	4.5	12	23	29	34	
		C_L = 150 pF		17	33	42	49	
		C_L = 50 pF	6.0	10	20	25	29	
		C_L = 150 pF		14	28	35	42	
t_{PLZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	C_L = 50 pF	2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PHZ}			2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PZL}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{PZH}		C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L = 50 pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{out}	Three-State Output Capacitance (Output Enable = V_{CC})		–	7.5	15	15	15	pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (per Buffer)		–	50	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, B1, B2, B3, B4 (Pins 2, 4, 6, 8, 11, 13, 15, 17) — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs when the outputs are enabled.

CONTROLS

Enable A (Pin 1) — Output enable (active low). When a low voltage is applied to this pin, the outputs of the "A" devices are enabled and the devices function as noninverting buffers. When a high voltage is applied, the outputs assume the high-impedance state.

Enable B (Pin 19) — Output enable (active high). When a high voltage is applied to this pin, these outputs of the "B" devices are enable and the devices function as noninverting buffers. When a low voltage is applied, the outputs assume the high-impedance state.

OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (Pins 18, 16, 14, 12, 9, 7, 5, 3) — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high-impedance outputs.

SWITCHING WAVEFORMS

FIGURE 1

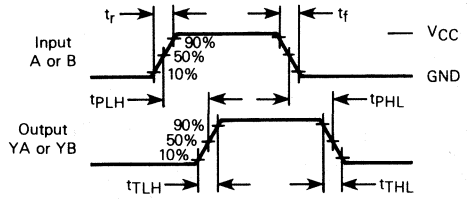


FIGURE 2

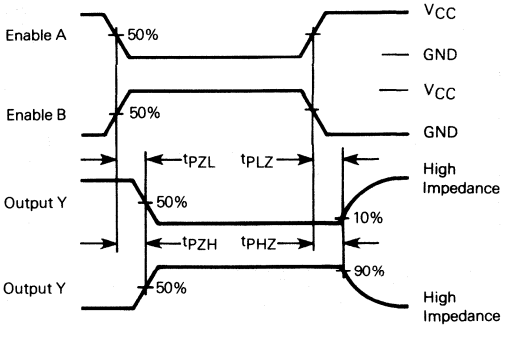


FIGURE 3 — TEST CIRCUIT

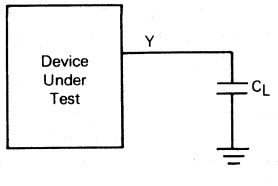
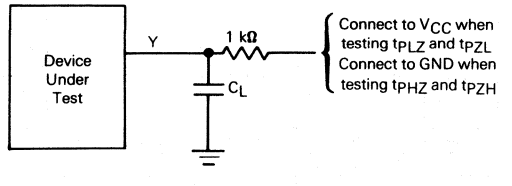


FIGURE 4 — TEST CIRCUIT



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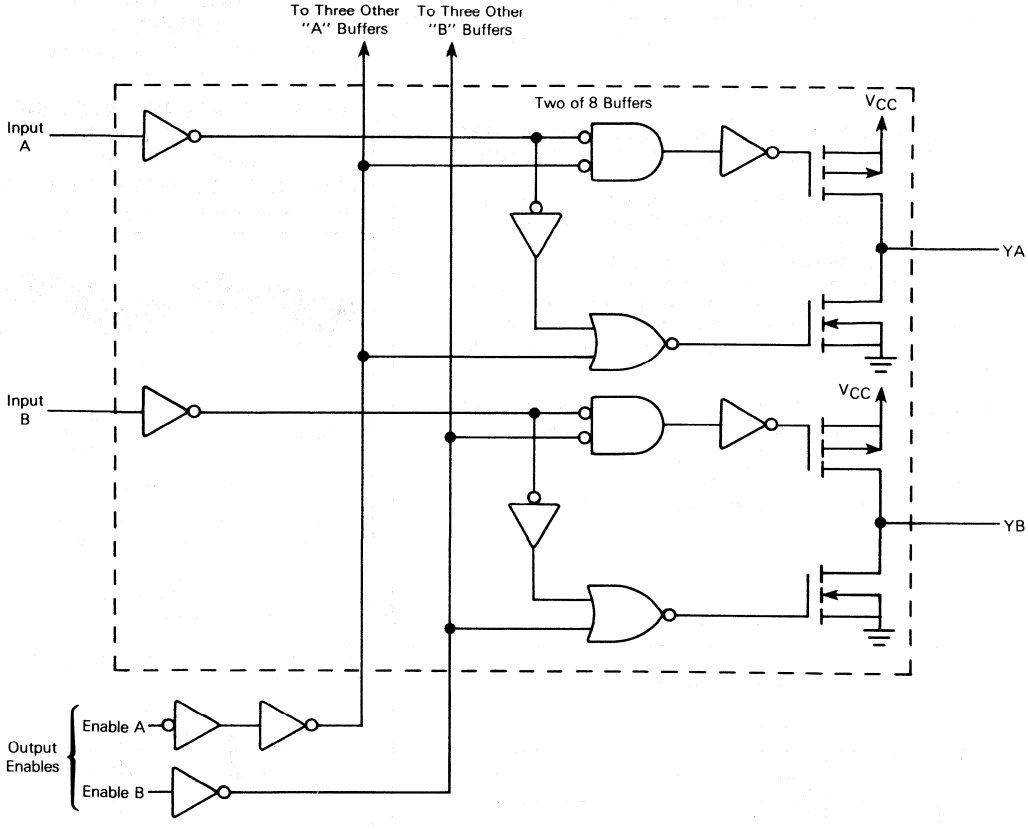
FUNCTION DIAGRAM



MOTOROLA

MC54/74HCT241

Product Preview

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/ LINE RECEIVER (WITH LSTTL-COMPATIBLE INPUTS)

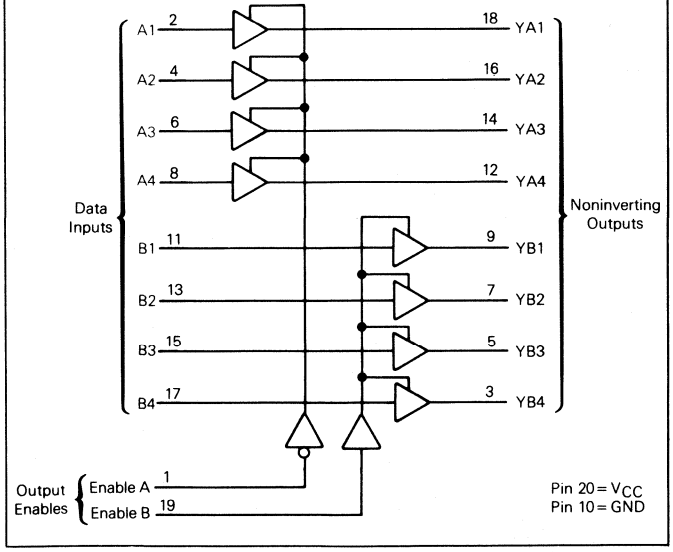
The HCT241 may be used as a level converter for interfacing LSTTL to High-Speed CMOS. The inputs of HCT devices are compatible with both LSTTL and CMOS output voltage levels.

The HCT241 is identical in pinout to the LS241.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has noninverting outputs with one active-low output enable ("A" buffers) and one active-high output enable ("B" buffers).

- Compatible with LSTTL Outputs — No Pullup Resistor Required
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Voltage Range: 4.5 to 5.5 Volts
- Low Quiescent Current Characteristic of CMOS Devices
- Diode Protection on All Inputs

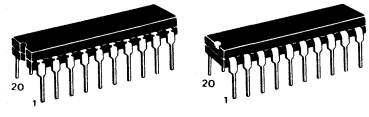
LOGIC DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/ LINE RECEIVER (WITH LSTTL-COMPATIBLE INPUTS)



J SUFFIX
CERAMIC PACKAGE
CASE 732

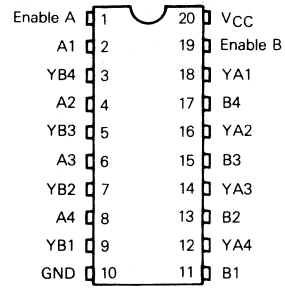
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCTXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCTXXXN (Plastic Package)
MC74HCTXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output	Inputs		Output
Enable A	A	YA	Enable B	B	YB
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

Z = High Impedance

MOTOROLA

MC54/74HC242
MC54/74HC243

Advance Information

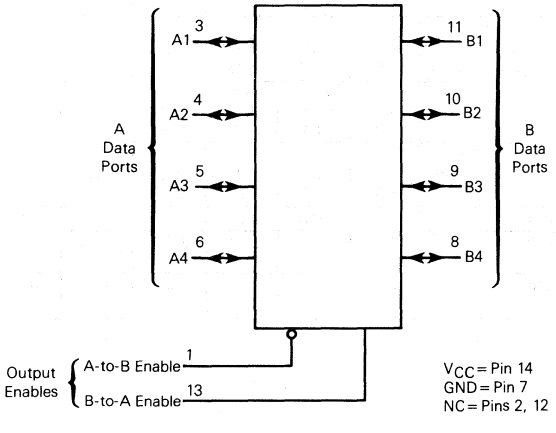
QUAD 3-STATE BUS TRANSCEIVERS

The MC54/74HC242 and MC54/74HC243 are identical in pinout to the LS242 and LS243. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These quad bus transceivers are designed for asynchronous two-way communications between data buses. The states of the Output Enables (A-to-B Enable and B-to-A Enable) determine both the direction of data flow (from A to B or from B to A) and the modes of the Data Ports (input, output, or high-impedance).

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

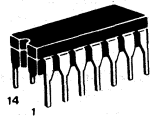
BLOCK DIAGRAM
HC242—Inverting Outputs
HC243—Noninverting Outputs



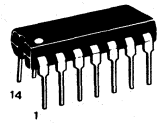
This document contains information on a new product. Specifications and information herein are subject to change without notice.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD 3-STATE BUS TRANSCEIVERS



J SUFFIX
CERAMIC PACKAGE
CASE 632



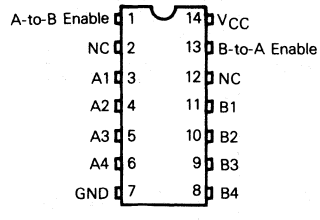
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



NC = no connection

FUNCTION TABLE

Control Inputs		MC54/74HC242 Data Port Status		MC54/74HC243 Data Port Status	
A-to-B Enable	B-to-A Enable	A	B	A	B
H	H	$\overline{O}$	I	O	I
L	H	Z	Z	Z	Z
H	L	Z	Z	Z	Z
L	L	I	$\overline{O}$	I	O

I = Input, O = Output, $\overline{O}$ = Inverting Output,
Z = High Impedance

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C 54HC and 74HC		85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed			Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} or V_{IL} V_{out}=V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, A to B/B to A		10	18	ns
t_{PHL}	(Figures 1 and 3)	C_L = 50 pF	10	18	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Output A or B		9	25	ns
t_{PHZ}	(Figures 2 and 4)	C_L = 5 pF	11	25	
t_{PZL}	Maximum Propagation Delay, Output Enable to Output A or B		15	28	ns
t_{PZH}	(Figures 2 and 4)	C_L = 50 pF	17	28	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L = 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, A to B/B to A (Figures 1 and 3)	C_L = 50 pF	2.0	50	100	126	149	ns
		C_L = 150 pF		75	150	189	224	
		C_L = 50 pF	4.5	10	20	25	30	
		C_L = 150 pF		15	30	38	45	
		C_L = 50 pF	6.0	9	17	21	25	
		C_L = 150 pF		13	26	32	38	
t_{PHL}		C_L = 50 pF	2.0	50	100	126	149	ns
		C_L = 150 pF		75	150	189	224	
		C_L = 50 pF	4.5	10	20	25	30	
		C_L = 150 pF		15	30	38	45	
		C_L = 50 pF	6.0	9	17	21	25	
		C_L = 150 pF		13	26	32	38	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Output A or B (Figures 2 and 4)	C_L = 50 pF	2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PHZ}			2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PZL}	Maximum Propagation Delay, Output Enable to Output A or B (Figures 2 and 4)	C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{PZH}		C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L = 50 pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{out}	Three-State Output Capacitance (Output Enable = V_{CC} or GND)		–	7.5	15	15	15	pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (per Transceiver)		–	50	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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FUNCTION DESCRIPTIONS

DATA PORTS

A1, A2, A3, A4 (Pins 3, 4, 5, 6) and B1, B2, B3, B4 (Pins 11, 10, 9, 8) — Data on these pins may be transferred between data buses. Depending upon the states of the Output Enables, these pins may be inputs, outputs, or open circuits (high-impedance).

CONTROL INPUTS

A-to-B Enable (Pin 1) and B-to-A Enable (Pin 13) — Data on these Output Enables determine both the direction of data flow (from A to B or from B to A) and the states of the outputs (standard or high impedance), according to the Function Table.

SWITCHING WAVEFORMS

FIGURE 1a — HC242

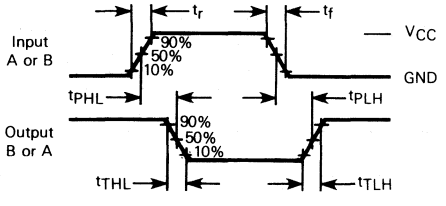


FIGURE 1b — HC243

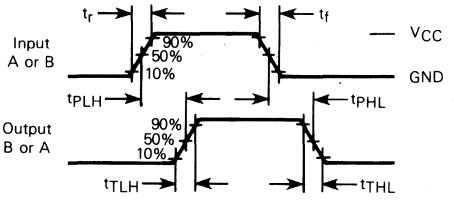


FIGURE 2

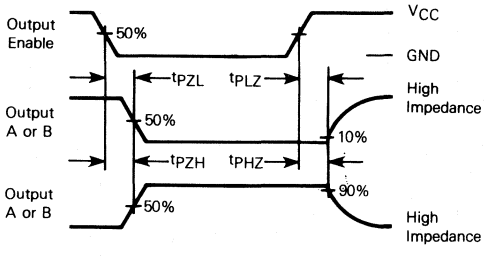


FIGURE 3 — TEST CIRCUIT

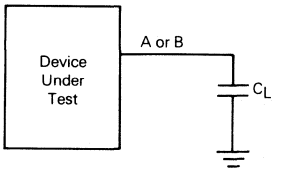
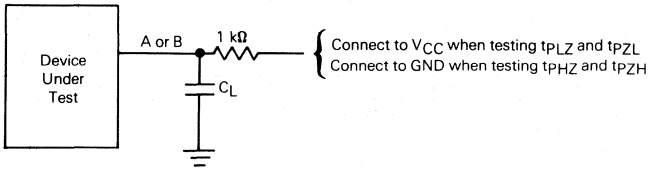


FIGURE 4 — TEST CIRCUIT



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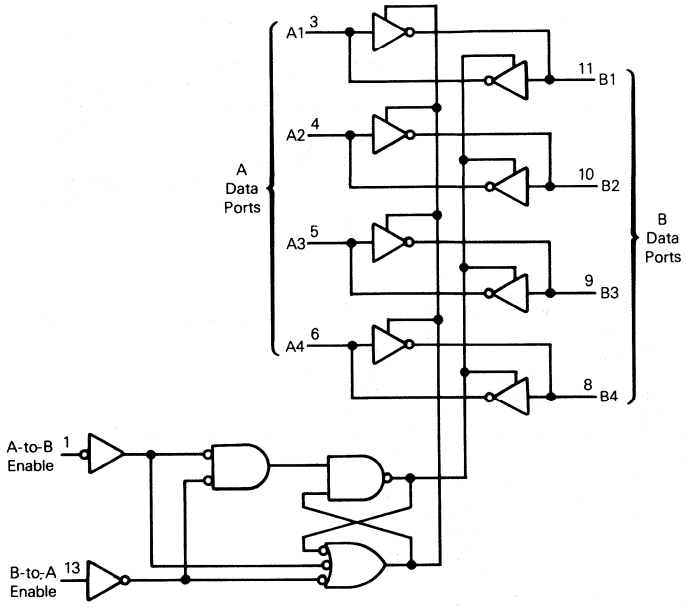
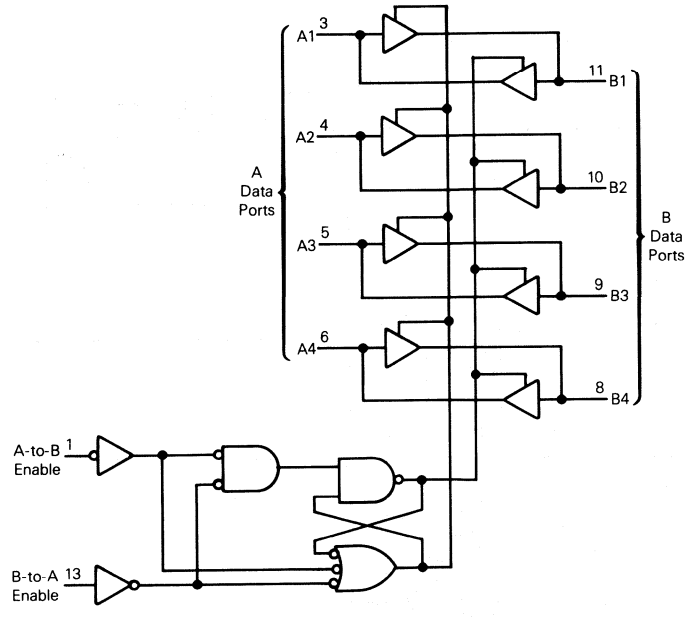
FUNCTION DIAGRAM
HC242

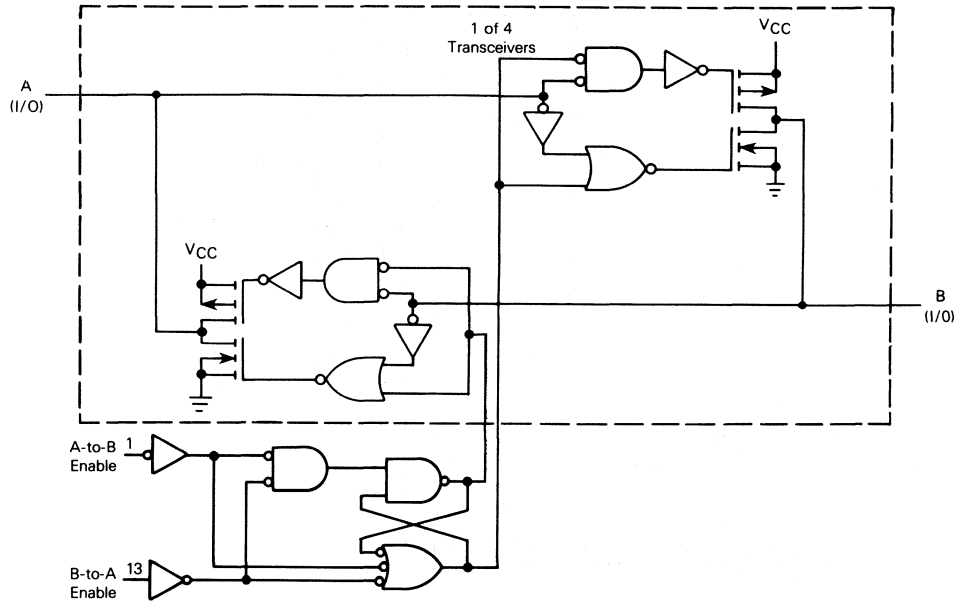


FUNCTION DIAGRAM
HC243

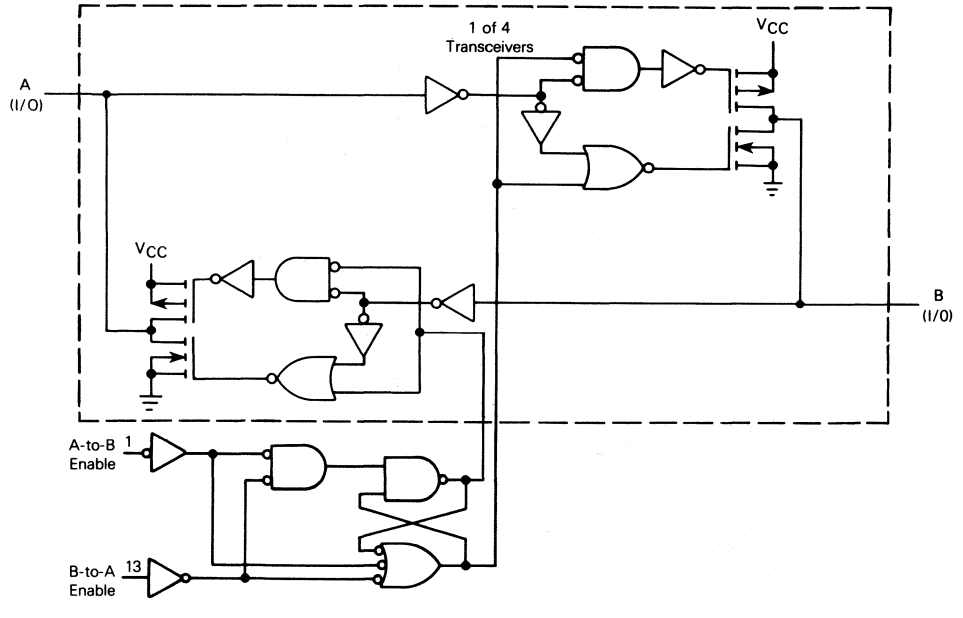


5

LOGIC DIAGRAM HC242



LOGIC DIAGRAM HC243



5

MOTOROLA

MC54/74HC244

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

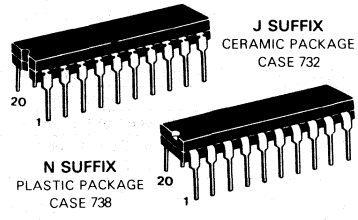
OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/ LINE RECEIVER

The MC54/74HC244 is identical in pinout to the LS244. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has noninverting outputs and two active-low output enables.

The HC244 is similar in function to the HC240 and HC241.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 732

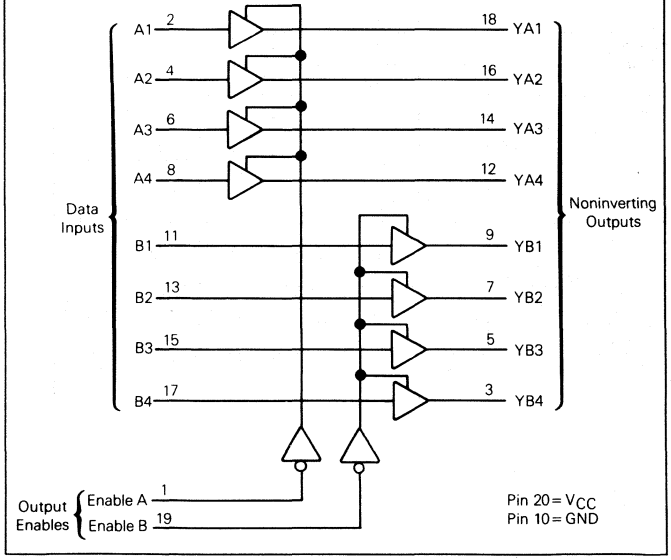
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

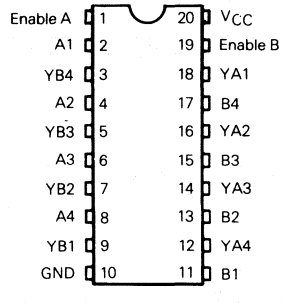
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

Z = High Impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

5

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C 54HC and 74HC		85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed			Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, A to YA or B to YB	C_L = 50 pF		20	ns
t_{PHL}	(Figures 1 and 3)			20	
t_{PLZ}	Maximum Propagation Delay, Output Enable to YA or YB	C_L = 5 pF		25	ns
t_{PHZ}	(Figures 2 and 4)			25	
t_{PZL}	Maximum Propagation Delay, Output Enable to YA or YB	C_L = 50 pF		28	ns
t_{PZH}	(Figures 2 and 4)			28	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L = 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	C_L = 50 pF	2.0	58	115	145	171	ns
		C_L = 150 pF		83	165	208	246	
		C_L = 50 pF	4.5	12	23	29	34	
		C_L = 150 pF		17	33	42	49	
		C_L = 50 pF	6.0	10	20	25	29	
		C_L = 150 pF		14	28	35	42	
t_{PHL}		C_L = 50 pF	2.0	58	115	145	171	
		C_L = 150 pF		83	165	208	246	
		C_L = 50 pF	4.5	12	23	29	34	
		C_L = 150 pF		17	33	42	49	
		C_L = 50 pF	6.0	10	20	25	29	
		C_L = 150 pF		14	28	35	42	
t_{PLZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	C_L = 50 pF	2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PHZ}			2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PZL}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{PZH}		C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L = 50 pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{in}	Maximum Input Capacitance		–	5	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output Enable = V_{CC})		–	7.5	15	15	15	pF
C_{PD}	Power Dissipation Capacitance* (per Buffer)		–	50	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, B1, B2, B3, B4 (Pins 2, 4, 6, 8, 11, 13, 15, 17) — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

Enable A, Enable B (Pins 1, 19) — Output enables (active low). When a low voltage is applied to these pins, the outputs are enabled and the devices function as noninverting buffers. When a high voltage is applied, the outputs assume the high-impedance state.

OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (Pins 18, 16, 14, 12, 9, 7, 5, 3) — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high-impedance outputs.

SWITCHING WAVEFORMS

FIGURE 1

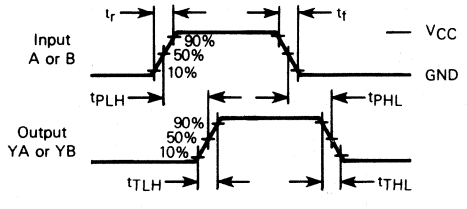


FIGURE 2

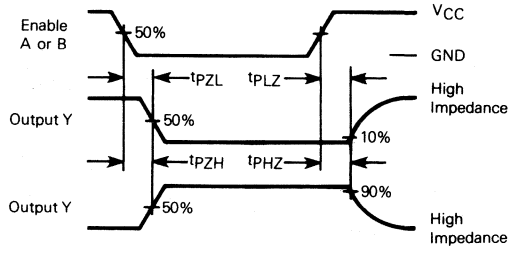


FIGURE 3 — TEST CIRCUIT

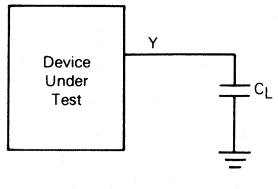
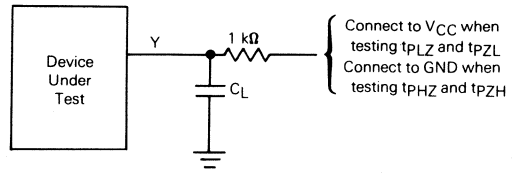


FIGURE 4 — TEST CIRCUIT



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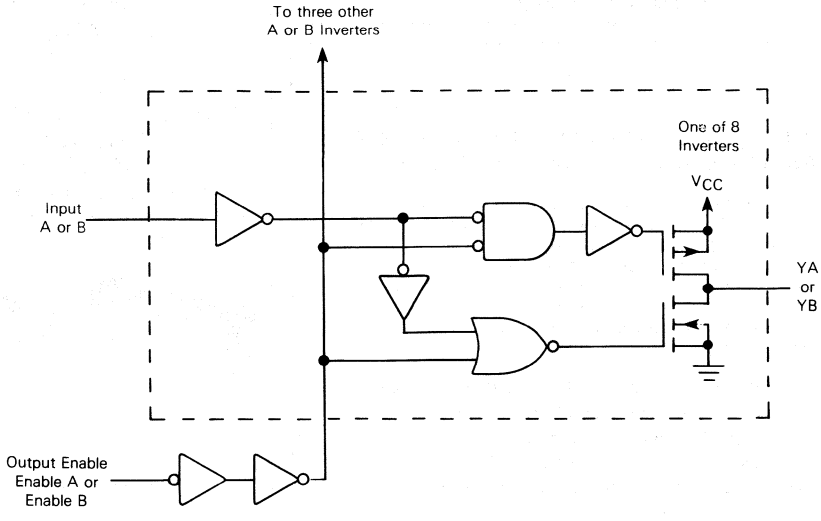
FUNCTION DIAGRAM



MOTOROLA

MC54/74HCT244

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/ LINE RECEIVER (WITH LSTTL-COMPATIBLE INPUTS)

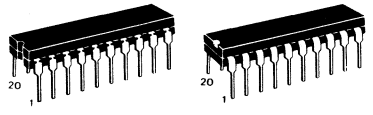
OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/ LINE RECEIVER (WITH LSTTL-COMPATIBLE INPUTS)

The HCT244 may be used as a level converter for interfacing LSTTL to High-Speed CMOS. The inputs of HCT devices are compatible with both LSTTL and CMOS output voltage levels.

The HCT244 is identical in pinout to the LS244.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has noninverting outputs and two active-low output enables.

- Compatible with LSTTL Outputs — No Pullup Resistor Required
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Voltage Range: 4.5 to 5.5 Volts
- Low Quiescent Current Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 732

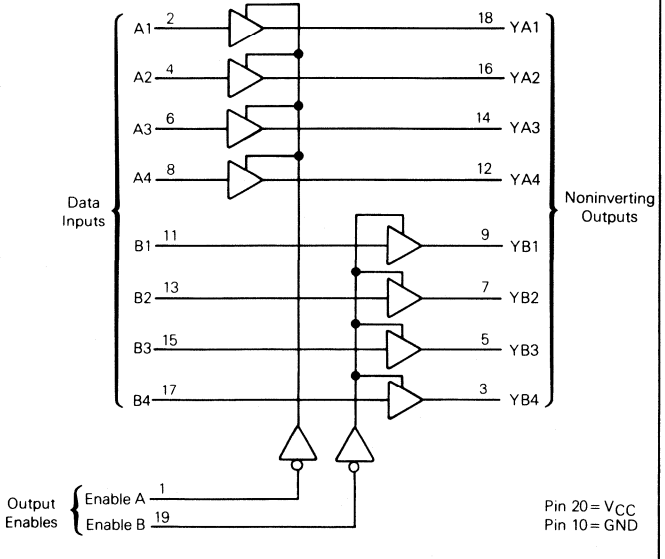
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

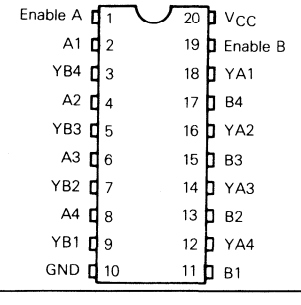
54 Series: −55°C to +125°C
MC54HCTXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCTXXXN (Plastic Package)
MC74HCTXXXJ (Ceramic Package)

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

Z = High Impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

5

MOTOROLA

MC54/74HC245

Product Preview

OCTAL 3-STATE, NONINVERTING BUS TRANSCEIVER

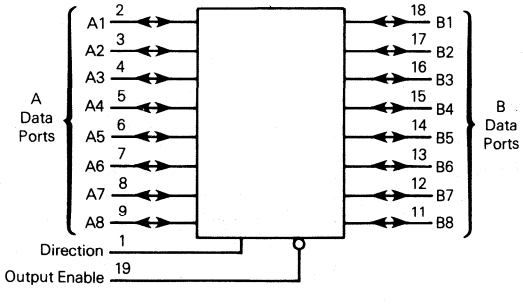
The MC54/74HC245 is identical in pinout to the LS245. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC245 is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HC245 performs functions similar to those of the HC640 and the HC643.

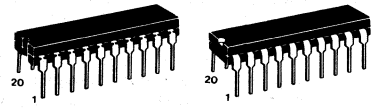
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM



HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE, NONINVERTING BUS TRANSCEIVER



J SUFFIX
CERAMIC PACKAGE
CASE 732

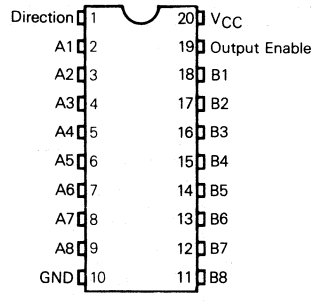
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs		
Output Enable	Direction	Operation
L	L	Data transmitted from Bus B to Bus A
L	H	Data transmitted from Bus A to Bus B
H	X	Buses Isolated (High-Impedance State)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

5

MOTOROLA

MC54/74HCT245

Product Preview

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER (WITH LSTTL-COMPATIBLE INPUTS)

The MC54/74HCT245 may be used as a level converter for interfacing LSTTL to High-Speed CMOS. The inputs of HCT devices are compatible with both LSTTL and CMOS output voltage levels. Therefore, no pullup resistors are required at the inputs of the HCT245 when interfacing with LSTTL.

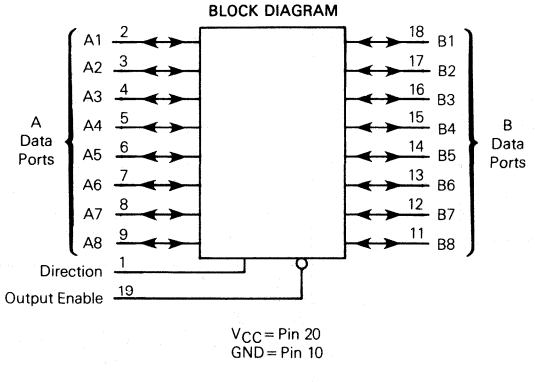
The HCT245 is identical in pinout to the LS245.

The HCT245 is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HCT245 performs functions similar to those of the HC640 and the HC643.

- Compatible with LSTTL Outputs — No Pullup Resistor Required
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Voltage Range: 4.5 to 5.5 Volts
- Low Quiescent Current Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM

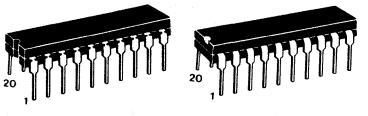


V_{CC} = Pin 20
GND = Pin 10

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER (WITH LSTTL-COMPATIBLE INPUTS)



J SUFFIX
CERAMIC PACKAGE
CASE 732

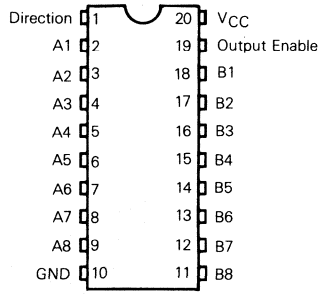
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCTXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCTXXXN (Plastic Package)
MC74HCTXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs		
Enable	Direction	Operation
L	L	Data transmitted from Bus B to Bus A
L	H	Data transmitted from Bus A to Bus B
H	X	Buses Isolated (High-Impedance State)

X = don't care

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MOTOROLA

MC54/74HC251

Advance Information

8-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

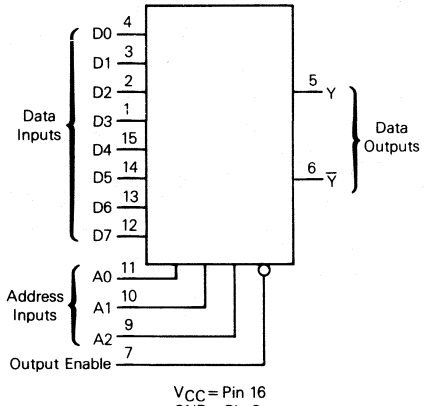
The MC54/74HC251 is identical in pinout to the LS251. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Output Enable pin must be a low logic level for the selected data to appear at the outputs. If Output Enable is high, both the Y and the Y outputs are in the high-impedance state. This 3-state feature allows the HC251 to be used in bus-oriented systems.

The HC251 is similar in function to the HC151 which does not have 3-state outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs
- Selects One of Eight Binary Data Sources
- 3-State Capability
- May Be Used In Parallel-to-Serial Conversion

BLOCK DIAGRAM

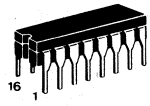


V_{CC} = Pin 16
GND = Pin 8

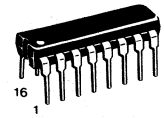
This document contains information on a new product. Specifications and information herein are subject to change without notice.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

8-INPUT DATA SELECTOR/ MULTIPLEXER WITH 3-STATE OUTPUTS



J SUFFIX
CERAMIC PACKAGE
CASE 620



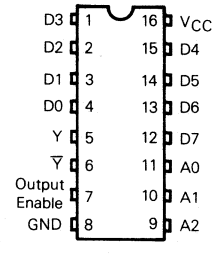
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs	
A2	A1	A0	Output Enable	Y	$\overline{Y}$
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

Z = high-impedance state
D0, D1. . .D7 = the level of the respective D input

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±25	mA
I_{out}	DC Output Current, per Pin	±50	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

5

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input D to Output Y	C_L = 15 pF	22	29	ns
t_{PHL}	(Figures 1 and 5)		22	29	
t_{PLH}	Maximum Propagation Delay, Input D to Output $\overline{Y}$	C_L = 15 pF	24	32	ns
t_{PHL}	(Figures 2 and 5)		24	32	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y	C_L = 15pF	26	35	ns
t_{PHL}	(Figures 3 and 5)		26	35	
t_{PLH}	Maximum Propagation Delay, Input A to Output $\overline{Y}$	C_L = 15 pF	27	35	ns
t_{PHL}	(Figures 3 and 5)		27	35	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Output Y	C_L = 5 pF	27	35	ns
t_{PHZ}	(Figures 4 and 6)		27	35	
t_{PZL}	Maximum Propagation Delay, Output Enable to Output Y	C_L = 15 pF	19	26	ns
t_{PZH}	(Figures 4 and 6)		19	26	
t_{PLZ}	Maximum Propagation Delay, Output Enable to $\overline{Y}$	C_L = 5 pF	26	40	ns
t_{PHZ}	(Figures 4 and 6)		26	40	
t_{PZL}	Maximum Propagation Delay, Output Enable to $\overline{Y}$	C_L = 15 pF	19	27	ns
t_{PZH}	(Figures 4 and 6)		19	27	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	C_L = 15 pF	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input D to Output Y (Figures 1 and 5)	2.0	70	195	244	283	ns
		4.5	27	39	49	57	
		6.0	23	33	41	48	
t_{PHL}		2.0	70	195	244	283	ns
		4.5	27	39	49	57	
		6.0	23	33	41	48	
t_{PLH}	Maximum Propagation Delay, Input D to Output $\overline{Y}$ (Figures 2 and 5)	2.0	75	185	231	268	ns
		4.5	29	37	46	54	
		6.0	25	32	40	46	
t_{PHL}		2.0	75	185	231	268	ns
		4.5	29	37	46	54	
		6.0	25	32	40	46	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 3 and 5)	2.0	90	205	256	300	ns
		4.5	31	41	51	60	
		6.0	26	35	44	51	
t_{PHL}		2.0	90	205	256	300	ns
		4.5	31	41	51	60	
		6.0	26	35	44	51	
t_{PLH}	Maximum Propagation Delay, Input A to Output $\overline{Y}$ (Figures 3 and 5)	2.0	95	205	256	300	ns
		4.5	32	41	51	60	
		6.0	27	35	44	51	
t_{PHL}		2.0	95	205	256	300	ns
		4.5	32	41	51	60	
		6.0	27	35	44	51	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 4 and 6)	2.0	60	195	244	283	ns
		4.5	30	39	49	57	
		6.0	26	33	41	48	
t_{PHZ}		2.0	60	195	244	283	ns
		4.5	30	39	49	57	
		6.0	26	33	41	48	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns) (Continued)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{PZL}	Maximum Propagation Delay, Output Enable to Output Y (Figures 4 and 6)	2.0	45	145	181	210	ns
		4.5	21	29	36	42	
		6.0	18	25	31	36	
t_{PZH}		2.0	45	145	181	210	ns
		4.5	21	29	36	42	
		6.0	18	25	31	36	
t_{PLZ}	Maximum Propagation Delay, Output Enable to $\overline{Y}$ (Figures 4 and 6)	2.0	60	220	275	319	ns
		4.5	29	44	55	64	
		6.0	25	37	46	54	
t_{PHZ}		2.0	60	220	275	319	ns
		4.5	29	44	55	64	
		6.0	25	37	46	54	
t_{PZL}	Maximum Propagation Delay, Output Enable to $\overline{Y}$ (Figures 4 and 6)	2.0	45	150	188	218	ns
		4.5	21	30	38	44	
		6.0	18	26	33	38	
t_{PZH}		2.0	45	150	188	218	ns
		4.5	21	30	38	44	
		6.0	18	26	33	38	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Input Capacitance	–	5	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output Enable = V_{CC})	–	7.5	15	15	15	pF
C_{PD}	Power Dissipation Capacitance*	–	110	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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PIN DESCRIPTIONS

INPUTS

D0, D1,. . .,D7 (PINS 4, 3, 2, 1, 15, 14, 13, 12) – Data inputs. Data on one of these eight binary inputs may be selected to appear on the output.

CONTROL INPUTS

A0, A1, A2 (PINS 11, 10, 9) – Address inputs. The data on these pins are the binary address of the selected input (see the Function Table).

OUTPUT ENABLE (PIN 7) – Output Enable. This input pin must be at a low logic level for the selected data to appear at the outputs. If the Output Enable pin is high, both the Y and $\overline{Y}$ outputs are taken to the high-impedance state.

OUTPUTS

Y, $\overline{Y}$ (PINS 5, 6) – Data outputs. The selected data is presented at these pins in both true (Y output) and complemented ($\overline{Y}$ output) forms.

SWITCHING WAVEFORMS

FIGURE 1

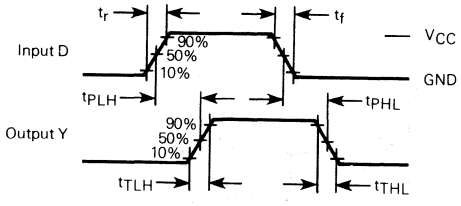


FIGURE 2

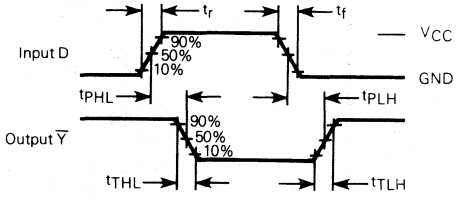


FIGURE 3

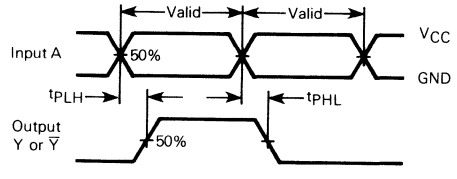


FIGURE 4

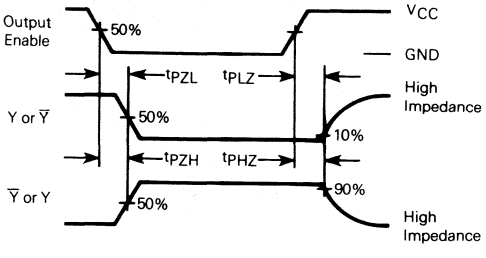


FIGURE 5 — TEST CIRCUIT

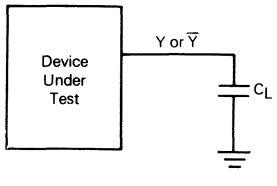
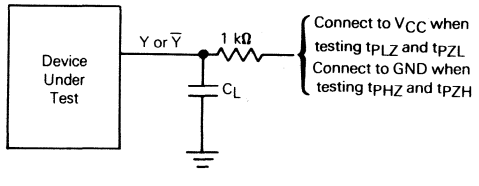


FIGURE 6 — TEST CIRCUIT



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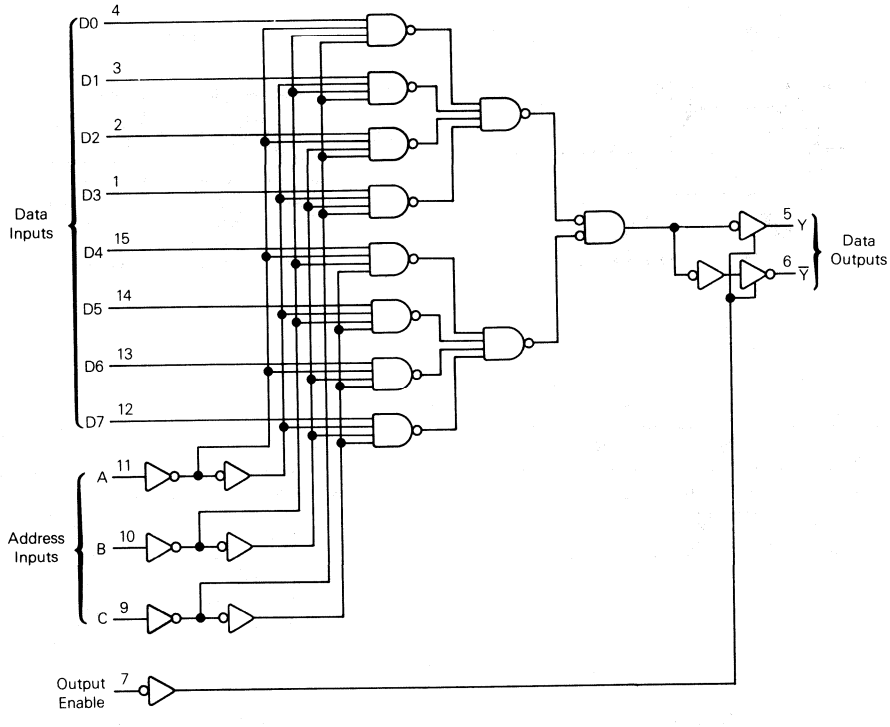
LOGIC DIAGRAM



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MOTOROLA

MC54/74HC253

Advance Information

DUAL 4-INPUT DATA SELECTOR/MULTIPLEXER WITH THREE-STATE OUTPUTS

The MC54/74HC253 is identical in pinout to the LS253. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The Address inputs select one of four Data inputs from each multiplexer. Each multiplexer has an active low Three-State Output Enable control and a three-state noninverting output.

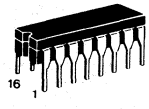
The HC253 is similar in function to the HC153 which does not have 3-state outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

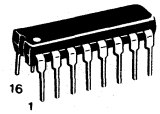
HIGH-PERFORMANCE CMOS

LOW-POWER COMPLEMENTARY MOS SILICON-GATE

DUAL 4-INPUT DATA SELECTOR/MULTIPLEXER WITH THREE-STATE OUTPUTS



J SUFFIX
CERAMIC PACKAGE
CASE 620



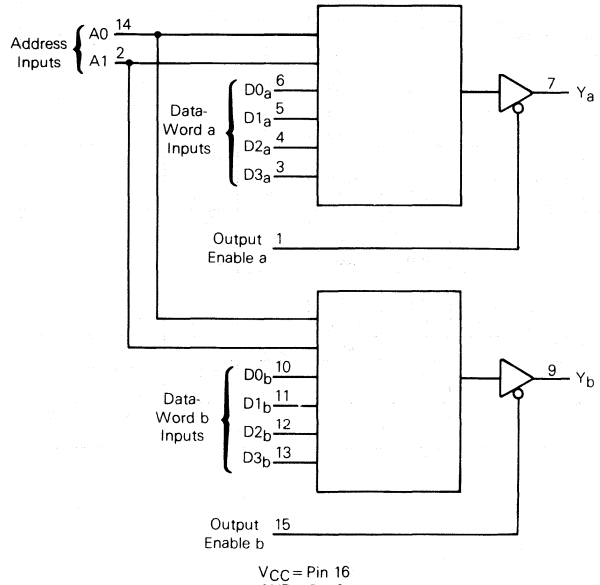
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

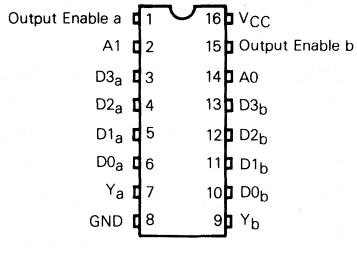
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
A1	A0	Output Enable	Y
X	X	H	Z
L	L	L	D0
L	H	L	D1
H	L	L	D2
H	H	L	D3

D0, D1, D2, and D3 = the level of the respective Data Inputs

Z = high-impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Data to Output Y	C_L = 15 pF	18	23	ns
t_{PHL}	(Figures 1 and 4)		18	23	
t_{PLH}	Maximum Propagation Delay, Address to Output Y	C_L = 15 pF	24	30	ns
t_{PHL}	(Figures 1 and 4)		24	30	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Output Y	C_L = 5 pF	15	27	ns
t_{PHZ}	(Figures 2 and 3)		15	27	
t_{PZL}		C_L = 15 pF	11	18	ns
t_{PZH}			11	18	
t_{TLH}, t_{THL}	Maximum Output Transition Times (Figures 1 and 4)	C_L = 15 pF	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{PLH}	Maximum Propagation Delay, Data to Output Y	2.0	99	126	158	189	ns
	(Figures 1 and 4)	4.5	22	28	35	42	
		6.0	19	23	29	35	
t_{PHL}		2.0	99	126	158	189	ns
		4.5	22	28	35	42	
		6.0	19	23	29	35	
t_{PLH}	Maximum Propagation Delay, Address to Output Y	2.0	131	158	198	237	ns
	(Figures 1 and 4)	4.5	29	35	44	53	
		6.0	24	30	38	45	
t_{PHL}		2.0	131	158	198	237	ns
		4.5	29	35	44	53	
		6.0	24	30	38	45	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Y	2.0	90	135	169	203	ns
	(Figures 2 and 3)	4.5	20	30	38	45	
		6.0	17	25	31	38	
t_{PHZ}		2.0	90	135	169	203	ns
		4.5	20	30	38	45	
		6.0	17	25	31	38	
t_{PZL}	Maximum Propagation Delay, Output Enable to Y	2.0	63	90	113	135	ns
	(Figures 2 and 3)	4.5	14	20	25	30	
		6.0	12	17	21	26	
t_{PZH}		2.0	63	90	113	135	ns
		4.5	14	20	25	30	
		6.0	12	17	21	26	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	2.0	38	75	95	110	ns
	(Figures 1 and 4)	4.5	8	15	19	22	
		6.0	6	13	16	29	
C_{out}	Three-State Output Capacitance (Output Enable)	–	7.5	15	15	15	pF
C_{in}	Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	90	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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PIN DESCRIPTIONS

DATA INPUTS

$D0_a$-$D3_a$, $D0_b$-$D3_b$ (PINS 3, 4, 5, 6, 10, 11, 12, 13) — Data Inputs. When one of these pairs of inputs is selected and the outputs are enabled, the outputs assume the state of the respective inputs.

CONTROL INPUTS

A0, A1 (PINS 2, 14) — Address Inputs. These inputs select the pair of Data inputs to appear at the corresponding outputs.

OUTPUT ENABLE (PINS 1, 15) — Active-low three-state Output Enable. When a low logic level is applied to these inputs, the corresponding outputs are enabled. When a high logic level is applied, the outputs assume the high-impedance state.

OUTPUTS

Y_a, Y_b (PINS 7, 9) — Noninverting Device Three-State Outputs.

SWITCHING WAVEFORMS

FIGURE 1

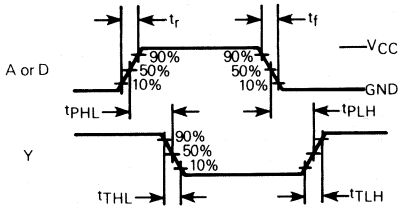


FIGURE 2

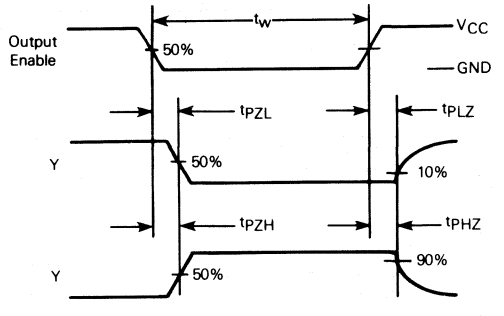


FIGURE 3 — TEST CIRCUIT

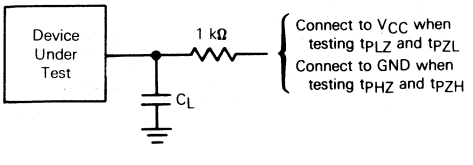
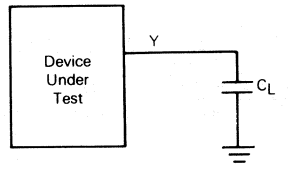


FIGURE 4 — TEST CIRCUIT



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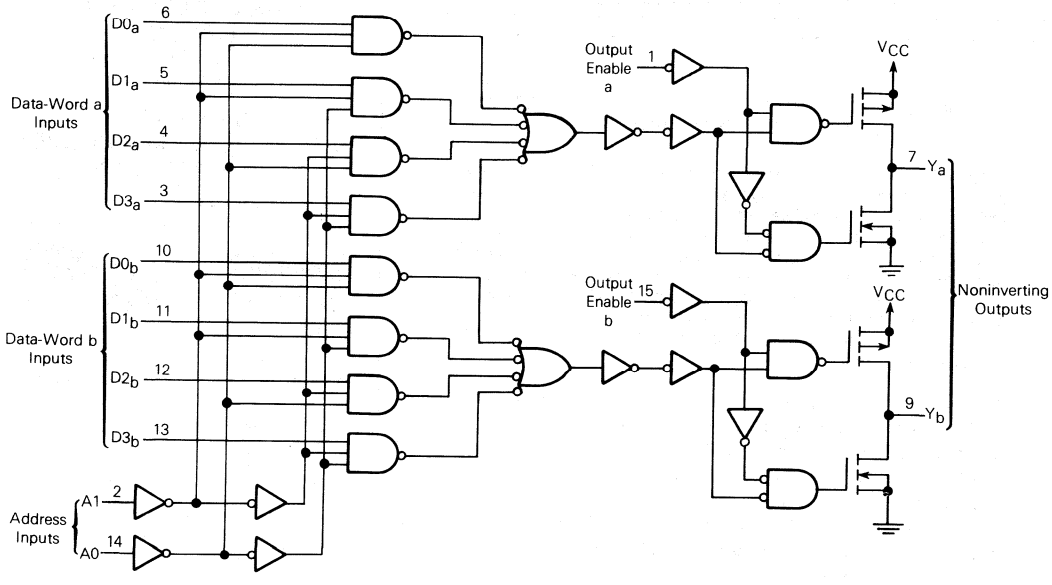
LOGIC DIAGRAM



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MOTOROLA

MC54/74HC257

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

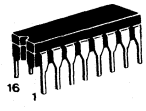
QUAD 2-INPUT DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

The MC54/74HC257 is identical in pinout to the LS257. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

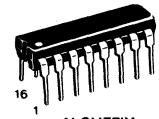
This device selects a 4-bit word from either the A or B inputs, determined by the Select input, and routes it to the outputs. The data is presented at the outputs in noninverted form when the Output Enable pin is at a logic low. A high logic level on the Output Enable pin switches the outputs into the high-impedance state.

The HC257 is similar in function to the HC157 and HC158 which do not have 3-state outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620



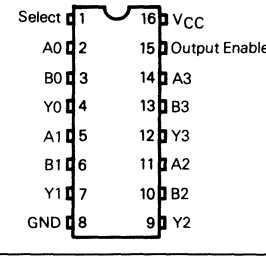
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

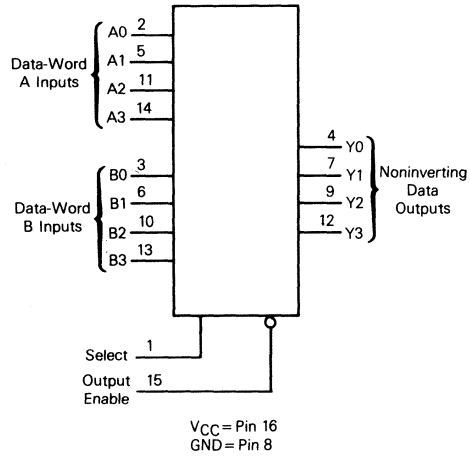
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



BLOCK DIAGRAM



FUNCTION TABLE

Inputs		Outputs
Output Enable	Select	Y0-Y3
H	X	Z
L	L	A0-A3
L	H	B0-B3

X = don't care
Z = high-impedance state
A0-A3, B0-B3 = the levels of the respective Data-Word Inputs.

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output Y	C_L = 50 pF	12	18	ns
t_{PHL}	(Figures 1 and 4)		12	18	
t_{PLH}	Maximum Propagation Delay, Select to Output Y	C_L = 50 pF	14	18	ns
t_{PHL}	(Figures 2 and 4)		14	18	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Output Y	C_L = 5 pF	10	25	ns
t_{PHZ}	(Figures 3 and 5)		10	25	
t_{PZL}	Maximum Propagation Delay, Output Enable to Output Y	C_L = 50 pF	10	28	ns
t_{PZH}	(Figures 3 and 5)		10	28	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	C_L = 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 4)	C_L = 50 pF	2.0	50	100	126	149	ns
		C_L = 150 pF		75	150	189	224	
		C_L = 50 pF	4.5	10	20	25	30	
		C_L = 150 pF		15	30	38	45	
		C_L = 50 pF	6.0	9	17	21	25	
		C_L = 150 pF		13	26	32	38	
t_{PHL}		C_L = 50 pF	2.0	50	100	126	149	ns
		C_L = 150 pF		75	150	189	224	
		C_L = 50 pF	4.5	10	20	25	30	
		C_L = 150 pF		15	30	38	45	
		C_L = 50 pF	6.0	9	17	21	25	
		C_L = 150 pF		13	26	32	38	
t_{PLH}	Maximum Propagation Delay, Select to Output Y (Figures 2 and 4)	C_L = 50 pF	2.0	50	100	126	149	ns
		C_L = 150 pF		75	150	189	224	
		C_L = 50 pF	4.5	10	20	25	30	
		C_L = 150 pF		15	30	38	45	
		C_L = 50 pF	6.0	9	17	21	25	
		C_L = 150 pF		13	26	32	38	
t_{PHL}		C_L = 50 pF	2.0	50	100	126	149	ns
		C_L = 150 pF		75	150	189	224	
		C_L = 50 pF	4.5	10	20	25	30	
		C_L = 150 pF		15	30	38	45	
		C_L = 50 pF	6.0	9	17	21	25	
		C_L = 150 pF		13	26	32	38	

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SWITCHING CHARACTERISTICS (Input $t_r = t_f = 6$ ns) (Continued)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{PLZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5)	$C_L = 50$ pF	2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PHZ}			2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PZL}	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5)	$C_L = 50$ pF	2.0	75	150	189	224	ns
		$C_L = 150$ pF		100	200	252	298	
		$C_L = 50$ pF	4.5	15	30	38	45	
		$C_L = 150$ pF		20	40	50	60	
		$C_L = 50$ pF	6.0	13	26	32	38	
		$C_L = 150$ pF		17	34	43	51	
t_{PZH}		$C_L = 50$ pF	2.0	75	150	189	224	ns
		$C_L = 150$ pF		100	200	252	298	
		$C_L = 50$ pF	4.5	15	30	38	45	
		$C_L = 150$ pF		20	40	50	60	
		$C_L = 50$ pF	6.0	13	26	32	38	
		$C_L = 150$ pF		17	34	43	51	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	$C_L = 50$ pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{in}	Maximum Input Capacitance		–	5	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output Enable = V_{CC})		–	7.5	15	15	15	pF
C_{PD}	Power Dissipation Capacitance*		–	30	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

PIN DESCRIPTIONS

INPUTS

A0, A1, A2, A3 (PINS 2, 5, 11, 14) – Data-Word A inputs. The logic data present on these pins is transferred to the outputs when the Select input is at a logic low and the Output Enable input is at a logic low. The data is presented to the outputs in noninverted form.

B0, B1, B2, B3 (PINS 3, 6, 10, 13) – Data-Word B inputs. The logic data present on these pins is transferred to the outputs when the Select input is at a logic high and the Output Enable input is at a logic low. The data is presented to the outputs in noninverted form.

OUTPUTS

Y0, Y1, Y2, Y3 (PINS 4, 7, 9, 12) – Data Outputs. The selected input data word is presented at these outputs when the Output Enable input is at a logic low. For the Output Enable input at a logic high, the outputs are switched to the high impedance state.

CONTROL INPUTS

SELECT (PIN 1) – Data-word select. This input determines the data word to be transferred to the outputs. A logic low on this input selects the A inputs and a logic high selects the B inputs.

OUTPUT ENABLE (PIN 15) – Output Enable. A logic low on this input allows the selected input data to be presented at the outputs. A logic high on this input forces the outputs into the high-impedance state.

5

SWITCHING WAVEFORMS

FIGURE 1

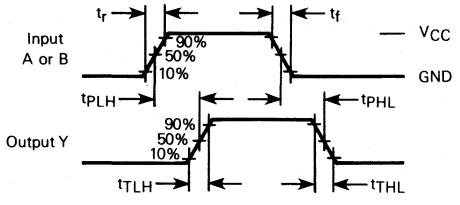


FIGURE 2

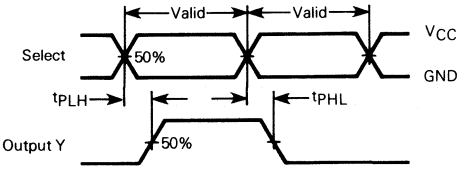


FIGURE 3

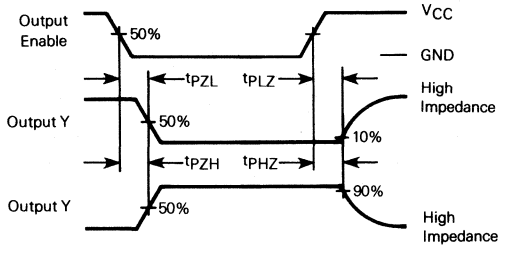


FIGURE 4 — TEST CIRCUIT

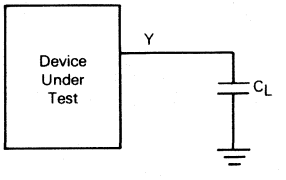
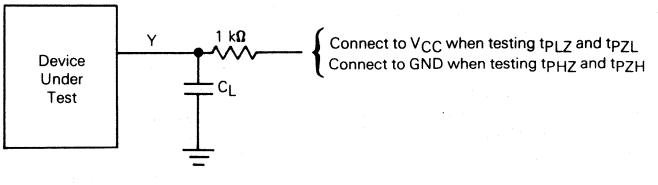


FIGURE 5 — TEST CIRCUIT



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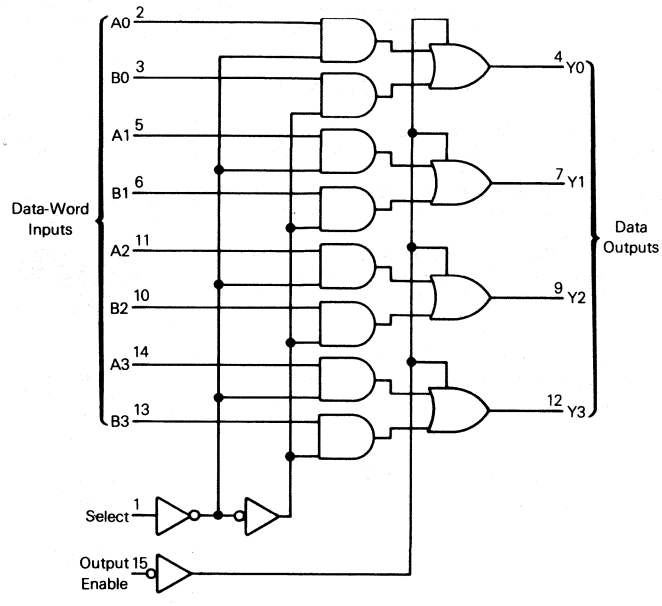
LOGIC DIAGRAM



MOTOROLA

MC54/74HC259

Product Preview

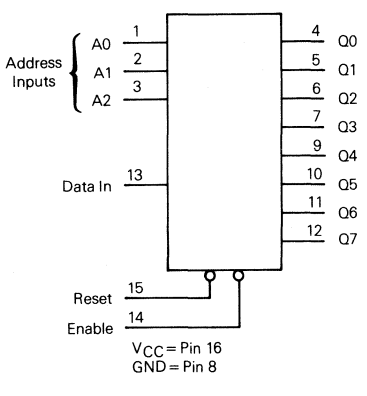
8-BIT ADDRESSABLE LATCH/1-OF-8 DECODER

The MC54/74HC259 is identical in pinout to the LS259. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This 8-Bit Addressable Latch can perform four basic functions. In the Addressable Latch mode, data is read into the addressed stage of the latch. When Enable and Reset are HIGH, the latch contents are stored regardless of any other inputs. With Enable and Reset low, the output of the addressed stage assumes the HIGH state (i.e.: 8-Line Demultiplexer). When Enable = H and Reset = L all stages are reset to the low state.

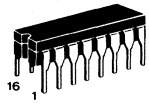
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM

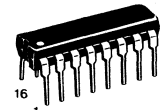


HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

8-BIT ADDRESSABLE LATCH/ 1-OF-8 DECODER



J SUFFIX
CERAMIC PACKAGE
CASE 620



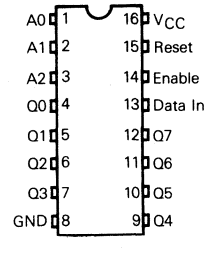
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Enable	Reset	Function
L	H	Addressable Latch
H	H	Memory
L	L	8-Line Demultiplexer
H	L	Reset

5

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

MC54/74HC266

Advance Information

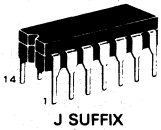
QUAD 2-INPUT EXCLUSIVE NOR GATE

The MC54/74HC266 is identical in pinout to the LS266, but does not have open-drain outputs. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

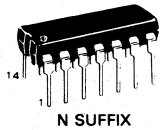
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD 2-INPUT EXCLUSIVE NOR GATE



J SUFFIX
CERAMIC PACKAGE
CASE 632

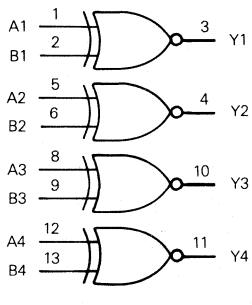


N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXJ (Ceramic Package Only)
74 Series: −40°C to +85°C
MC74HCXXN (Plastic Package)
MC74HCXXJ (Ceramic Package)

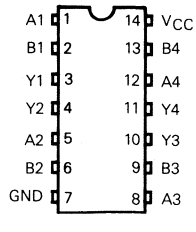
FUNCTION DIAGRAM



$Y = \overline{A \oplus B}$
$= AB + \overline{A}\,\overline{B}$

V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



TRUTH TABLE

Inputs		Outputs
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output Y	8	20	ns
t_{PHL}	(Figures 1 and 2)	9	20	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	60	120	151	179	ns
		4.5	12	24	30	36	
		6.0	10	20	26	30	
t_{PHL}		2.0	60	120	151	179	ns
		4.5	12	24	30	36	
		6.0	10	20	26	30	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	33	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption per gate:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS

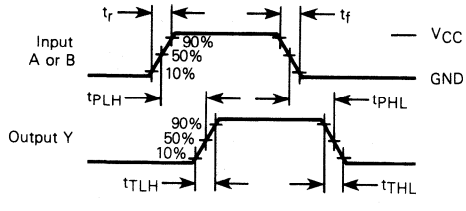
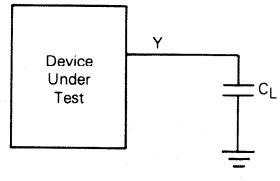
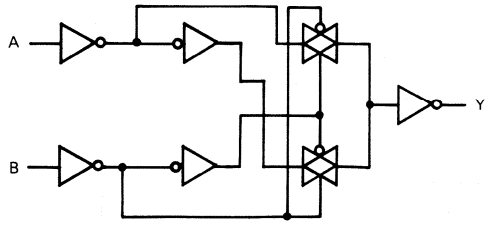


FIGURE 2 — TEST CIRCUIT



LOGIC DIAGRAM
(¼ of Device)



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MOTOROLA

MC54/74HC273

Advance Information

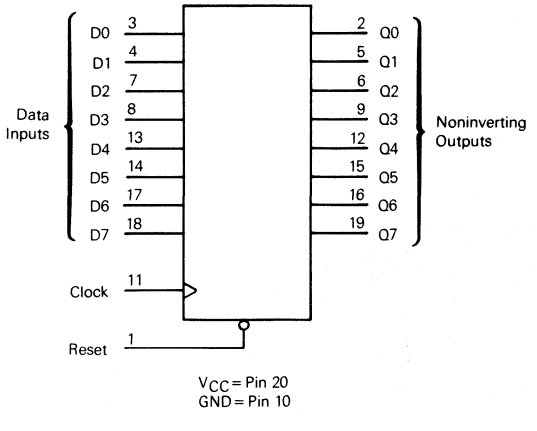
OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

The MC54/74HC273 is identical in pinout to the LS273. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The device consists of eight D-type flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active-low.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

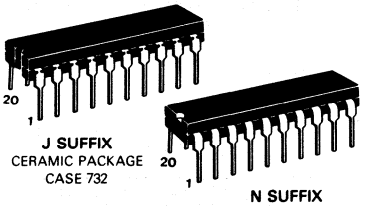
BLOCK DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET



J SUFFIX
CERAMIC PACKAGE
CASE 732

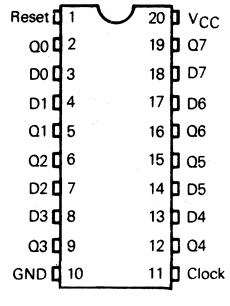
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs
Reset	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	no change
H	↓	X	no change

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)		30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q		27	ns
t_{PHL}	(Figures 1 and 4)		27	
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)		27	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	11	5	4	4	MHz
		4.5	54	27	21	18	
		6.0	64	32	25	21	
t_{PLH}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	80	160	202	238	ns
		4.5	16	32	40	48	
		6.0	14	27	34	41	
t_{PHL}		2.0	80	160	202	238	ns
		4.5	16	32	40	48	
		6.0	14	27	34	41	
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0	80	160	202	238	ns
		4.5	16	32	40	48	
		6.0	14	27	34	41	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		60	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Clock to Data (Figure 3)	2.0	−20	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−3	0	0	0	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

5

SWITCHING WAVEFORMS

FIGURE 1

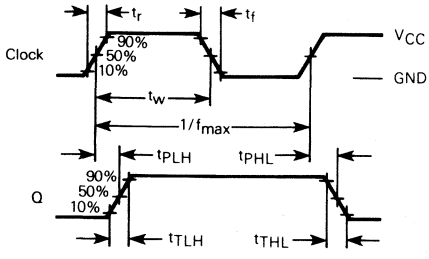


FIGURE 2

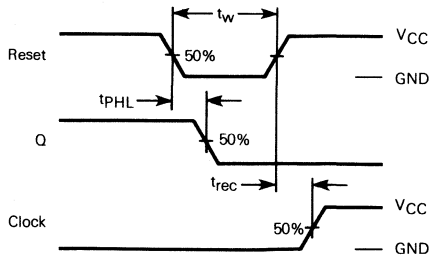


FIGURE 3

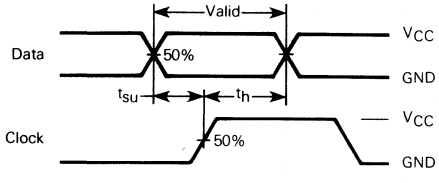
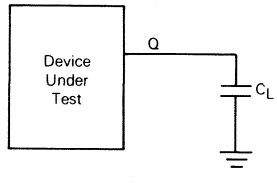


FIGURE 4 — TEST CIRCUIT



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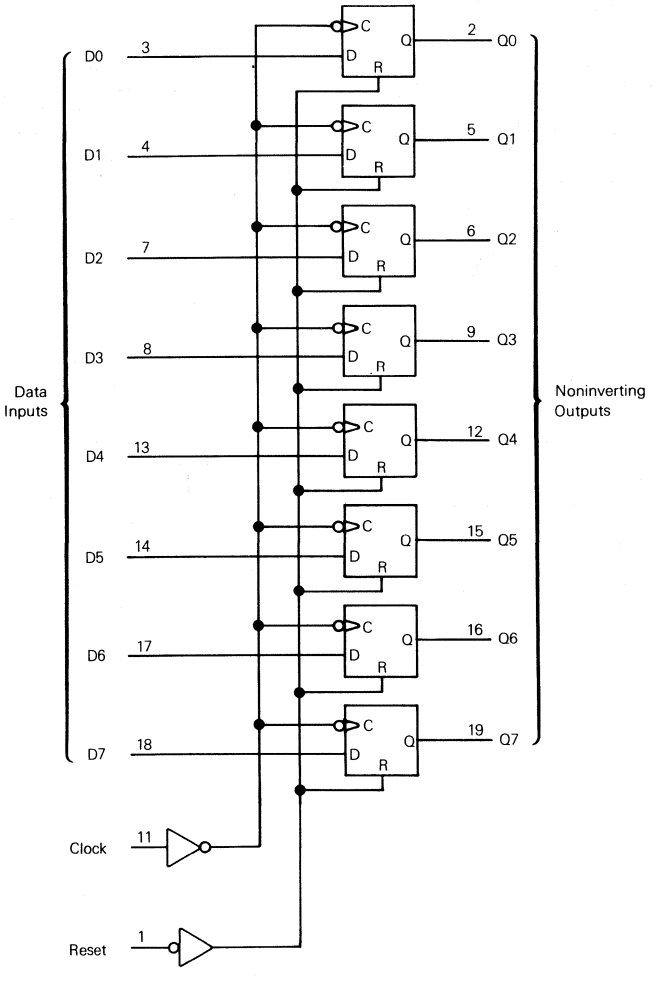
LOGIC DIAGRAM



5

MOTOROLA

MC54/74HC280

Advance Information

9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

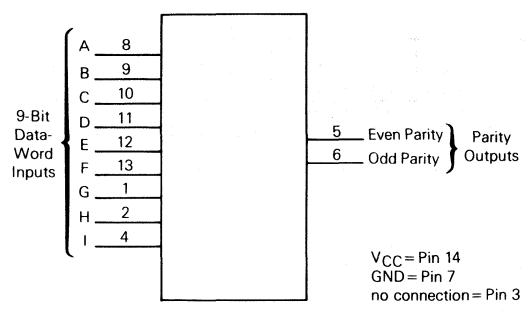
The MC54/74HC280 is identical in pinout to the LS280. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This circuit consists of 9 data-bit inputs (A through I) and 2 outputs (Even Parity and Odd Parity) to allow both odd and even parity applications. Words of greater than 9-bits can be accommodated by cascading other MC54/74HC280 devices.

This device can be used in systems utilizing the LS180 parity generator/checker. Although the HC280 does not have expander inputs, the corresponding function is provided by an input at pin 4 and the absence of any connection at pin 3. This permits the HC280 to be substituted for the LS180 to produce an identical function, even if the HC280s are mixed with existing LS180s.

- Generates Even and Odd Parity for Nine Data Inputs
- Cascadable for n Bits
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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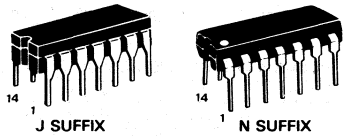
9-BIT ODD/EVEN PARITY GENERATOR/CHECKER



J SUFFIX
CERAMIC PACKAGE
CASE 632

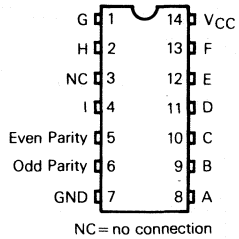
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



NC = no connection

FUNCTION TABLE

Number of Inputs A through I that are high	Outputs	
	Even Parity	Odd Parity
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \leq (V_{in}$ or $V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C 54HC and 74HC	85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed		Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Data Inputs to Parity Outputs	17	35	ns
t_{PHL}	(Figures 1 and 2)	17	35	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Data Inputs to Parity Outputs (Figures 1 and 2)	2.0	103	205	258	305	ns
		4.5	21	41	52	61	
		6.0	17	35	44	52	
t_{PHL}		2.0	103	205	258	305	ns
		4.5	21	41	52	61	
		6.0	17	35	44	52	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–		–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

PIN DESCRIPTIONS

INPUTS

A, B, C, D, E, F, G, H, I (Pins 8-13, 1, 2, 4) – Nine-bit data-word inputs. The data word placed on these pins is checked for even or odd parity.

OUTPUTS

Even Parity (Pin 5) – Even-parity output. This pin goes high if the data word has even parity and low if the data word has odd parity.

Odd Parity (Pin 6) – Odd-parity output. This pin goes high if the data word has odd parity and low if the data word has even parity.

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FIGURE 1 – SWITCHING WAVEFORMS

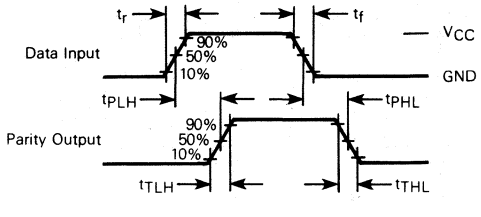
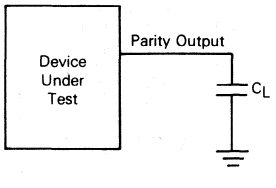
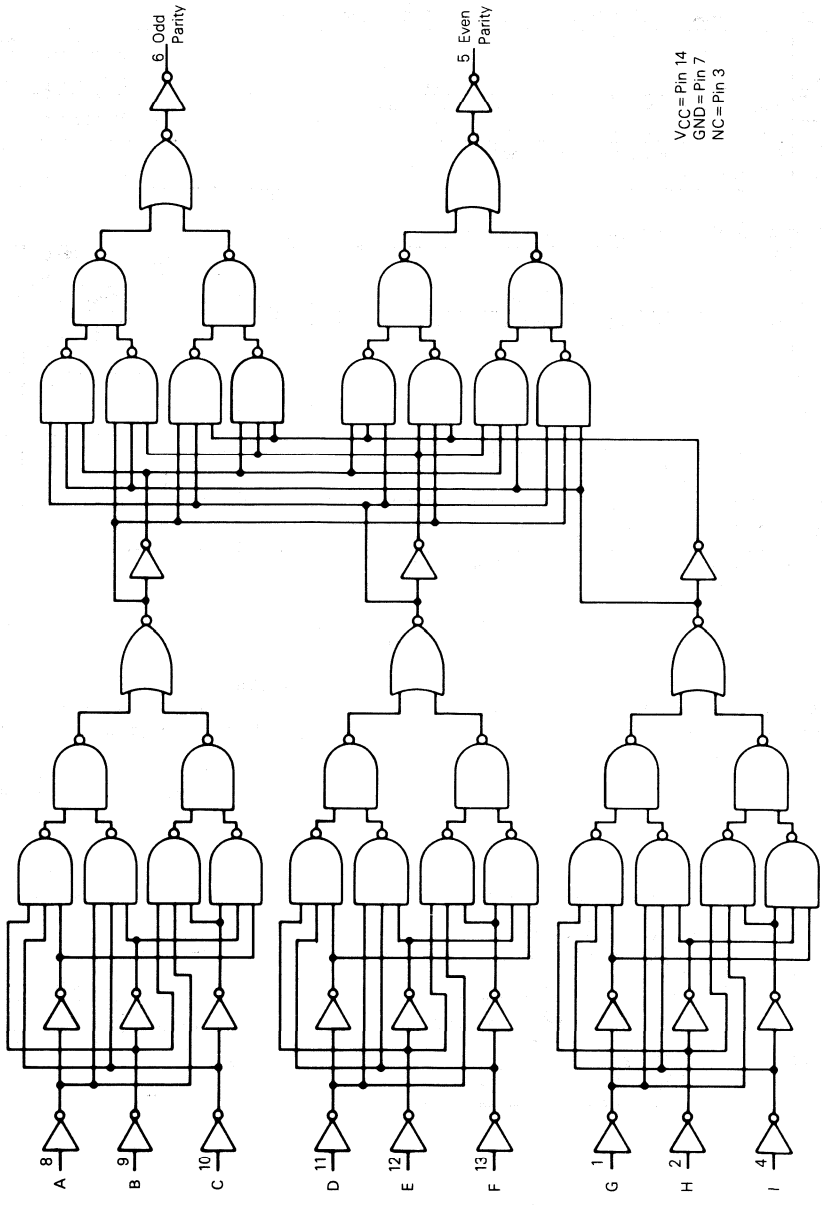


FIGURE 2 – TEST CIRCUIT



LOGIC DIAGRAM
(Positive Logic)



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MOTOROLA

MC54/74HC283

Product Preview

4-BIT BINARY FULL ADDER WITH FAST CARRY

The MC54/74HC283 is identical in pinout to the LS283. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC283 is a high-speed 4-bit binary Full Adder with internal carry lookahead. The device adds two 4-bit words (A and B) plus the Carry-In bit. The binary sum appears at the Sum outputs (S), and any resulting carries appear at the Carry-Out pin.

Because of the symmetry of the binary add function, the HC283 can be used with either all inputs and outputs active high (positive logic), or with all inputs and outputs active low (negative logic). With active high inputs, Carry In cannot be left open, but must be held low when no carry in is intended.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

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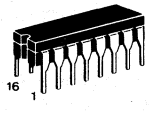
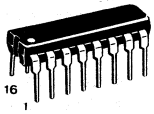
SILICON-GATE

4-BIT BINARY FULL ADDER WITH FAST CARRY



J SUFFIX
CERAMIC PACKAGE
CASE 620



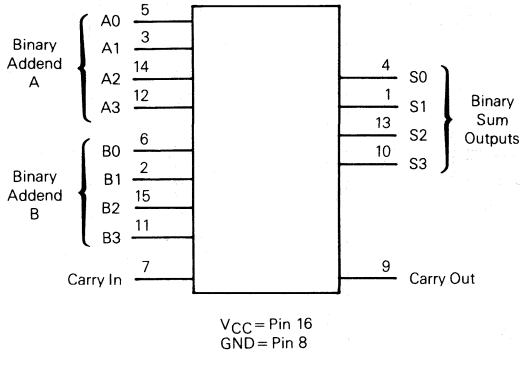
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

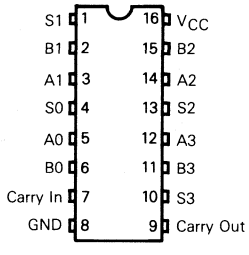
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



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MOTOROLA

MC54/74HC292

Product Preview

PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER

The MC54/74HC292 is identical in pinout to the LS292. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device divides the incoming clock frequency by a number (a power of 2) that is preset by the Programming inputs. It has two Clock inputs, either of which may be used as a clock inhibit. The device also has an active-low Reset, which initializes the internal flip-flop states. Test Point outputs (TP1, TP2, TP3) are provided to facilitate incoming inspections.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

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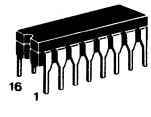
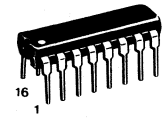
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER



J SUFFIX
CERAMIC PACKAGE
CASE 620



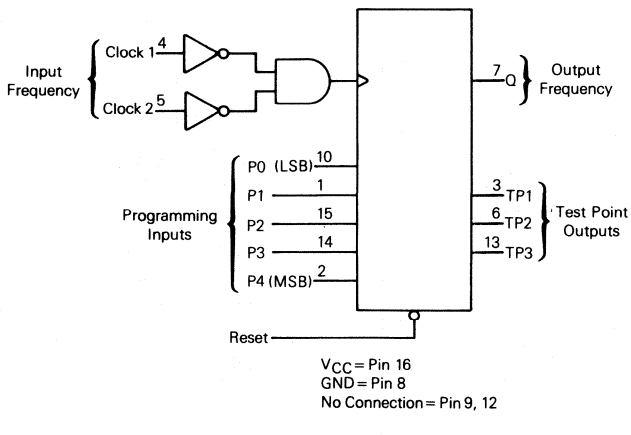
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

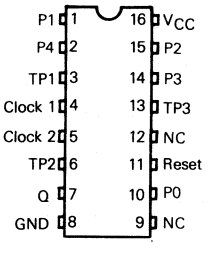
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
No Connection = Pin 9, 12

PIN ASSIGNMENT



NC = No Connection

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MOTOROLA

MC54/74HC294

Product Preview

PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER

The MC54/74HC294 is identical in pinout to the LS294. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device divides the incoming clock frequency by a number (a power of 2) that is preset by the Programming inputs. It has two Clock inputs, either of which may be used as a clock inhibit. The device also has an active-low Reset, which initializes the internal flip-flop states. A Test Point output, is provided to facilitate incoming inspections.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
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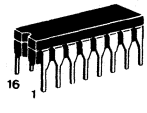
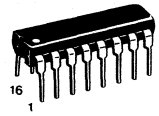
SILICON-GATE

PROGRAMMABLE FREQUENCY
DIVIDER/DIGITAL TIMER



J SUFFIX
CERAMIC PACKAGE
CASE 620



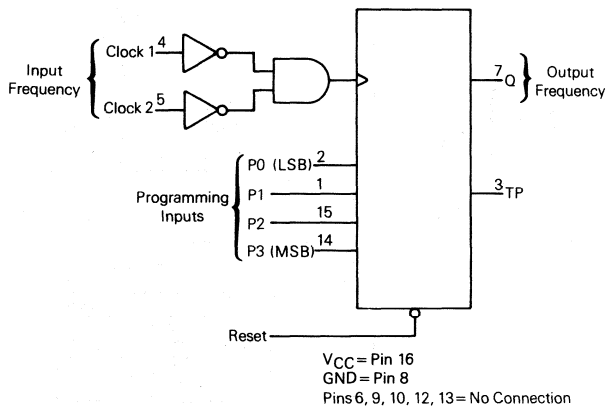
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

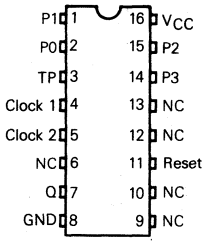
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
Pins 6, 9, 10, 12, 13 = No Connection

PIN ASSIGNMENT



NC = No Connection

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

5

MOTOROLA

MC54/74HC298

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD 2-INPUT DATA SELECTOR/MULTIPLEXER WITH OUTPUT LATCH

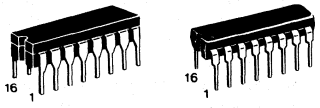
QUAD 2-INPUT DATA SELECTOR/ MULTIPLEXER WITH OUTPUT LATCH

The MC54/74HC298 is identical in pinout to the LS298. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects one of two 4-bit words to be stored in the output latch with the falling edge of the Clock input.

The HC298 is the equivalent of a quad 2-input multiplexer followed by a 4-bit edge-triggered latch. A common Select input selects between two 4-bit data words. The selected word is transferred to the output latch synchronous with the high-to-low transition of the Latch Clock input.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620

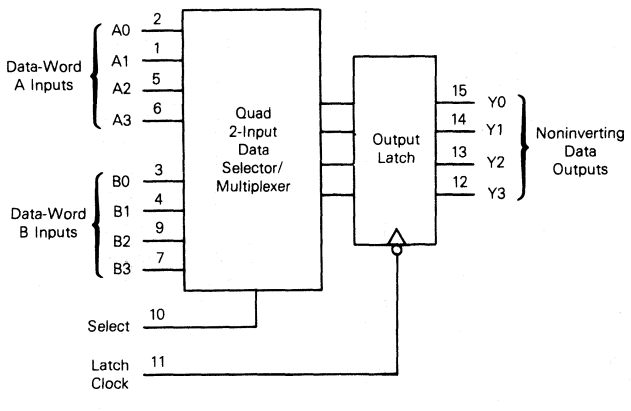
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

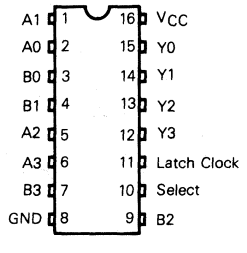
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
Select	Latch Clock	Y0-Y3
L	↓	A0-A3
H	↓	B0-B3

A0-A3, B0-B3 = the levels of the respective Data-Word Inputs.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

5

MOTOROLA

MC54/74HC299

Product Preview

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS

The MC54/74HC299 is identical in pinout to the LS299. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

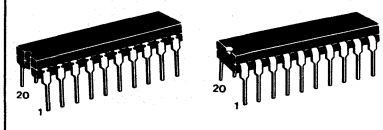
The MC54/74HC299 features multiplexed parallel input/output data ports to achieve full 8-bit handling in a 20 pin package. Due to the large output drive capability and the 3-state feature, this device is ideally suited for interface with bus lines in a bus-oriented system.

Two Mode-Select inputs and two Output-Enable inputs are used to choose the mode of operation as listed in the function table. Synchronous parallel loading is accomplished by taking both Mode-Select lines, S0 and S1, high. This places the outputs in the high-impedance state, which permits data applied to the data ports to be clocked into the register. Reading out of the register can be done while the outputs are enabled in any mode. The Reset input is asynchronous, active-low, and it overrides all other inputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE PARALLEL OUTPUTS



J SUFFIX
CERAMIC PACKAGE
CASE 732-03

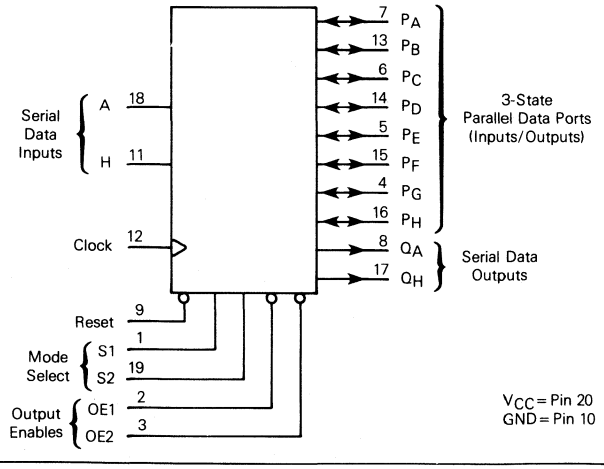
N SUFFIX
PLASTIC PACKAGE
CASE 738-02

ORDERING INFORMATION

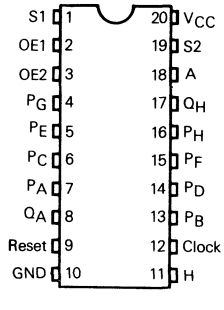
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTION TABLE

Inputs								
	Mode Select		Output Enables			Serial Data		
Reset	S2	S1	OE1	OE2	Clock	A	H	Response
L	X	X	H	X	X	X	X	Asynchronous Reset;
L	X	X	X	H	X	X	X	$Q_A = Q_H = L$
L	H	H	X	X	X	X	X	P_A through $P_H = Z$
L	L	X	L	L	X	X	X	Asynchronous Reset; $Q_A = Q_H = L$
L	X	L	L	L	X	X	X	P_A through $P_H = L$
H	L	H	X	X	⌐	D	X	Shift Right; $A \rightarrow Q_A$; $Q_A \rightarrow Q_B$; etc.
H	L	H	L	L	⌐	D	X	Shift Right; $A \rightarrow Q_A = P_A$; $Q_A \rightarrow Q_B = P_B$
H	H	L	X	X	⌐	X	D	Shift Left; $H \rightarrow Q_H$; $Q_H \rightarrow Q_G$; etc.
H	H	L	L	L	⌐	X	D	Shift Left; $H \rightarrow Q_H = P_H$; $Q_H \rightarrow Q_G = P_G$
H	H	H	X	X	⌐	X	X	Parallel Load; $P_n \rightarrow Q_n$
H	L	L	H	X	X	X	X	Hold: P_A through $P_H = Z$
H	L	L	X	H	X	X	X	
H	L	L	L	L	X	X	X	Hold: $P_n = Q_n$

Z = high impedance

5

MOTOROLA

MC54/74HC354

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

8-INPUT DATA SELECTOR/ MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

8-INPUT DATA SELECTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

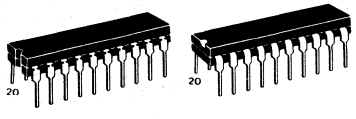
The MC54/74HC354 is identical in pinout to the LS354. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC354 selects one of eight latched binary Data inputs, as determined by the Address Inputs. The information at the Data inputs is stored in the transparent 8-bit Data Latch when the active-low Data-Latch Enable pin is held low. The Address information may be stored in the transparent Address Latch, which is enabled by the active-low Address-Latch Enable pin.

The device outputs are placed in high-impedance states when Output Enable 1 is high, Output Enable 2 is high, or Output Enable 3 is low.

The HC354 is similar in function to the HC356, which has a clocked Data Latch that is not transparent.

- Transparent Data Latch
- Transparent Address Latch
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 732

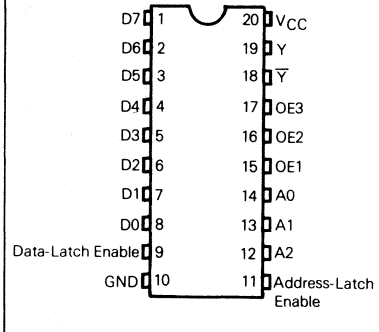
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

54 Series: $-55°C$ to $+125°C$
MC54HCXXXJ (Ceramic Package Only)

74 Series: $-40°C$ to $+85°C$
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



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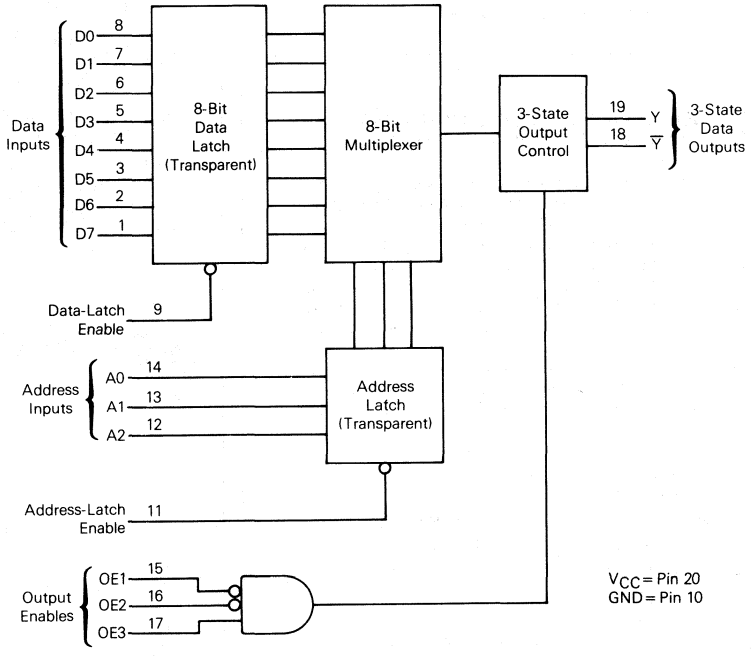
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



FUNCTION TABLE

Inputs							Outputs		Description
Address			Data-Latch Enable	Output Enables					
A2	A1	A0		OE1	OE2	OE3	Y	$\overline{Y}$	
X	X	X	X	H	X	X	Z	Z	Outputs in high-impedance states
X	X	X	X	X	H	X	Z	Z	
X	X	X	X	X	X	L	Z	Z	
L	L	L	H	L	L	H	D0	$\overline{D0}$	Data Latch is transparent
L	L	H					D1	$\overline{D1}$	
L	H	L					D2	$\overline{D2}$	
L	H	H					D3	$\overline{D3}$	
H	L	L					D4	$\overline{D4}$	
H	L	H					D5	$\overline{D5}$	
H	H	L					D6	$\overline{D6}$	
H	H	H					D7	$\overline{D7}$	
L	L	L	L	L	L	H	$D0_n$	$\overline{D0}_n$	New data is latched into Data Latch
L	L	H					$D1_n$	$\overline{D1}_n$	
L	H	L					$D2_n$	$\overline{D2}_n$	
L	H	H					$D3_n$	$\overline{D3}_n$	
H	L	L					$D4_n$	$\overline{D4}_n$	
H	L	H					$D5_n$	$\overline{D5}_n$	
H	H	L					$D6_n$	$\overline{D6}_n$	
H	H	H					$D7_n$	$\overline{D7}_n$	

X = don't care Z = high impedance

D0-D7 = the data at inputs D0 through D7

$D0_n$-$D7_n$ = the data present at inputs D0 through D7 when the Data-Latch Enable pin was taken low.

MOTOROLA

MC54/74HC356

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

8-INPUT DATA SELECTOR/ MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

8-INPUT DATA SELECTOR/MULTIPLEXER WITH DATA AND ADDRESS LATCHES AND WITH 3-STATE OUTPUTS

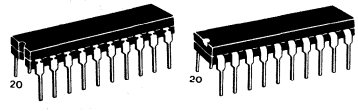
The MC54/74HC356 is identical in pinout to the LS356. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC356 selects one of eight latched binary Data inputs, as determined by the Address inputs. The information at the Data inputs is latched into the Data Latch with the rising edge of the Data-Latch Clock. The Address information may be stored in the transparent Address Latch, which is enabled by the active-low Address-Latch Enable pin.

The device outputs are placed in high-impedance states when Output Enable 1 is high, Output Enable 2 is high, or Output Enable 3 is low.

The HC356 is similar in function to the HC354, which has a transparent Data Latch.

- Nontransparent Data Latch
- Transparent Address Latch
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 732

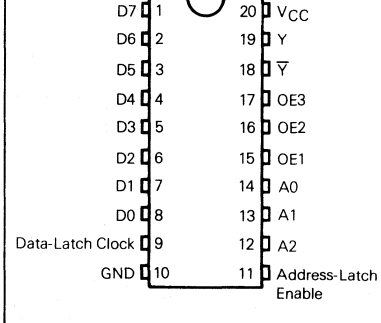
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



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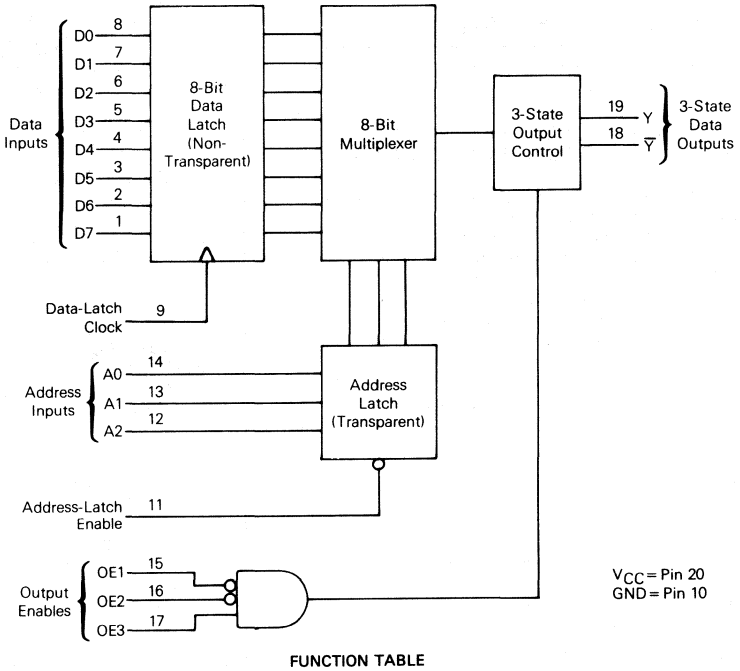
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



FUNCTION TABLE

Inputs							Outputs		
Address			Data-Latch Clock	Output Enables					
A2	A1	A0		OE1	OE2	OE3	Y	$\overline{Y}$	Description
X	X	X	X	H	X	X	Z	Z	Outputs in high-impedance states
X	X	X	X	X	H	X	Z	Z	
X	X	X	X	X	X	L	Z	Z	
L	L	L	↗	L	L	H	$D0_n$	$\overline{D0}_n$	New data is latched into Data Latch
L	L	H					$D1_n$	$\overline{D1}_n$	
L	H	L					$D2_n$	$\overline{D2}_n$	
L	H	H					$D3_n$	$\overline{D3}_n$	
H	L	L					$D4_n$	$\overline{D4}_n$	
H	L	H					$D5_n$	$\overline{D5}_n$	
H	H	L					$D6_n$	$\overline{D6}_n$	
H	H	H					$D7_n$	$\overline{D7}_n$	
L	L	L	H, L, or ↘	L	L	H	$D0_p$	$\overline{D0}_p$	Outputs do not change states.
L	L	H					$D1_p$	$\overline{D1}_p$	
L	H	L					$D2_p$	$\overline{D2}_p$	
L	H	H					$D3_p$	$\overline{D3}_p$	
H	L	L					$D4_p$	$\overline{D4}_p$	
H	L	H					$D5_p$	$\overline{D5}_p$	
H	H	L					$D6_p$	$\overline{D6}_p$	
H	H	H					$D7_p$	$\overline{D7}_p$	

X = don't care Z = high impedance

$D0_n$-$D7_n$ = the data present at inputs D0 through D7 when the Data-Latch Clock made the transition from low to high.

$D0_p$-$D7_p$ = the data previously latched into the Data Latch by the low-to-high transition of the Data-Latch Clock

MOTOROLA

MC54/74HC365

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

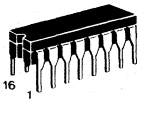
HEX 3-STATE BUFFER WITH COMMON ENABLES

HEX 3-STATE BUFFER WITH COMMON ENABLES

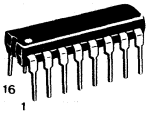
The MC54/74HC365 is identical in pinout to the LS365. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is a high-speed hex buffer with 3-state outputs and two common active-low Output Enables. When either of the enables is high, the buffer outputs are placed into high-impedance states. The HC365 has noninverting outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs
- Chip Complexity: 90 FETs or 22.5 Equivalent Gates



J SUFFIX
CERAMIC PACKAGE
CASE 620



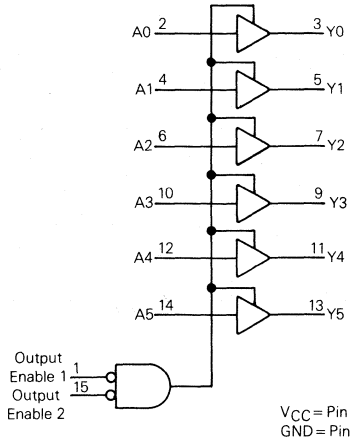
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

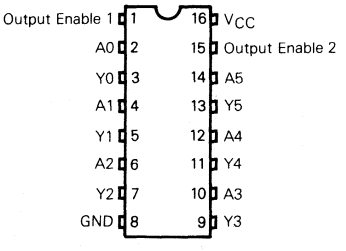
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs
Enable 1	Enable 2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

X = don't care
Z = high impedance

ADI-1021

5

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12 mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C ★ 54HC and 74HC		85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed Limit			Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	±0.005	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	0.04	8	80	160	μA

★ The 25°C Guaranteed Limits are also valid for the 74HC series at −40°C and the 54HC series at −55°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, (Figures 1 and 3)	C_L = 50 pF	15	22	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, (Figures 2 and 4)	C_L = 5 pF	25	36	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, (Figures 2 and 4)	C_L = 50 pF	29	40	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L = 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C ★ 54HC and 74HC Typical	25°C ★ 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, (Figures 1 and 3)	C_L = 50 pF	2.0	35	105	130	150	ns
		C_L = 150 pF		45	135	168	205	
		C_L = 50 pF	4.5	14	24	30	36	
		C_L = 150 pF		17	29	36	45	
		C_L = 50 pF	6.0	11	19	24	28	
		C_L = 150 pF		15	24	30	36	
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, (Figures 2 and 4)	C_L = 50 pF	2.0	58	175	218	260	ns
			4.5	26	44	55	66	
			6.0	22	37	46	55	
t_{PZL}, t_{PZH}	Maximum Propagation Delay, (Figures 2 and 4)	C_L = 50 pF	2.0	90	230	287	345	ns
		C_L = 150 pF		98	245	306	367	
		C_L = 50 pF	4.5	31	44	55	66	
		C_L = 150 pF		38	53	66	80	
		C_L = 50 pF	6.0	25	35	43	52	
		C_L = 150 pF		29	41	51	62	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L = 50 pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{out}	Three-State Output Capacitance (Output Enable = V_{CC})		–	7.5	15	15	15	pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (Per Package)		–	240	–	–	–	pF

★ The 25°C Guaranteed Limits are also valid for the 74HC series at −40°C and the 54HC series at −55°C.

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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SWITCHING WAVEFORMS

FIGURE 1

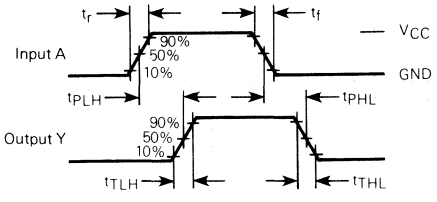


FIGURE 2

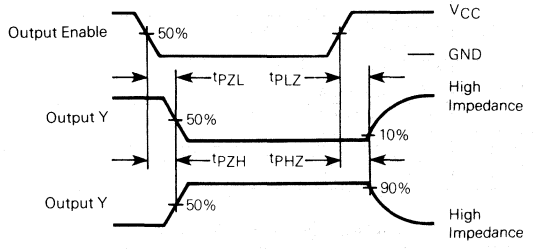


FIGURE 3 — TEST CIRCUIT

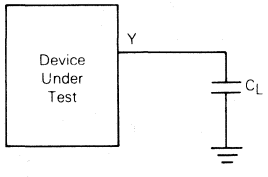
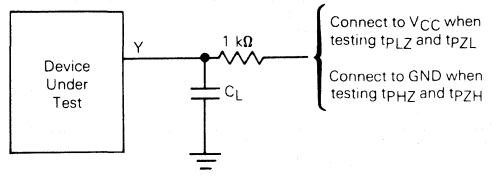
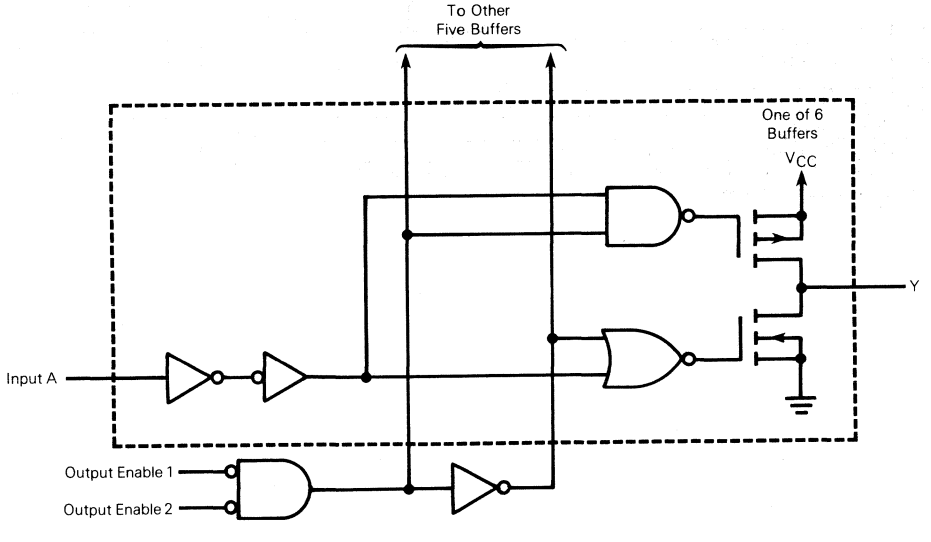


FIGURE 4 — TEST CIRCUIT



FUNCTION DIAGRAM



5

MOTOROLA

MC54/74HC366

Advance Information

HIGH-PERFORMANCE
CMOS
(LOW-POWER COMPLEMENTARY MOS)

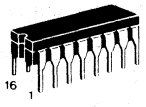
HEX 3-STATE BUFFER
WITH COMMON ENABLES

HEX 3-STATE BUFFER WITH COMMON ENABLES

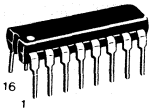
The MC54/74HC366 is identical in pinout to the LS366. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is a high-speed hex buffer with 3-state outputs and two common active-low Output Enables. When either of the enables is high, the buffer outputs are placed into high-impedance states. The HC366 has inverting outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs
- Chip Complexity: 78 FETs or 19.5 Equivalent Gates



J SUFFIX
CERAMIC PACKAGE
CASE 620



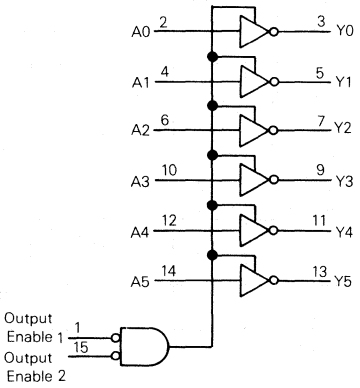
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: – 55°C to + 125°C
MC54HCXXXJ (Ceramic Package Only)

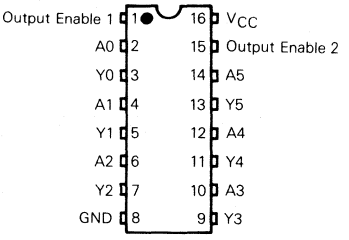
74 Series: – 40°C to + 85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

LOGIC DIAGRAM



V_{CC}= Pin 16
GND= Pin 8

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs
Enable 1	Enable 2	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

X= don't care
Z= high impedance

ADI-1022

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C ★ 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed Limit		
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\|$ = 20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\|$ = 20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{out} = −20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} I_{out} = −6.0 mA I_{out} = −7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{out} = 20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{out} = 6.0 mA I_{out} = 7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable = V_{IH} V_{out} = V_{CC} or GND	6.0	±0.005	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	0.04	8	80	160	μA

★ The 25°C Guaranteed Limits are also valid for the 74HC series at −40°C and the 54HC series at −55°C.

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SWITCHING CHARACTERISTICS (V_{CC}= 5 V, T_A= 25°C, Input t_r= t_f= 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, (Figures 1 and 3)	C_L= 50 pF	12	18	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, (Figures 2 and 4)	C_L= 5 pF	25	36	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, (Figures 2 and 4)	C_L= 50 pF	29	40	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L= 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input t_r= t_f= 6 ns)

Symbol	Parameter		V_{CC}	25°C ★ 54HC and 74HC Typical	25°C ★ 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, (Figures 1 and 3)	C_L = 50 pF	2.0	33	82	102	125	ns
		C_L = 150 pF		43	107	134	160	
		C_L = 50 pF	4.5	12	19	24	30	
		C_L = 150 pF		16	26	32	39	
		C_L = 50 pF	6.0	10	16	20	24	
		C_L = 150 pF		14	22	27	33	
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, (Figures 2 and 4)	C_L = 50 pF	2.0	58	175	218	260	ns
			4.5	26	44	55	66	
			6.0	22	37	46	55	
t_{PZL}, t_{PZH}	Maximum Propagation Delay, (Figures 2 and 4)	C_L = 50 pF	2.0	90	230	287	345	ns
		C_L = 150 pF		98	245	306	367	
		C_L = 50 pF	4.5	31	44	55	66	
		C_L = 150 pF		38	53	66	80	
		C_L = 50 pF	6.0	25	35	43	52	
		C_L = 150 pF		29	41	51	62	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L = 50 pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{out}	Three-State Output Capacitance (Output Enable= V_{CC})		–	7.5	15	15	15	pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (Per Package)		–	240	–	–	–	pF

★ The 25°C Guaranteed Limits are also valid for the 74HC series at – 40°C and the 54HC series at – 55°C.

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

5

SWITCHING WAVEFORMS

FIGURE 1

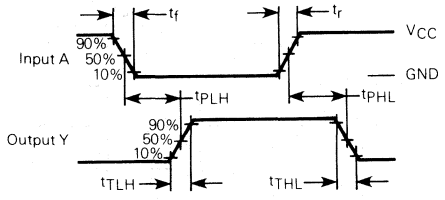


FIGURE 2

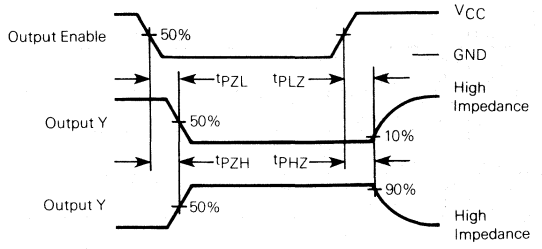


FIGURE 3 — TEST CIRCUIT

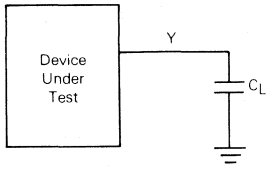
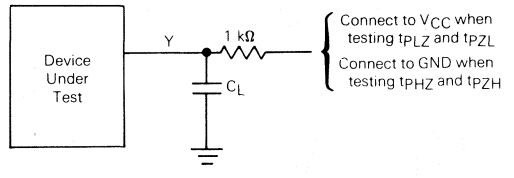
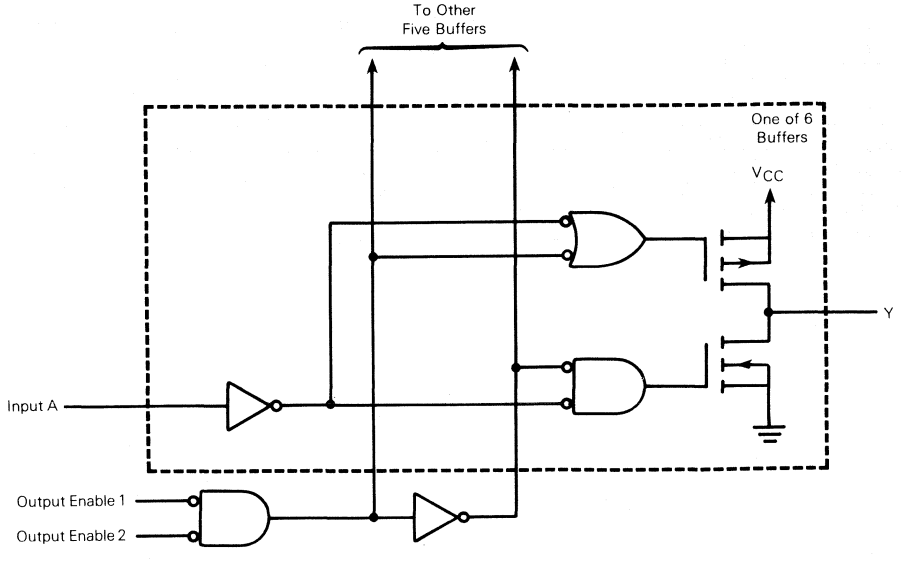


FIGURE 4 — TEST CIRCUIT



FUNCTION DIAGRAM



5

MOTOROLA

MC54/74HC367

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

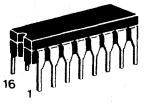
HEX 3-STATE BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

HEX 3-STATE BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

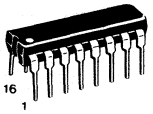
The MC54/74HC367 is identical in pinout to the LS367. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is arranged into 2-bit and 4-bit sections, each having its own active-low Output Enable. When either of the enables is high, the affected buffer outputs are placed into high-impedance states. The HC367 has noninverting outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs
- Chip Complexity: 92 FETs or 23 Equivalent Gates



J SUFFIX
CERAMIC PACKAGE
CASE 620



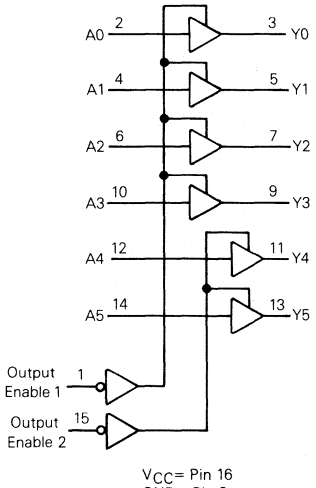
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: – 55°C to + 125°C
MC54HCXXXJ (Ceramic Package Only)

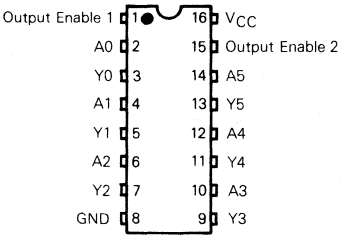
74 Series: – 40°C to + 85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
Enable 1, Enable 2	A	Y
L	L	L
L	H	H
H	X	Z

X = don't care
Z = high impedance

ADI-1023

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C ★ 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed Limit		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	±0.005	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	0.04	8	80	160	μA

★The 25°C Guaranteed Limits are also valid for the 74HC series at −40°C and the 54HC series at −55°C.

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SWITCHING CHARACTERISTICS (V_{CC}= 5 V, T_A= 25°C, Input t_r= t_f= 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, (Figures 1 and 3)	C_L= 50 pF	13	22	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, (Figures 2 and 4)	C_L= 5 pF	25	33	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, (Figures 2 and 4)	C_L= 50 pF	23	37	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L= 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input t_r= t_f= 6 ns)

Symbol	Parameter		V_{CC}	25°C★ 54HC and 74HC Typical	25°C★ 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, (Figures 1 and 3)	C_L= 50 pF	2.0	35	105	130	150	ns
		C_L= 150 pF		45	135	168	205	
		C_L= 50 pF	4.5	14	24	30	36	
		C_L= 150 pF		17	29	36	45	
		C_L= 50 pF	6.0	11	19	24	28	
		C_L= 150 pF		15	24	30	36	
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, (Figures 2 and 4)	C_L= 50 pF	2.0	47	117	146	220	ns
			4.5	22	35	44	52	
			6.0	19	31	39	46	
t_{PZL}, t_{PZH}	Maximum Propagation Delay, (Figures 2 and 4)	C_L= 50 pF	2.0	69	172	216	250	ns
		C_L= 150 pF		75	187	233	280	
		C_L= 50 pF	4.5	24	38	47	57	
		C_L= 150 pF		29	46	57	69	
		C_L= 50 pF	6.0	22	35	43	52	
		C_L= 150 pF		26	42	52	63	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L= 50 pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{out}	Three-State Output Capacitance (Output Enable= V_{CC})		–	7.5	15	15	15	pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (Per Package)		–	240	–	–	–	pF

★ The 25°C Guaranteed Limits are also valid for the 74HC series at – 40°C and the 54HC series at – 55°C.

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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SWITCHING WAVEFORMS

FIGURE 1

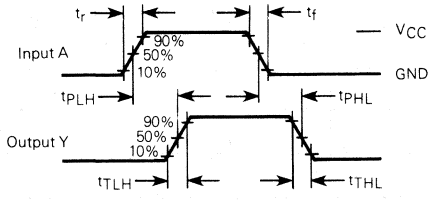


FIGURE 2

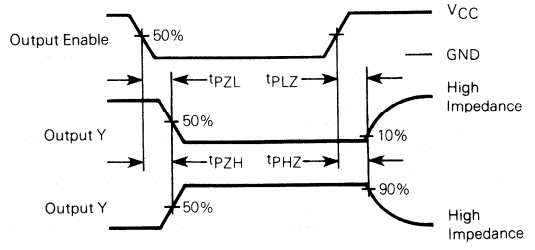


FIGURE 3 — TEST CIRCUIT

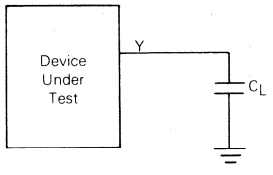
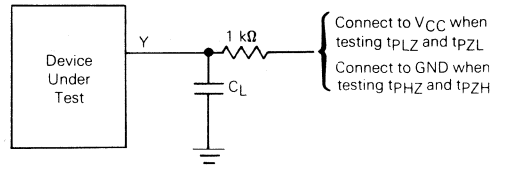
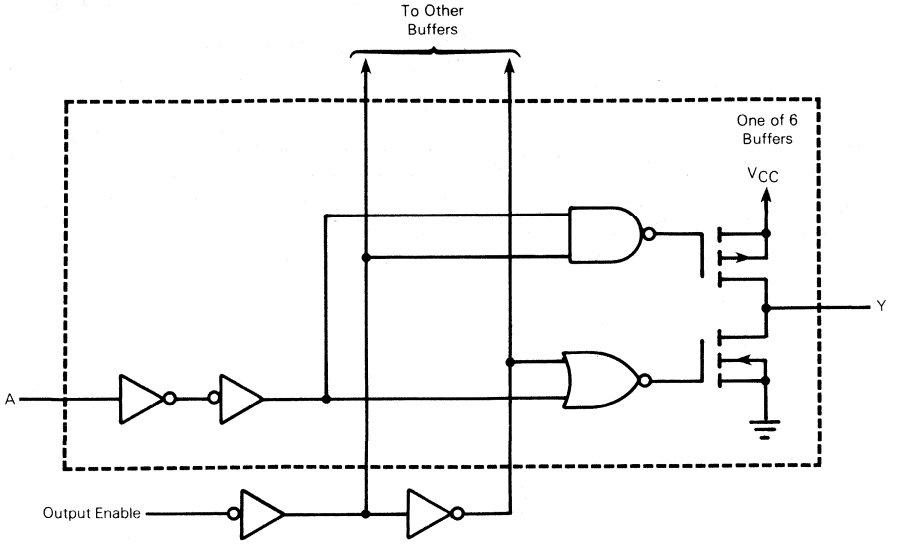


FIGURE 4 — TEST CIRCUIT



FUNCTION DIAGRAM



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MOTOROLA

MC54/74HC368

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

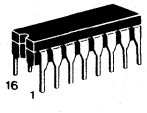
HEX 3-STATE BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

HEX 3-STATE BUFFER WITH SEPARATE 2-BIT AND 4-BIT SECTIONS

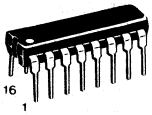
The MC54/74HC368 is identical in pinout to the LS368. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is arranged into 2-bit and 4-bit sections, each having its own active-low Output Enable. When either of the enables is high, the affected buffer outputs are placed into high-impedance states. The HC368 has inverting outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs
- Chip Complexity: 80 FETs or 20 Equivalent Gates



J SUFFIX
CERAMIC PACKAGE
CASE 620



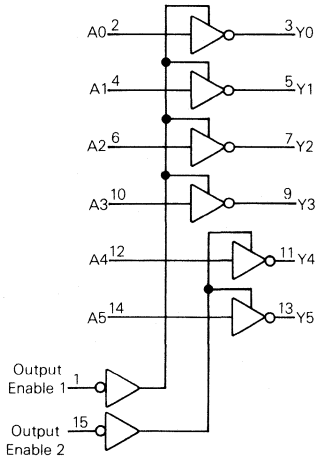
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

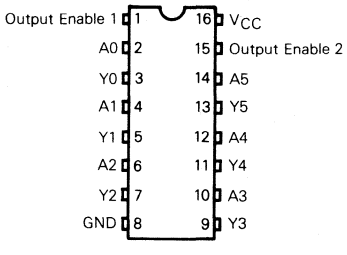
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
Enable 1, Enable 2	A	Y
L	L	H
L	H	L
H	X	Z

X = don't care
Z = high impedance

ADI-1024

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C ★ 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed Limit		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	±0.005	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	0.04	8	80	160	μA

★ The 25°C Guaranteed Limits are also valid for the 74HC series at −40°C and the 54HC series at −55°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC		Unit
			Typical	Guaranteed Limit	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, (Figures 1 and 3)	C_L = 50 pF	11	18	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, (Figures 2 and 4)	C_L = 5 pF	19	33	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, (Figures 2 and 4)	C_L = 50 pF	23	37	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L = 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C ★ 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed Limit		
t_{PLH}, t_{PHL}	Maximum Propagation Delay, (Figures 1 and 3)	C_L = 50 pF	2.0	33	82	102	125	ns
		C_L = 150 pF		43	107	134	160	
		C_L = 50 pF	4.5	12	19	24	30	
		C_L = 150 pF		16	26	32	39	
		C_L = 50 pF	6.0	10	16	20	24	
		C_L = 150 pF		14	22	27	33	
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, (Figures 2 and 4)	C_L = 50 pF	2.0	47	117	146	220	ns
			4.5	22	35	44	52	
			6.0	19	31	39	46	
t_{PZL}, t_{PZH}	Maximum Propagation Delay, (Figures 2 and 4)	C_L = 50 pF	2.0	69	172	216	250	ns
		C_L = 150 pF		75	187	233	280	
		C_L = 50 pF	4.5	24	38	47	57	
		C_L = 150 pF		29	46	57	69	
		C_L = 50 pF	6.0	22	35	43	52	
		C_L = 150 pF		26	42	52	63	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	C_L = 50 pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{out}	Three-State Output Capacitance (Output Enable = V_{CC})		–	7.5	15	15	15	pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (Per Package)		–	240	–	–	–	pF

★ The 25°C Guaranteed Limits are also valid for the 74HC series at −40°C and the 54HC series at −55°C.

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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SWITCHING WAVEFORMS

FIGURE 1

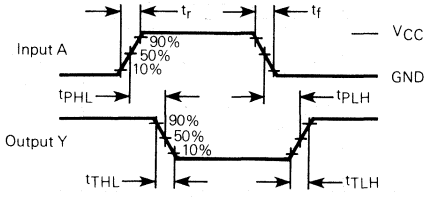


FIGURE 2

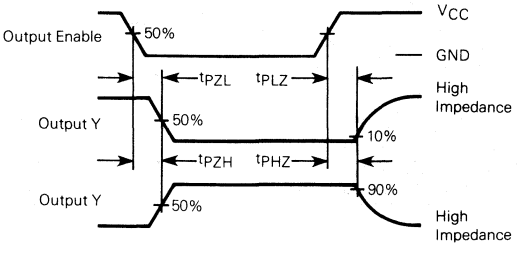


FIGURE 3 — TEST CIRCUIT

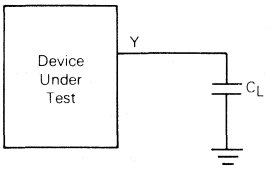
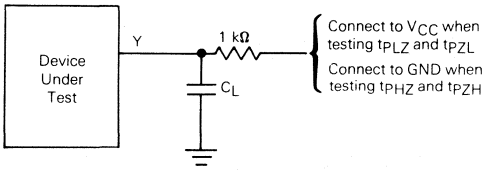
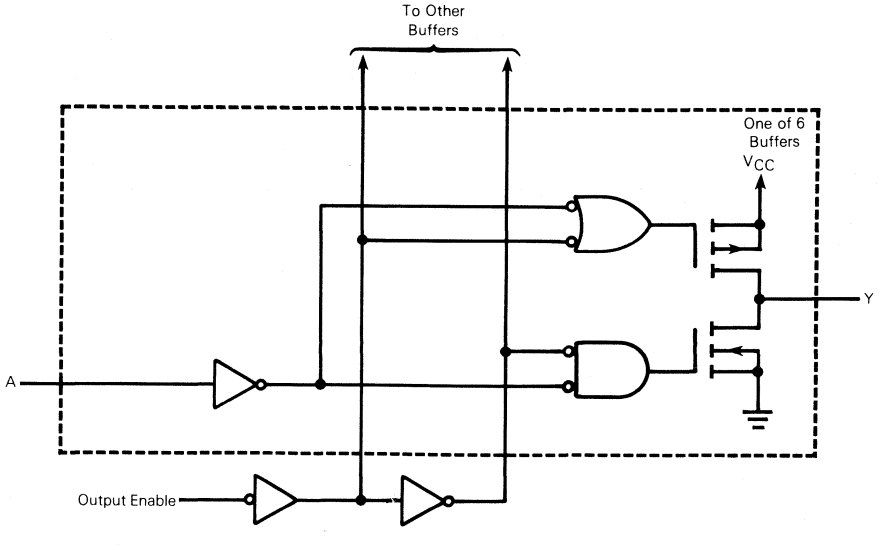


FIGURE 4 — TEST CIRCUIT



FUNCTION DIAGRAM



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MOTOROLA

MC54/74HC373

Advance Information

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

The MC54/74HC373 is identical in pinout to the LS373. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

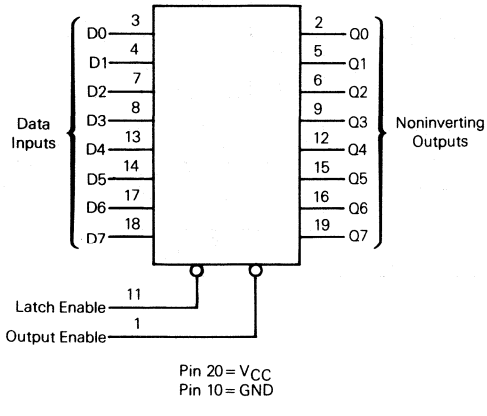
These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup time becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all outputs are forced to the high-impedance state. Data may thus be latched even when the device is not selected.

The HC373 is identical in function to the HC573, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HC533, which has inverting outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM

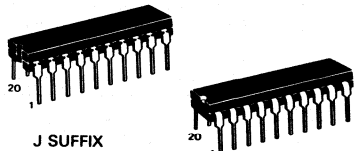


This document contains information on a new product. Specifications and information herein are subject to change without notice.

HIGH-PERFORMANCE CMOS

LOW-POWER COMPLEMENTARY MOS SILICON-GATE

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH



J SUFFIX
CERAMIC PACKAGE
CASE 732

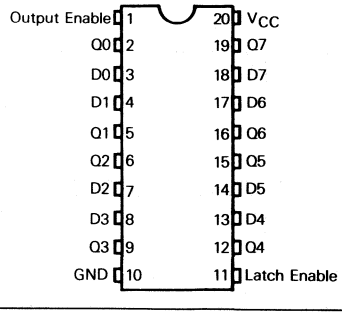
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Output Enable	Latch Enable	D	Output
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

5

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C 54HC and 74HC		85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed			Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input D to Q	C_L = 50 pF	13	25	ns
t_{PHL}	(Figures 1 and 5)		13	25	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Q	C_L = 50 pF	15	30	ns
t_{PHL}	(Figures 2 and 5)		15	30	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Q	C_L = 5 pF	13	25	ns
t_{PHZ}	(Figures 3 and 6)		13	25	
t_{PZL}	Maximum Propagation Delay, Output Enable to Q	C_L = 50 pF	14	28	ns
t_{PZH}	(Figures 3 and 6)		14	28	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	C_L = 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{PHL}		C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	C_L = 50 pF	2.0	88	175	221	261	ns
		C_L = 150 pF		113	225	284	335	
		C_L = 50 pF	4.5	18	35	44	52	
		C_L = 150 pF		23	45	57	67	
		C_L = 50 pF	6.0	15	30	37	44	
		C_L = 150 pF		19	38	48	57	
t_{PHL}		C_L = 50 pF	2.0	88	175	221	261	ns
		C_L = 150 pF		113	225	284	335	
		C_L = 50 pF	4.5	18	35	44	52	
		C_L = 150 pF		23	45	57	67	
		C_L = 50 pF	6.0	15	30	37	44	
		C_L = 150 pF		19	38	48	57	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	C_L = 50 pF	2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PHZ}			2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PZL}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{PZH}		C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	

SWITCHING CHARACTERISTICS (Input $t_r = t_f = 6$ ns) (Continued)

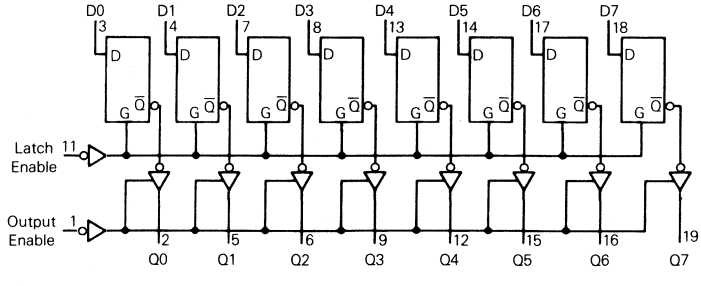
Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	$C_L = 50$ pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{out}	Three-State Output Capacitance (Output Enable = V_{CC})		–	7.5	15	15	15	pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		–	50	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{su}	Minimum Setup Time, Input D to Latch Enable (Figure 4)	2.0	– 10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_h	Minimum Hold Time, Latch Enable to Input D (Figure 4)	2.0	25	50	63	75	ns
		4.5	5	10	13	15	
		6.0	4	9	11	13	
t_w	Minimum Pulse Width, Latch Enable (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

LOGIC DIAGRAM



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SWITCHING WAVEFORMS

FIGURE 1

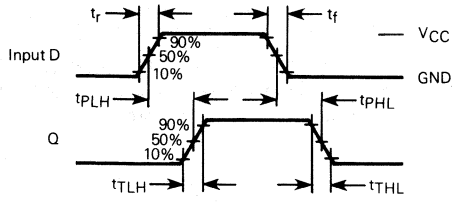


FIGURE 2

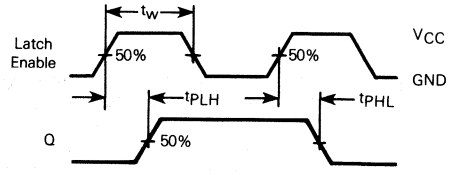


FIGURE 3

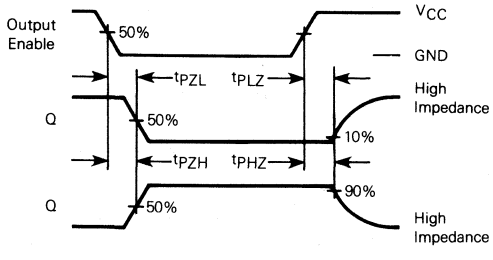


FIGURE 4

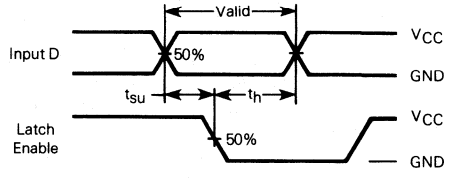


FIGURE 5 — TEST CIRCUIT

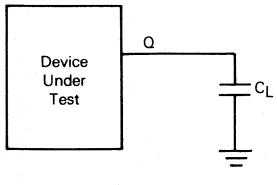
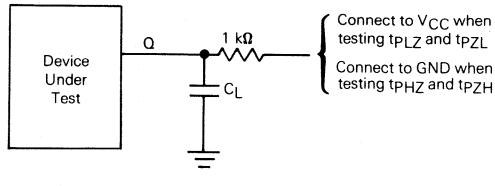


FIGURE 6 — TEST CIRCUIT



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MOTOROLA

MC54/74HCT373

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH (WITH LSTTL-COMPATIBLE INPUTS)

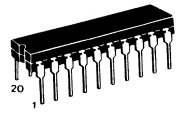
OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH (WITH LSTTL-COMPATIBLE INPUTS)

The HCT373 may be used as a level converter for interfacing LSTTL to High-Speed CMOS. The inputs of HCT devices are compatible with both LSTTL and CMOS output voltage levels.

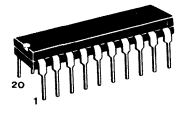
The HCT373 is identical in pinout to the LS373. The latch appears transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup time becomes latched.

The Output Enable does not affect the state of the latch, but when Output Enable is high, all outputs are forced to the high-impedance state. Data may thus be latched even when the device is not selected.

- Compatible with LSTTL Outputs — No Pullup Resistor Required
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Voltage Range: 4.5 to 5.5 Volts
- Low Quiescent Current Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 732



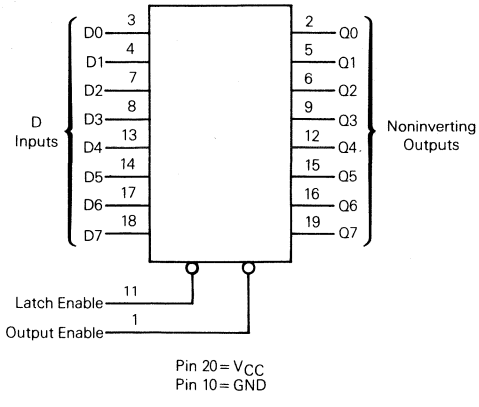
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

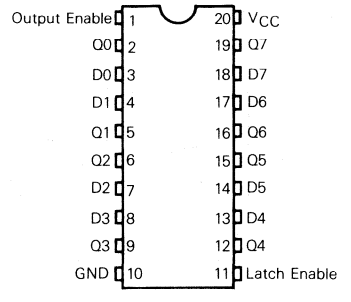
54 Series: −55°C to +125°C
MC54HCTXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCTXXXN (Plastic Package)
MC74HCTXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

MC54/74HC374

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

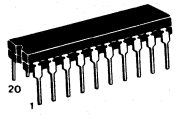
OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

The MC54/74HC374 is identical in pinout to the LS374. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

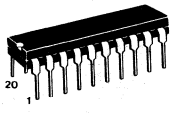
Data meeting the setup time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state. Data may thus be stored even when the device is not selected.

The HC374 is identical in function to the HC574, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HC534, which has inverting outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 732



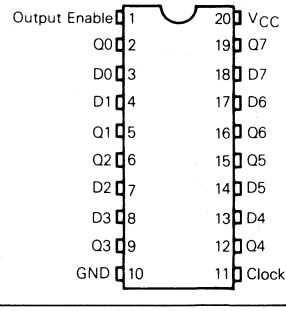
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

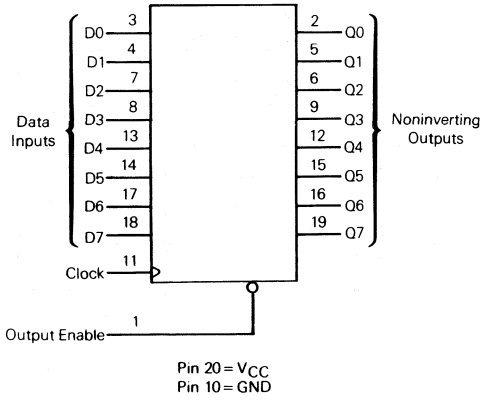
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



BLOCK DIAGRAM



FUNCTION TABLE

Output Enable	Clock	D	Output
L	⎍	H	H
L	⎍	L	L
L	L, H, ⎎	X	no change
H	X	X	Z

X = don't care
Z = high impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

5

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C 54HC and 74HC		85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed			Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	C_L = 50 pF	65	35	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q	C_L = 50 pF	15	32	ns
t_{PHL}	(Figures 1 and 4)		15	32	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Q	C_L = 5 pF	13	25	ns
t_{PHZ}	(Figures 2 and 5)		13	25	
t_{PZL}	Maximum Propagation Delay, Output Enable to Q	C_L = 50 pF	14	28	ns
t_{PZH}	(Figures 2 and 5)		14	28	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	C_L = 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	C_L = 50 pF	2.0	12	6	5	4	MHz
			4.5	60	30	24	20	
			6.0	71	35	28	24	
t_{PLH}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	C_L = 50 pF	2.0	90	180	227	268	ns
		C_L = 150 pF		115	230	290	343	
		C_L = 50 pF	4.5	18	36	45	54	
		C_L = 150 pF		23	46	58	69	
		C_L = 50 pF	6.0	15	31	39	46	
		C_L = 150 pF		20	39	49	58	
t_{PHL}		C_L = 50 pF	2.0	90	180	227	268	ns
		C_L = 150 pF		115	230	290	343	
		C_L = 50 pF	4.5	18	36	45	54	
		C_L = 150 pF		23	46	58	69	
		C_L = 50 pF	6.0	15	31	39	46	
		C_L = 150 pF		20	39	49	58	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	C_L = 50 pF	2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PHZ}			2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PZL}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{PZH}		C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	C_L = 50 pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{out}	Three-State Output Capacitance (Output Enable = V_{CC})		–	7.5	15	15	15	pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (per Latch)		–	50	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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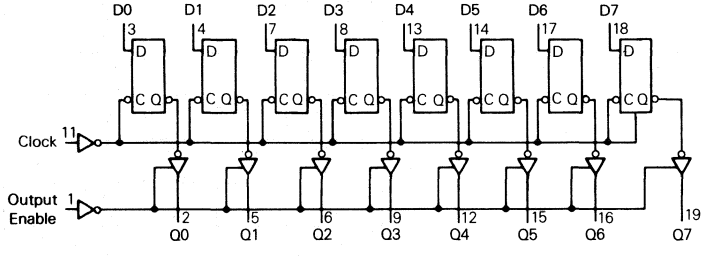
TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
			Typical	Guaranteed Limit			
t_{su}	Minimum Setup Time, Input D to Clock (Figure 3)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Clock to Input D (Figure 3)	2.0	−10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

LOGIC DIAGRAM



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SWITCHING WAVEFORMS

FIGURE 1

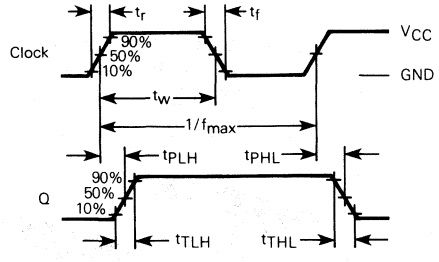


FIGURE 2

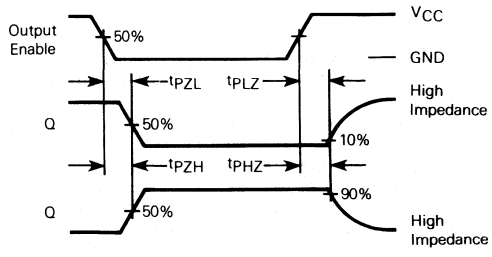


FIGURE 3

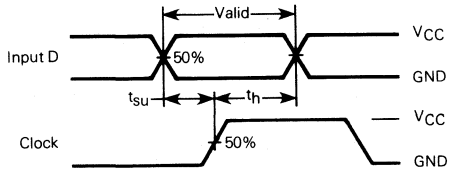


FIGURE 4 — TEST CIRCUIT

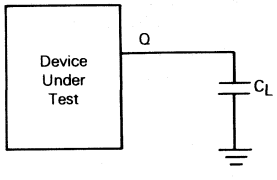
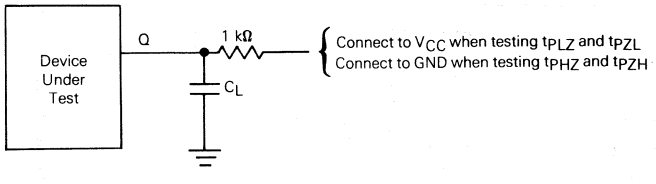


FIGURE 5 — TEST CIRCUIT



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MOTOROLA

MC54/74HCT374

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP (WITH LSTTL-COMPATIBLE INPUTS)

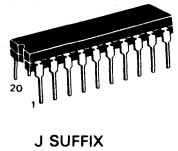
OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP (WITH LSTTL-COMPATIBLE INPUTS)

The HCT374 may be used as a level converter for interfacing LSTTL to High-Speed CMOS. The inputs of HCT devices are compatible with both LSTTL and CMOS output voltage levels.

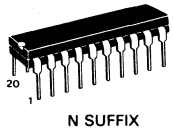
The HCT374 is identical in pinout to the LS374.

Data meeting the setup time is clocked to the outputs with the rising edge of the clock. The Output Enable does not affect the state of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state. Data may thus be stored even when the device is not selected.

- Compatible with LSTTL Outputs — No Pullup Resistor Required
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Voltage Range: 4.5 to 5.5 Volts
- Low Quiescent Current Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 732



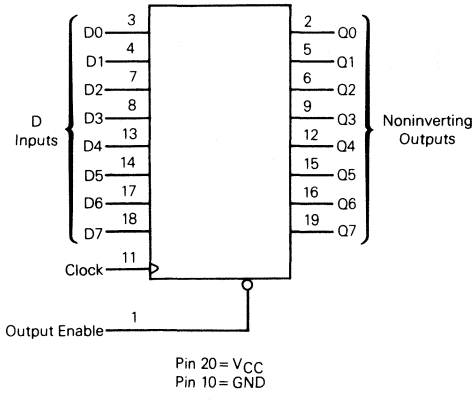
N SUFFIX
PLASTIC PACKAGE
CASE 738

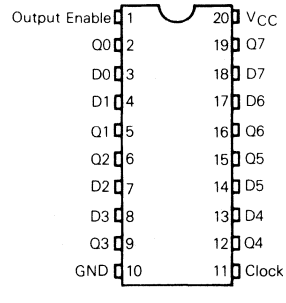
ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCTXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCTXXXN (Plastic Package)
MC74HCTXXXJ (Ceramic Package)

BLOCK DIAGRAM





FUNCTION TABLE

Output Enable	Clock	D	Q
L	↗	H	H
L	↗	L	L
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

MC54/74HC390

Advance Information

DUAL 4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷5 SECTIONS

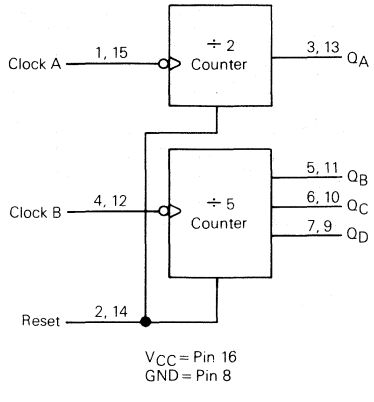
The MC54/74HC390 is identical in pinout to the LS390. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five section. The divide-by-two and divide-by-five counters have separate clock inputs, and can be cascaded to implement various combinations of ÷2 and/or ÷5 up to a ÷100 counter.

Flip-flops internal to the counters are triggered by high-to-low transitions of the clock input. A separate, asynchronous reset is provided for each 4-bit counter. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or strobes except when gated with the Clock of the HC390.

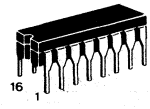
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM

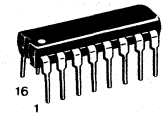


HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL 4-STAGE BINARY RIPPLE COUNTER WITH ÷2 AND ÷5 SECTIONS



J SUFFIX
CERAMIC PACKAGE
CASE 620



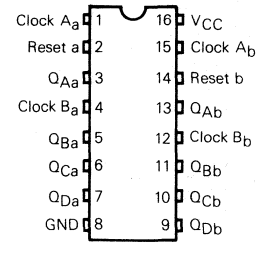
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Clock A	Clock B	Reset	Action
X	X	H	Reset ÷2 and ÷5
↓	X	L	Increment ÷2
X	↓	L	Increment ÷5

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed	85°C 74HC Guaranteed	125°C 54HC Guaranteed	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Frequency, Clock A or Clock B (50% Duty Cycle) (Figures 1 and 3)	60	30	MHz
t_{PLH}	Maximum Propagation Delay, Clock A to Q_A (Figures 1 and 3)	12	20	ns
t_{PHL}		12	20	
t_{PLH}	Maximum Propagation Delay, Clock A to Q_C (Q_A Connected to Clock B) (Figures 1 and 3)	32	50	ns
t_{PHL}		32	50	
t_{PLH}	Maximum Propagation Delay, Clock B to Q_B (Figures 1 and 3)	15	21	ns
t_{PHL}		15	21	
t_{PLH}	Maximum Propagation Delay, Clock B to Q_C (Figures 1 and 3)	16	32	ns
t_{PHL}		16	32	
t_{PLH}	Maximum Propagation Delay, Clock B to Q_D (Figures 1 and 3)	15	21	ns
t_{PHL}		15	21	
t_{PHL}	Maximum Propagation Delay, Reset to Q_A, Q_B, Q_D (Figures 2 and 3)	15	28	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Frequency, Clock A or Clock B (50% Duty Cycle) (Figures 1 and 3)	2.0	10	5	4	3	MHz
		4.5	54	27	21	18	
		6.0	62	31	24	20	
t_{PLH}	Maximum Propagation Delay, Clock A to Q_A (Figures 1 and 3)	2.0	45	120	150	180	ns
		4.5	15	24	30	35	
		6.0	13	21	26	31	
t_{PHL}		2.0	45	120	150	180	ns
		4.5	15	24	30	35	
		6.0	13	21	26	31	
t_{PLH}	Maximum Propagation Delay, Clock A to Q_C (Q_A Connected to Clock B (Figures 1 and 3)	2.0	100	290	360	430	ns
		4.5	35	58	72	87	
		6.0	30	50	62	75	
t_{PHL}		2.0	100	290	360	430	ns
		4.5	35	58	72	87	
		6.0	30	50	62	75	
t_{PLH}	Maximum Propagation Delay, Clock B to Q_B (Figures 1 and 3)	2.0	50	130	160	195	ns
		4.5	16	26	33	39	
		6.0	13	22	28	33	
t_{PHL}		2.0	50	130	160	195	ns
		4.5	16	26	33	39	
		6.0	13	22	28	33	
t_{PLH}	Maximum Propagation Delay, Clock B to Q_C (Figures 1 and 3)	2.0	60	185	230	280	ns
		4.5	20	37	46	55	
		6.0	17	32	40	48	
t_{PHL}		2.0	60	185	230	280	ns
		4.5	20	37	46	55	
		6.0	17	32	40	48	
t_{PLH}	Maximum Propagation Delay, Clock B to Q_D (Figures 1 and 3)	2.0	50	130	160	195	ns
		4.5	16	26	33	39	
		6.0	13	22	28	33	
t_{PHL}		2.0	50	130	160	195	ns
		4.5	16	26	33	39	
		6.0	13	22	28	33	
t_{PHL}	Maximum Propagation Delay, Reset to Q_A, Q_B, Q_C, Q_D (Figures 2 and 3)	2.0	55	165	210	250	ns
		4.5	17	33	41	49	
		6.0	15	28	35	42	
C_{in}	Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	55	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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TIMING REQUIREMENTS

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_r, t_f	Maximum Input Rise and Fall Time (Figure 1)	–	1000	500	500	500	ns
t_w	Minimum Pulse Width, Clock A, Clock B, Reset (Figures 1 and 2)	2.0	30	80	100	120	ns
		4.5	10	16	20	24	
		6.0	9	14	18	20	
t_{rec}	Minimum Reset Recovery Time (Figure 2)	2.0	25	50	65	75	ns
		4.5	5	10	13	15	
		6.0	4	9	11	13	

PIN DESCRIPTIONS

INPUTS

CLOCK A (PINS 1, 15) and CLOCK B (PINS 4, 15) – Clock A is the clock input to the ÷ 2 counter; Clock B is the clock input to the ÷ 5 counter. The internal flip-flops are toggled by high-to-low transitions of the clock input.

CONTROL INPUTS

RESET (PINS 2, 14) – Asynchronous reset. A logic high at the Reset input prevents counting, resets the internal flip-flops, and forces Q_A through Q_D low.

OUTPUTS

Q_A (PINS 3, 13) – Output of the ÷ 2 counter.

Q_B, Q_C, Q_D (PINS 5, 6, 7, 9, 10, 11) – Outputs of the ÷ 5 counter. Q_D is the most significant bit. Q_A is the least significant bit when the counter is connected for BCD output as in Figure 4. Q_B is the least significant bit when the counter is operating in the bi-quinary mode as in Figure 5.

SWITCHING WAVEFORMS

FIGURE 1

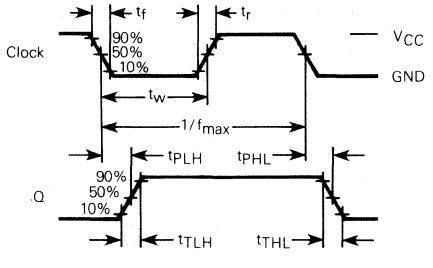


FIGURE 2

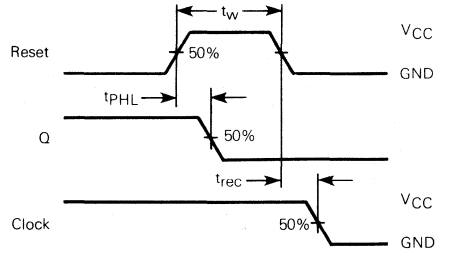
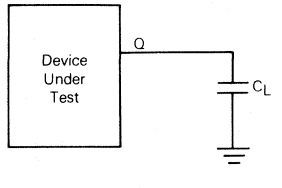
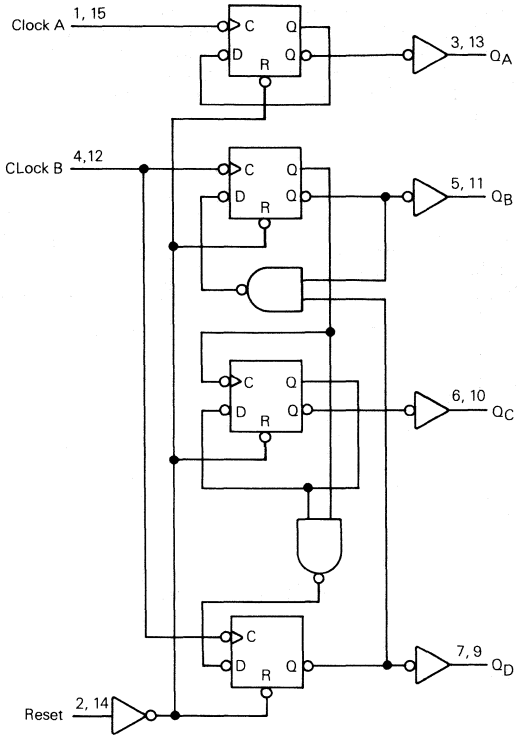


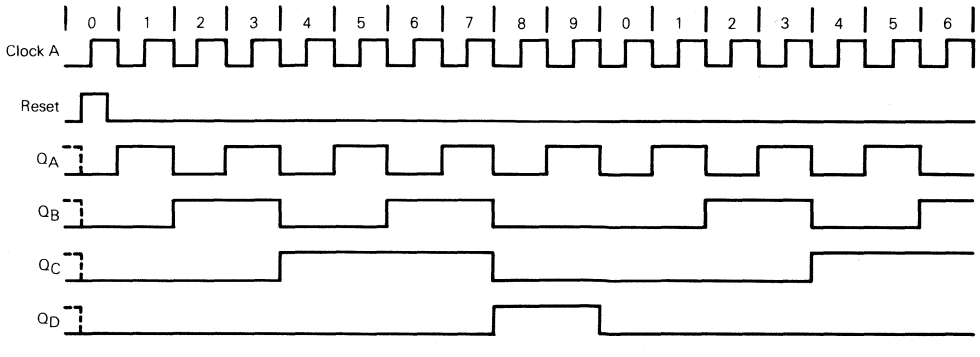
FIGURE 3 – TEST CIRCUIT



LOGIC DIAGRAM



TIMING DIAGRAM
(Q_A Connected to Clock B)



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APPLICATIONS INFORMATION

Each half of the MC54/74HC390 has independent ÷ 2 and ÷ 5 sections (except for the Reset function). The ÷ 2 and ÷ 5 counters can be connected to give BCD or bi-quinary (2-5) count sequences. If output Q_A is connected to the Clock B input (Figure 4), a decade divider with BCD output is obtained. The truth table for the BCD count sequence is given in Table 1.

To obtain a bi-quinary count sequence, the input signal is connected to the Clock B input, and output Q_D is connected to the Clock A input (Figure 5). Q_A provides a 50% duty cycle output. The bi-quinary count sequence truth table is given in Table 2.

TABLE 1 —
BCD COUNT SEQUENCE*

Count	Output Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

*Q_A connected to Clock B input.

TABLE 2 —
BI-QUINARY COUNT SEQUENCE**

Count	Output Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L

**Q_D connected to Clock A input.

CONNECTION DIAGRAMS

FIGURE 4 — BCD COUNT

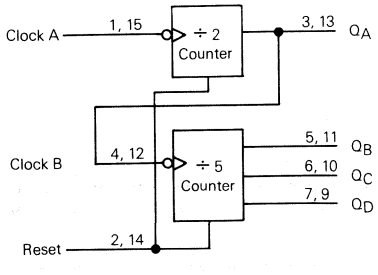
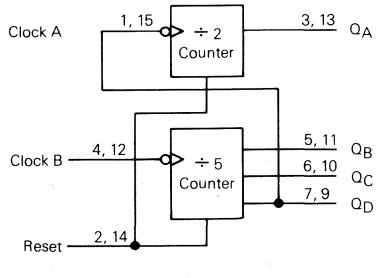


FIGURE 5 — BI-QUINARY COUNT



5

MOTOROLA

MC54/74HC393

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL 4-STAGE BINARY
RIPPLE COUNTER

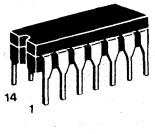
DUAL 4-STAGE BINARY RIPPLE COUNTER

The MC54/74HC393 is identical in pinout to the LS393. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 4-bit binary ripple counters with parallel outputs from each counter stage. A ÷ 256 counter can be obtained by cascading the two binary counters.

Internal flip-flops are triggered by high-to-low transitions of the clock input. Reset for the counters is asynchronous and active-high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC393.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632

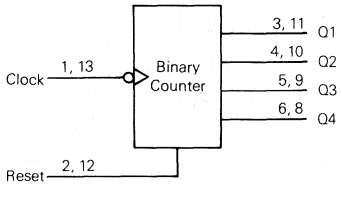
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

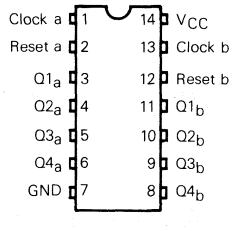
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



FUNCTION TABLE

Clock	Reset	Outputs
X	H	L
H	L	No Change
L	L	No Change
⌐	L	No Change
⌙	L	Advance to Next State

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C 54HC and 74HC		85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed			Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	60	30	MHz
t_{PLH} t_{PHL}	Maximum Propagation Delay, Clock to Q1 (Figures 1 and 3)	13 13	20 20	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay Clock to Q2 (Figures 1 and 3)	19 19	35 35	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay, Clock to Q3 (Figures 1 and 3)	23 23	42 42	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay, Clock to Q4 (Figures 1 and 3)	27 27	50 50	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q1, Q2, Q3, Q4 (Figures 2 and 3)	15	28	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = T_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0 4.5 6.0	10 54 62	5 27 31	4 21 24	3 18 20	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q1 (Figures 1 and 3)	2.0 4.5 6.0	45 15 13	120 24 21	150 30 26	180 35 31	ns
t_{PHL}		2.0 4.5 6.0	45 15 13	120 24 21	150 30 26	180 35 31	ns
t_{PLH}	Maximum Propagation Delay, Clock to Q2 (Figures 1 and 3)	2.0 4.5 6.0	68 23 20	190 38 32	240 47 40	285 57 48	ns
t_{PHL}		2.0 4.5 6.0	68 23 20	190 38 32	240 47 40	285 57 48	ns
t_{PLH}	Maximum Propagation Delay, Clock to Q3 (Figures 1 and 3)	2.0 4.5 6.0	90 30 26	240 48 41	300 60 51	360 72 61	ns
t_{PHL}		2.0 4.5 6.0	90 30 26	240 48 41	300 60 51	360 72 61	ns
t_{PLH}	Maximum Propagation Delay, Clock to Q4 (Figures 1 and 3)	2.0 4.5 6.0	100 35 30	290 58 50	360 72 62	430 87 75	ns
t_{PHL}		2.0 4.5 6.0	100 35 30	290 58 50	360 72 62	430 87 75	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q1, Q2, Q3, Q4 (Figures 2 and 3)	2.0 4.5 6.0	54 18 15	165 33 28	210 41 35	250 49 42	ns
C_{in}	Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	42	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption (per counter): $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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TIMING REQUIREMENTS

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125° 54HC	Unit
			Typical	Guaranteed Limit			
t_r, t_f	Maximum Input Rise and Fall Time (Figure 1)	–	1000	500	500	500	ns
t_w	Minimum Pulse Width, Clock or Reset (Figures 1 and 2)	2.0	30	80	100	120	ns
		4.5	10	16	20	24	
		6.0	9	14	18	20	
t_{rec}	Minimum Reset Recovery Time (Figure 2)	2.0	25	50	65	75	ns
		4.5	5	10	13	15	
		6.0	4	9	11	13	

PIN DESCRIPTIONS

INPUTS

CLOCK (PINS 1, 13) – Clock input. The internal flip-flops are toggled and the counter state advances on high-to-low transitions of the clock input.

CONTROL INPUTS

RESET (PINS 2, 12) – Active-high, asynchronous reset. A separate reset is provided for each counter. A logic high at the Reset input prevents counting and forces all four outputs low.

OUTPUTS

Q1, Q2, Q3, Q4 (PINS 3, 4, 5, 6, 8, 9, 10, 11) – Parallel binary outputs. Q4 is the most-significant bit.

SWITCHING WAVEFORMS

FIGURE 1

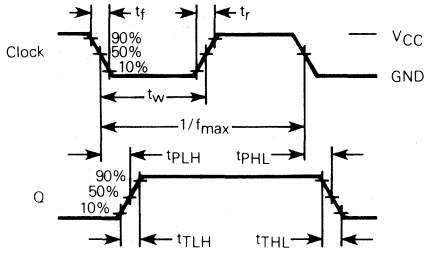


FIGURE 2

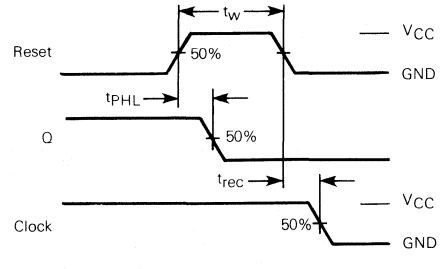
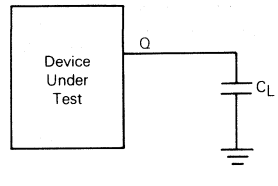


FIGURE 3 – TEST CIRCUIT



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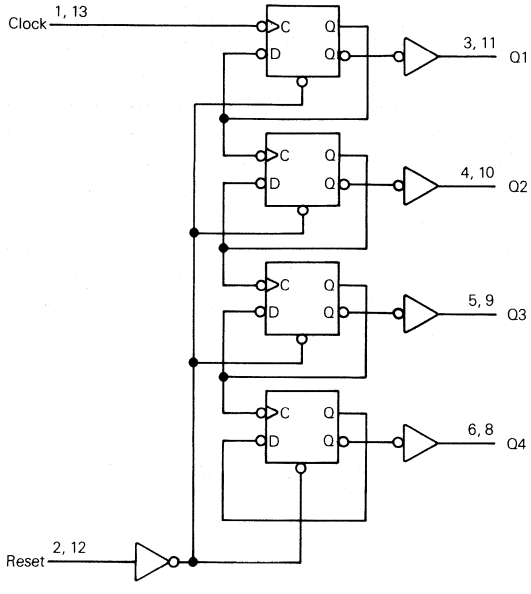
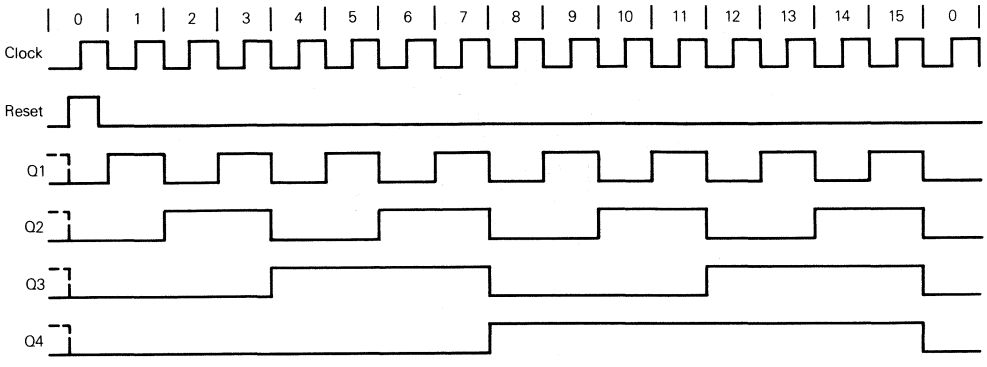
LOGIC DIAGRAM



TIMING DIAGRAM



COUNT SEQUENCE

	Output			
Count	Q4	Q3	Q2	Q1
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

5

MOTOROLA

MC54/74HC423

Product Preview

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

The MC54/74HC423 is identical in pinout to the LS423. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

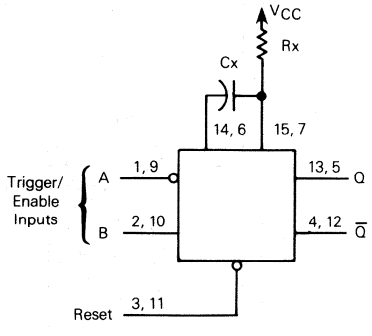
Each multivibrator features an active-low asynchronous reset and both negative- and positive-edge triggered inputs, either of which can be used as an enable. The output pulse width is dependent upon an external resistor and capacitor connection as shown in the block diagram.

The HC423 has the same pinout as the HC123 and the HC221 monostable multivibrators. However, both of these devices may be triggered by using the Reset pin .

If more pulse-width accuracy is required, use the MC54/74HC4538 Precision Monostable Multivibrator.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM

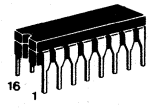


V_{CC} = Pin 16
GND = Pin 8

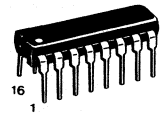
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR



J SUFFIX
CERAMIC PACKAGE
CASE 620



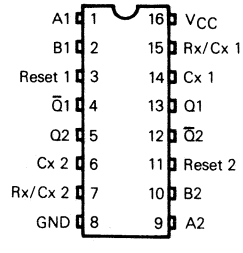
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs	
A	B	Reset	Q	Q̄
X	X	L	L	H
H	X	H	L	H
X	L	H	L	H
L	↓	H	⊓	⊔
↓	H	H	⊓	⊔
L	H	↓	⊓	⊔

5

MOTOROLA

MC54/74HC533

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

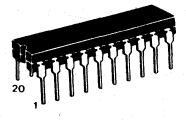
The MC54/74HC533 is identical in pinout to the LS533. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. The data appears at the outputs in inverted form. When Latch Enable goes low, data meeting the setup time becomes latched.

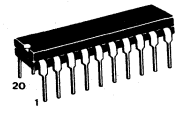
The Output Enable input does not affect the state of the latches, but when Output Enable is high, all outputs are forced to the high-impedance state. Data may thus be latched even when the device is not selected.

The HC533 is identical in function to the HC563, which has the input pins on the opposite side of the package from the output pins. The device is similar in function to the HC373, which has noninverting outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 732



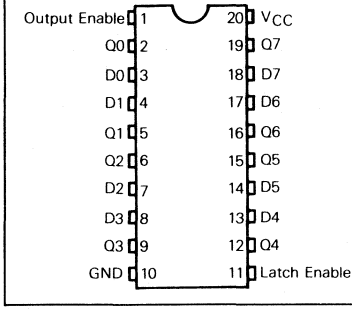
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

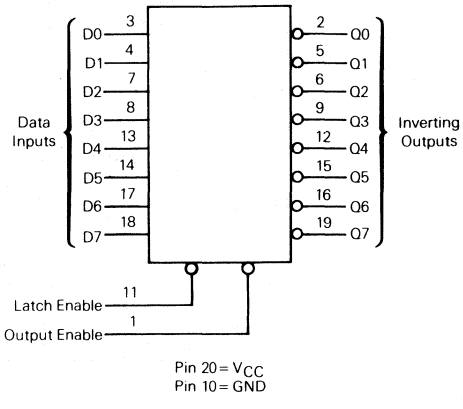
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



BLOCK DIAGRAM



FUNCTION TABLE

Inputs			Outputs
Output Enable	Latch Enable	D	Q
L	H	H	L
L	H	L	H
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

5

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C 54HC and 74HC		85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed			Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input D to Q	C_L = 50 pF	13	25	ns
t_{PHL}	(Figures 1 and 5)		13	25	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Q	C_L = 50 pF	15	30	ns
t_{PHL}	(Figures 2 and 5)		15	30	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Q	C_L = 5 pF	13	25	ns
t_{PHZ}	(Figures 3 and 6)		13	25	
t_{PZL}	Maximum Propagation Delay, Output Enable to Q	C_L = 50 pF	14	28	ns
t_{PZH}	(Figures 3 and 6)		14	28	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	C_L = 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	C_L = 50 pF	2.0	75	150	189	224	ns
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{PHL}		C_L = 50 pF	2.0	75	150	189	224	
		C_L = 150 pF		100	200	252	298	
		C_L = 50 pF	4.5	15	30	38	45	
		C_L = 150 pF		20	40	50	60	
		C_L = 50 pF	6.0	13	26	32	38	
		C_L = 150 pF		17	34	43	51	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	C_L = 50 pF	2.0	88	175	221	261	ns
		C_L = 150 pF		113	225	284	335	
		C_L = 50 pF	4.5	18	35	44	52	
		C_L = 150 pF		23	45	57	67	
		C_L = 50 pF	6.0	15	30	37	44	
		C_L = 150 pF		19	38	48	57	
t_{PHL}		C_L = 50 pF	2.0	88	175	221	261	ns
		C_L = 150 pF		113	225	284	335	
		C_L = 50 pF	4.5	18	35	44	52	
		C_L = 150 pF		23	45	57	67	
		C_L = 50 pF	6.0	15	30	37	44	
		C_L = 150 pF		19	38	48	57	

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SWITCHING CHARACTERISTICS (Input $t_r = t_f = 6$ ns) (Continued)

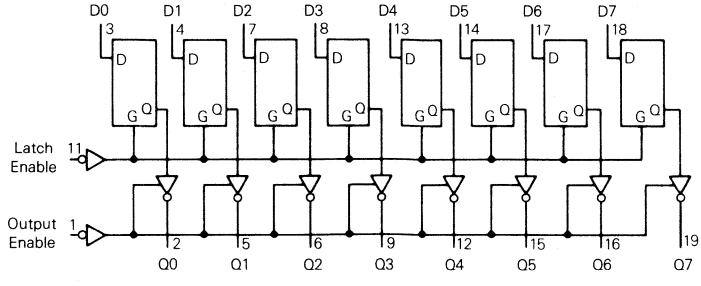
Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	$C_L = 50$ pF	2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PHZ}			2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PZL}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	$C_L = 50$ pF	2.0	75	150	189	224	ns
		$C_L = 150$ pF		100	200	252	298	
		$C_L = 50$ pF	4.5	15	30	38	45	
		$C_L = 150$ pF		20	40	50	60	
		$C_L = 50$ pF	6.0	13	26	32	38	
		$C_L = 150$ pF		17	34	43	51	
t_{PZH}		$C_L = 50$ pF	2.0	75	150	189	224	ns
		$C_L = 150$ pF		100	200	252	298	
		$C_L = 50$ pF	4.5	15	30	38	45	
		$C_L = 150$ pF		20	40	50	60	
		$C_L = 50$ pF	6.0	13	26	32	38	
		$C_L = 150$ pF		17	34	43	51	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	$C_L = 50$ pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{out}	Three-State Output Capacitance (Output Enable = V_{CC})		–	7.5	15	15	15	pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		–	50	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, Input D to Latch Enable (Figure 4)	2.0	−10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_h	Minimum Hold Time, Latch Enable to Input D (Figure 4)	2.0	25	50	63	75	ns
		4.5	5	10	13	15	
		6.0	4	9	11	13	
t_w	Minimum Pulse Width, Latch Enable (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

LOGIC DIAGRAM



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SWITCHING WAVEFORMS

FIGURE 1

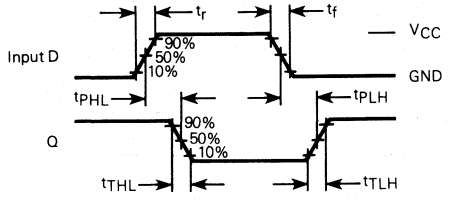


FIGURE 2

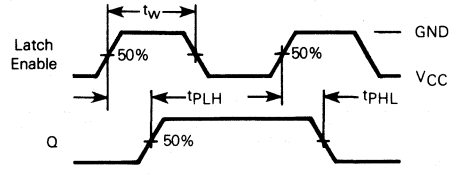


FIGURE 3

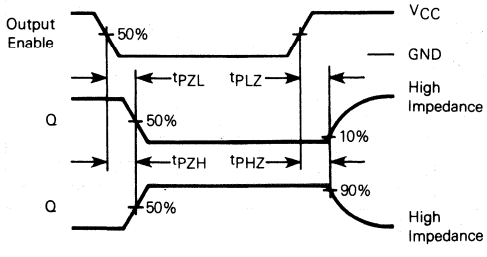


FIGURE 4

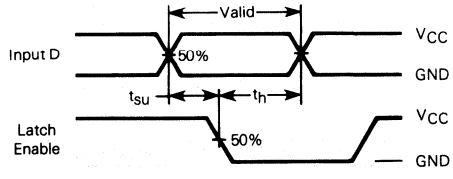


FIGURE 5 — TEST CIRCUIT

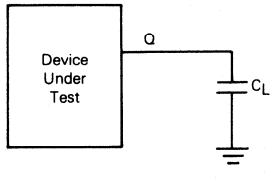
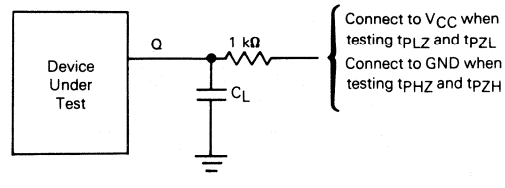


FIGURE 6 — TEST CIRCUIT



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MOTOROLA

MC54/74HC534

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

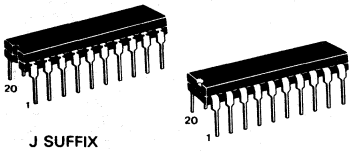
OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

The MC54/74HC534 is identical in pinout to the LS534. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data meeting the setup time is clocked, in inverted form, to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state. Data may thus be stored even when the device is not selected.

The HC534 is identical in function to the HC564, which has the input pins on the opposite side of the package from the output pins. The device is similar in function to the HC374, which has noninverting outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 732

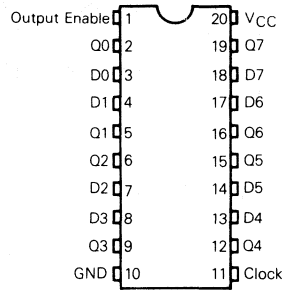
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

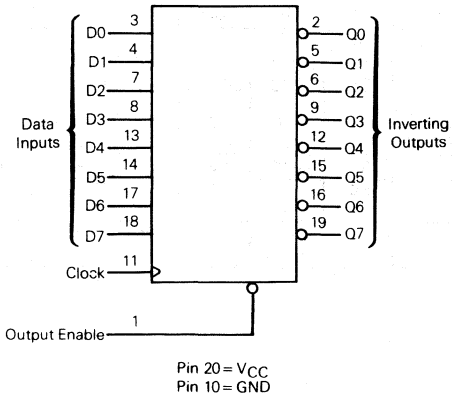
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



BLOCK DIAGRAM



Pin 20 = V_{CC}
Pin 10 = GND

FUNCTION TABLE

Inputs			Outputs
Output Enable	Clock	D	Q
L	↑	H	L
L	↑	L	H
L	L, H, ↓	X	no change
H	X	X	Z

X = don't care
Z = high impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C 54HC and 74HC	85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed		Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

5

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	C_L = 50 pF	65	35	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q	C_L = 50 pF	15	32	ns
t_{PHL}	(Figures 1 and 4)		15	32	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Q	C_L = 5 pF	13	25	ns
t_{PHZ}	(Figures 2 and 5)		13	25	
t_{PZL}	Maximum Propagation Delay, Output Enable to Q	C_L = 50 pF	14	28	ns
t_{PZH}	(Figures 2 and 5)		14	28	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	C_L = 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	C_L = 50 pF	2.0 4.5 6.0	12 60 71	6 30 35	5 24 28	4 20 24	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	C_L = 50 pF C_L = 150 pF	2.0	90 115	180 230	227 290	268 343	ns
		C_L = 50 pF C_L = 150 pF	4.5	18 23	36 46	45 58	54 69	
		C_L = 50 pF C_L = 150 pF	6.0	15 20	31 39	39 49	46 58	
t_{PHL}		C_L = 50 pF C_L = 150 pF	2.0	90 115	180 230	227 290	268 343	ns
		C_L = 50 pF C_L = 150 pF	4.5	18 23	36 46	45 58	54 69	
		C_L = 50 pF C_L = 150 pF	6.0	15 20	31 39	39 49	46 58	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	C_L = 50 pF	2.0 4.5 6.0	75 15 13	150 30 26	189 38 32	224 45 38	ns
t_{PHZ}			2.0 4.5 6.0	75 15 13	150 30 26	189 38 32	224 45 38	ns
t_{PZL}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	C_L = 50 pF C_L = 150 pF	2.0	75 100	150 200	189 252	224 298	ns
		C_L = 50 pF C_L = 150 pF	4.5	15 20	30 40	38 50	45 60	
		C_L = 50 pF C_L = 150 pF	6.0	13 17	26 34	32 43	38 51	
t_{PZH}		C_L = 50 pF C_L = 150 pF	2.0	75 100	150 200	189 252	224 298	ns
		C_L = 50 pF C_L = 150 pF	4.5	15 20	30 40	38 50	45 60	
		C_L = 50 pF C_L = 150 pF	6.0	13 17	26 34	32 43	38 51	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	C_L = 50 pF	2.0 4.5 6.0	30 6 5	60 12 10	75 15 13	90 18 15	ns
C_{out}	Three-State Output Capacitance (Output Enable = V_{CC})		–	7.5	15	15	15	pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance* (per Latch)		–	50	–	–	–	pF

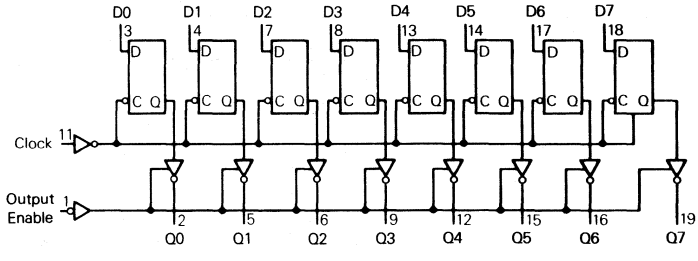
* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

5

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{su}	Minimum Setup Time, Input D to Clock (Figure 3)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Clock to Input D (Figure 3)	2.0	−10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

LOGIC DIAGRAM



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SWITCHING WAVEFORMS

FIGURE 1

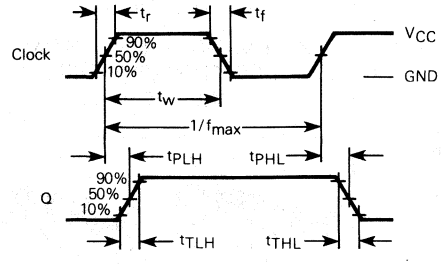


FIGURE 2

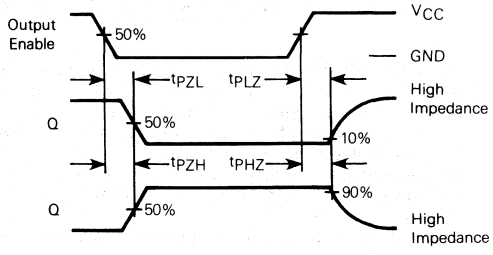


FIGURE 3

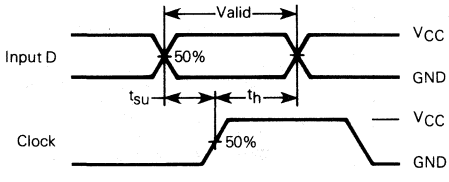


FIGURE 4 — TEST CIRCUIT

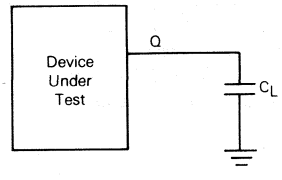
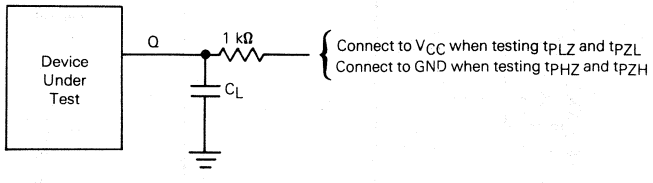


FIGURE 5 — TEST CIRCUIT



5

MOTOROLA

MC54/74HC540

Product Preview

OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/ LINE RECEIVER

The MC54/74HC540 is identical in pinout to the LS540. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal inverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device also features two ANDed active-low output enables, inverting outputs, and inputs and outputs on opposite sides of the package.

The HC540 is similar in function to the HC541, which has noninverting outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

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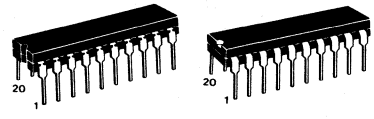
OCTAL 3-STATE INVERTING BUFFER/LINE DRIVER/ LINE RECEIVER



J SUFFIX
CERAMIC PACKAGE
CASE 732

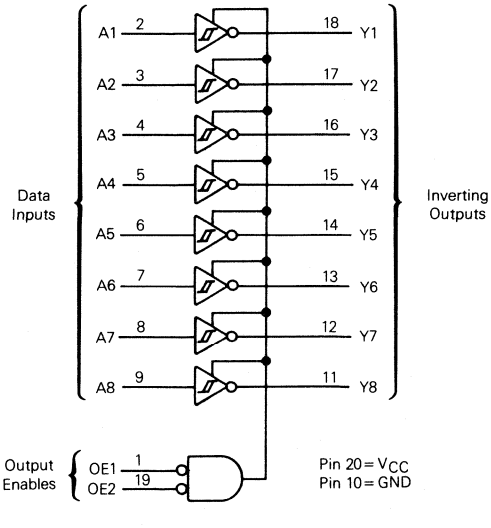
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

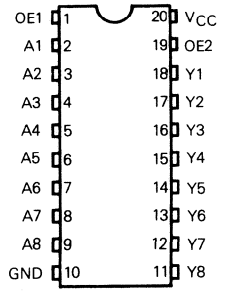
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs
OE1	OE2	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Z = High Impedance

5

MOTOROLA

MC54/74HC541

Product Preview

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/ LINE RECEIVER

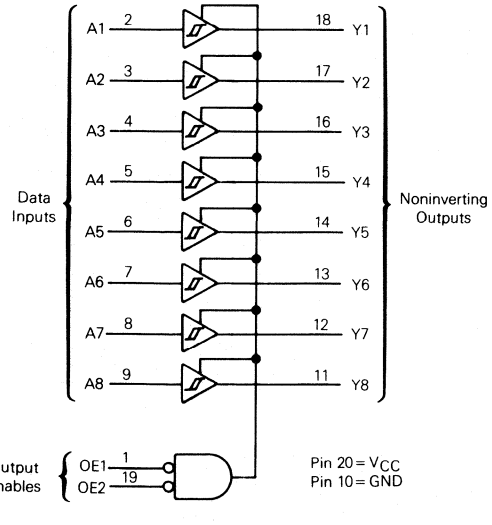
The MC54/74HC541 is identical in pinout to the LS541. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device also features two ANDed active-low output enables, noninverting outputs, and inputs and outputs on opposite sides of the package.

The HC541 is similar in function to the HC540, which has inverting outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

LOGIC DIAGRAM



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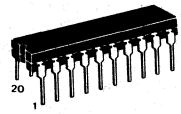
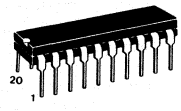
OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/ LINE RECEIVER



J SUFFIX
CERAMIC PACKAGE
CASE 732



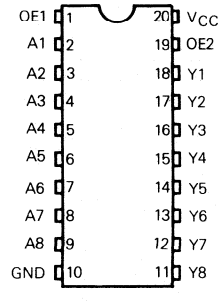
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Z = High Impedance

5

MOTOROLA

MC54/74HC563

Product Preview

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH

The MC54/74HC563 is identical in pinout to the LS563. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is identical in function to the HC533 but has the Data Inputs on the opposite side of the package from the outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. The data appears at the outputs in inverted form. When Latch Enable goes low, data meeting the set-up time becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all outputs are forced to the high-impedance state. Data may thus be latched even when the device is not selected.

The HC573 is the noninverting version of this function.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

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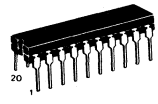
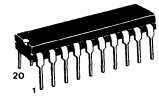
SILICON-GATE

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCH



J SUFFIX
CERAMIC PACKAGE
CASE 732



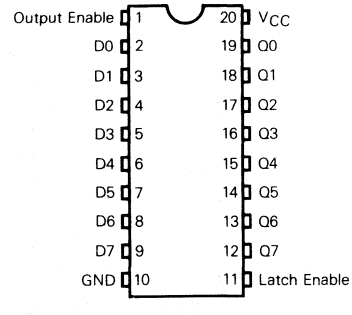
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

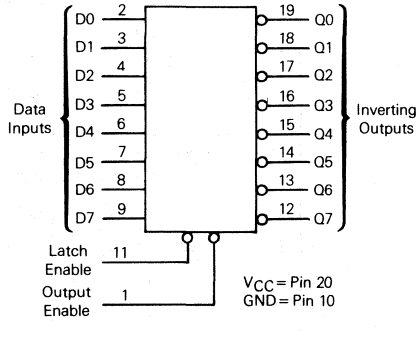
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



BLOCK DIAGRAM



FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	L
L	H	L	H
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

MOTOROLA

MC54/74HC564

Product Preview

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

The MC54/74HC564 is identical in pinout to the LS564. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

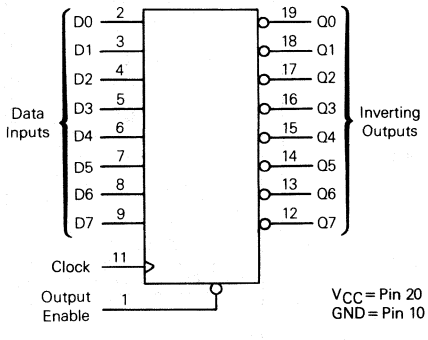
This device is identical in function to the HC534 but has the flip-flop inputs on the opposite side of the package from the outputs.

Data meeting the setup time is clocked, in inverted form, to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state. Data may thus be stored even when the device is not selected.

The HC574 is the noninverting version of the function.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM



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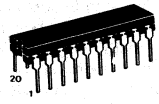
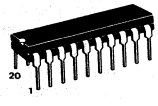
SILICON-GATE

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP



J SUFFIX
CERAMIC PACKAGE
CASE 732



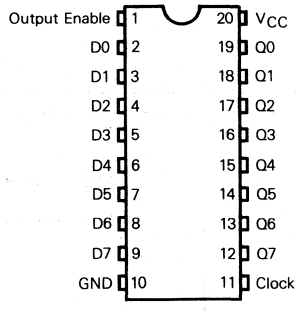
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Output Enable	Clock	D	Q
L	↑	H	L
L	↑	L	H
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

5

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MOTOROLA

MC54/74HC573

Product Preview

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH

The MC54/74HC573 is identical in pinout to the LS573. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup time becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all outputs are forced to the high-impedance state. Data may thus be latched even when the device is not selected.

This device is identical in function to the HC373 but has the Data Inputs on the opposite side of the package from the outputs.

The HC563 is the inverting version of this function.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

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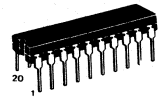
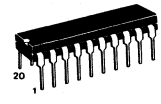
SILICON-GATE

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCH



J SUFFIX
CERAMIC PACKAGE
CASE 732



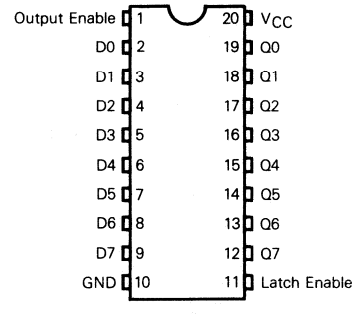
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



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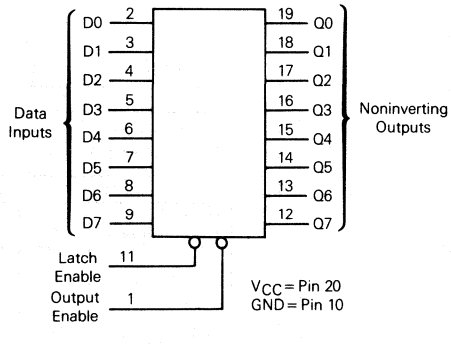


FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

MOTOROLA

MC54/74HC574

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOP

The MC54/74HC574 utilizes silicon-gate CMOS technology to achieve operating speeds similar to the LS574. The device can drive fifteen LSTTL loads. This Octal D-Type Flip-Flop also features the low power consumption, high noise immunity, and buffered outputs of standard CMOS integrated circuits.

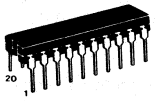
Data meeting the setup time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does nct affect the states of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state. Data may thus be stored even when the device is not selected.

The HC574 is identical in pinout to the LS574. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is identical in function to the HC374 but has the flip-flop inputs on the opposite side of the package from the outputs.

The HC564 is the inverting version of this function.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 732

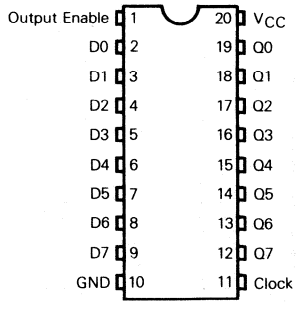
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



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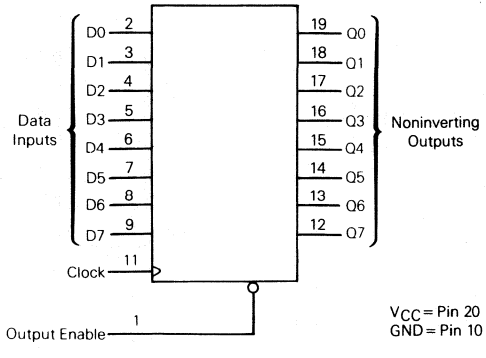


FUNCTION TABLE

Inputs			Output
Output Enable	Clock	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

5

MOTOROLA

MC54/74HC589

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

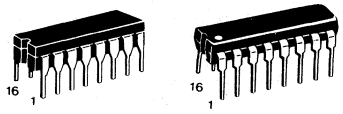
8-BIT SERIAL- OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER, WITH 3-STATE OUTPUT

8-BIT SERIAL- OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH 3-STATE OUTPUT

The MC54/74HC589 is similar in function to the HC597, which is not a 3-state device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of an 8-bit storage latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table). The shift register output, Q_H, is a three-state output, allowing this device to be used in bus-oriented systems.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620

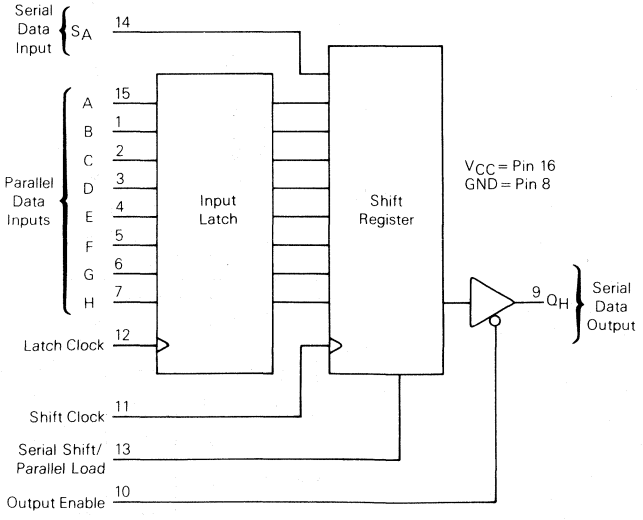
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

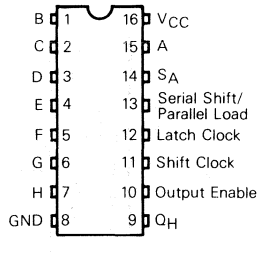
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 8)	C_L = 50 pF	60	30	MHz
t_{PLH}	Maximum Propagation Delay, Latch Clock to Q_H		18	35	ns
t_{PHL}	(Figures 1 and 8)	C_L = 50 pF	18	35	
t_{PLH}	Maximum Propagation Delay, Shift Clock to Q_H		16	30	ns
t_{PHL}	(Figures 2 and 8)	C_L = 50 pF	16	30	
t_{PLH}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q_H		16	30	ns
t_{PHL}	(Figures 4 and 8)	C_L = 50 pF	16	30	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Q_H		9	25	ns
t_{PHZ}	(Figures 3 and 9)	C_L = 5 pF	9	25	
t_{PZL}	Maximum Propagation Delay, Output Enable to Q_H		15	28	ns
t_{PZH}	(Figures 3 and 9)	C_L = 50 pF	15	28	
t_{TLH}, t_{THL}	Maximum Output Transition Time (Figures 1 and 8)	C_L = 50 pF	5	10	ns

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 8)	C_L = 50 pF	2.0	11	5	4	4	MHz
			4.5	54	27	21	18	
			6.0	64	32	25	21	
t_{PLH}	Maximum Propagation Delay, Latch Clock to Q_H (Figures 1 and 8)	C_L = 50 pF	2.0	105	210	265	313	ns
		C_L = 150 pF		130	260	328	387	
		C_L = 50 pF	4.5	21	42	53	63	
		C_L = 150 pF		26	52	66	77	
		C_L = 50 pF	6.0	18	36	45	53	
		C_L = 150 pF		22	44	56	66	
t_{PHL}		C_L = 50 pF	2.0	105	210	265	313	ns
		C_L = 150 pF		130	260	328	387	
		C_L = 50 pF	4.5	21	42	53	63	
		C_L = 150 pF		26	52	66	77	
		C_L = 50 pF	6.0	18	36	45	53	
		C_L = 150 pF		22	44	56	66	
t_{PLH}	Maximum Propagation Delay, Shift Clock to Q_H (Figures 2 and 8)	C_L = 50 pF	2.0	88	175	221	261	ns
		C_L = 150 pF		113	225	284	335	
		C_L = 50 pF	4.5	18	35	44	52	
		C_L = 150 pF		23	45	57	67	
		C_L = 50 pF	6.0	15	30	37	44	
		C_L = 150 pF		19	38	48	57	
t_{PHL}		C_L = 50 pF	2.0	88	175	221	261	ns
		C_L = 150 pF		113	225	284	335	
		C_L = 50 pF	4.5	18	35	44	52	
		C_L = 150 pF		23	45	57	67	
		C_L = 50 pF	6.0	15	30	37	44	
		C_L = 150 pF		19	38	48	57	
t_{PLH}	Maximum Propagation Delay, Serial Shift/ Parallel Load to Q_H (Figures 4 and 8)	C_L = 50 pF	2.0	88	175	221	261	ns
		C_L = 150 pF		113	225	284	335	
		C_L = 50 pF	4.5	18	35	44	52	
		C_L = 150 pF		23	45	57	67	
		C_L = 50 pF	6.0	15	30	37	44	
		C_L = 150 pF		19	38	48	57	
t_{PHL}		C_L = 50 pF	2.0	88	175	221	261	ns
		C_L = 150 pF		113	225	284	335	
		C_L = 50 pF	4.5	18	35	44	52	
		C_L = 150 pF		23	45	57	67	
		C_L = 50 pF	6.0	15	30	37	44	
		C_L = 150 pF		19	38	48	57	

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SWITCHING CHARACTERISTICS (Input $t_r = t_f = 6$ ns) (Continued)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{PLZ}	Maximum Propagation Delay, Output Enable to Q_H (Figures 3 and 9)	$C_L = 50$ pF	2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PHZ}			2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PZL}	Maximum Propagation Delay, Output Enalbe to Q_H (Figures 3 and 9)	$C_L = 50$ pF	2.0	75	150	189	224	ns
		$C_L = 150$ pF		100	200	252	298	
		$C_L = 50$ pF	4.5	15	30	38	45	
		$C_L = 150$ pF		20	40	50	60	
		$C_L = 50$ pF	6.0	13	26	32	38	
		$C_L = 150$ pF		17	34	43	51	
t_{PZH}		$C_L = 50$ pF	2.0	75	150	189	224	ns
		$C_L = 150$ pF		100	200	252	298	
		$C_L = 50$ pF	4.5	15	30	38	45	
		$C_L = 150$ pF		20	40	50	60	
		$C_L = 50$ pF	6.0	13	26	32	38	
		$C_L = 150$ pF		17	34	43	51	
t_{TLH}, t_{THL}	Maximum Output Transition Time (Figures 1 and 8)	$C_L = 50$ pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{out}	Three-State Output Capacitance (Output Enable = V_{CC})		–	7.5	15	15	15	pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		–		–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{su}	Minimum Setup Time, A-H to Latch Clock (Figure 5)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_{su}	Minimum Setup Time, Serial Data Input, S_A to Shift Clock (Figure 6)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_{su}	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock (Figure 7)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Latch Clock to A-H (Figure 5)	2.0	13	25	32	37	ns
		4.5	3	5	6	7	
		6.0	2	4	5	6	
t_h	Minimum Hold Time, Shift Clock to Serial Data Input, S_A (Figure 6)	2.0	−10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_h	Minimum Hold Time, Shift Clock to Serial Shift/Parallel Load (Figure 7)	2.0	−10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_w	Minimum Pulse Width, Shift Clock (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Latch Clock and Serial Shift/ Parallel Load (Figures 1 and 4)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

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FUNCTION TABLE

Inputs						Output	
Output Enable	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	S_A	A-H	Output Q_H	Resulting Function
H	X	X	X	X	X	Z	Q_H is in the high impedance state.
L	H	↗	L, H, ↘	X	a-h	no change	Parallel Data is stored in the input latch. The state of the shift register is unaffected.
L	L	↗	X	X	a-h	h	Parallel Data is stored in the input latch and loaded into the shift register.
L	L	L, H, ↘	L, H, ↘	X	X	h_L*	Parallel Data stored in the input latch is loaded into the shift register.
L	H	X	↗	L	X	Q_{Gn}	A low logic level is shifted into the shift register.
L	H	X	↗	H	X	Q_{Gn}	A high logic level is shifted into the shift register.
L	H	↗	↗	L, H	a-h	Q_{Gn}	Serial data is shifted into the shift register and parallel data is stored in the input latch.

*h_L = the data stored in stage H of the input latch.
X = don't care
Q_{Gn} = Data shifted from stage G
a-h = Data at inputs A-H, respectively
Z = High Impedance State

SWITCHING WAVEFORMS AND TEST CIRCUITS

FIGURE 1 — (SERIAL SHIFT/PARALLEL LOAD = L)

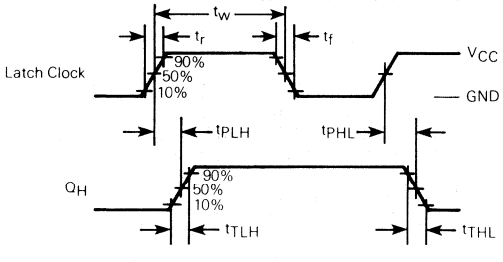

FIGURE 2 — (SERIAL SHIFT/PARALLEL LOAD = H)

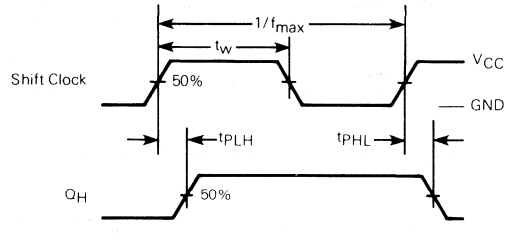

FIGURE 3

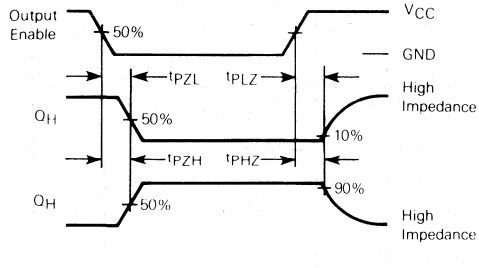

FIGURE 4

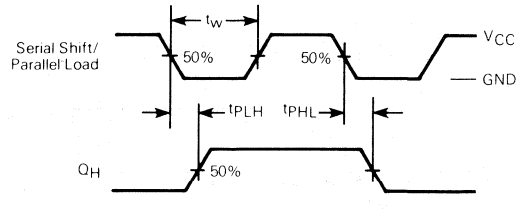

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FIGURE 5

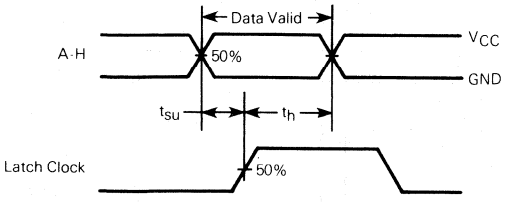


FIGURE 6

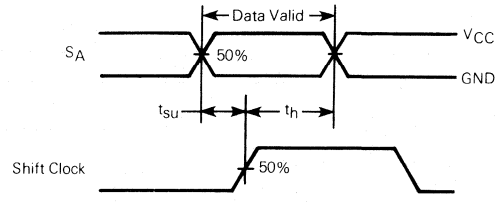


FIGURE 7

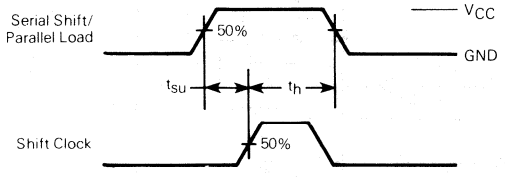


FIGURE 8 — TEST CIRCUIT

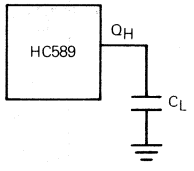
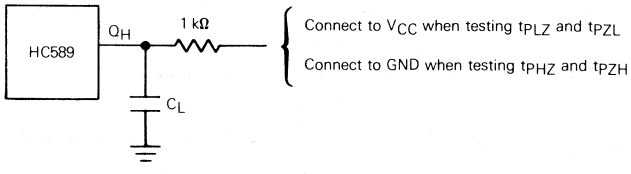


FIGURE 9 — TEST CIRCUIT



PIN DESCRIPTIONS

DATA INPUTS

A, B, C, D, E, F, G, H (PINS 15, 1, 2, 3, 4, 5, 6, 7) — Parallel data inputs. Data on these inputs are stored in the input latch on the rising edge of the Latch Clock input.

S_A (PIN 14) — Serial Data Input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

CONTROL INPUTS

SERIAL SHIFT/PARALLEL LOAD (PIN 13) — Shift register mode control. When a high logic level is applied to this pin, the shift register is allowed to serially shift data. When a low logic level is applied to this pin, the shift register accepts parallel data from the input latch.

SHIFT CLOCK (PIN 11) — Serial shift clock. A low-to-high transition on this input shifts data on the Serial Data input into the shift register and data in stage H is shifted out Q_H, being replaced by the data previously stored in stage G.

LATCH CLOCK (PIN 12) — Input latch clock. A low-to-high transition on this input loads the parallel data on inputs A-H into the input latch.

OUTPUT ENABLE (PIN 10) — Active-low output enable. A high logic level applied to this pin forces the Q_H output into the high impedance state. A low logic level applied enables the output. This control does not affect the state of the input latch or the shift register.

OUTPUT

Q_H (PIN 9) — Serial data output. This pin is the output from the last stage of the shift register. This is a 3-state output.

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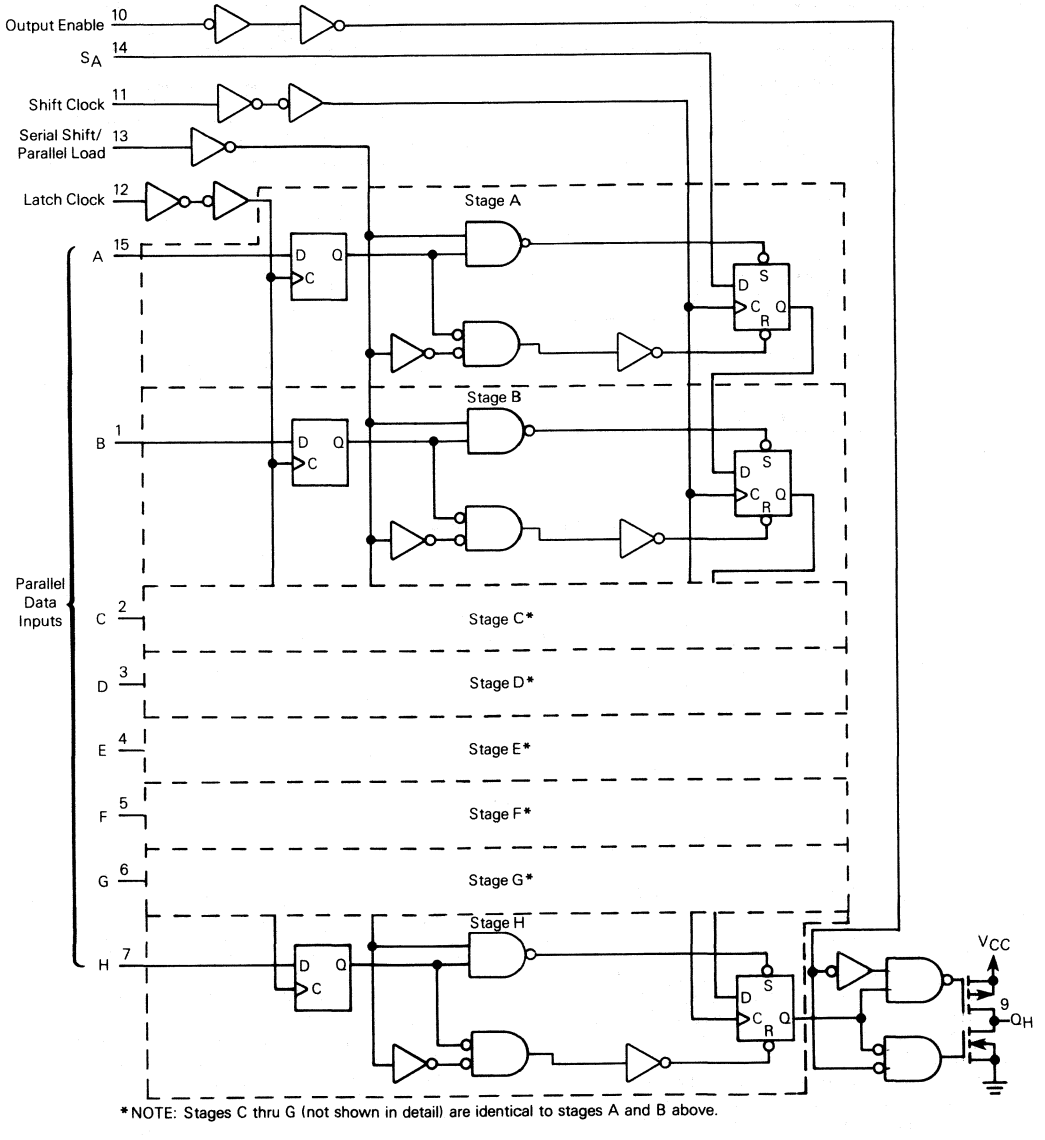
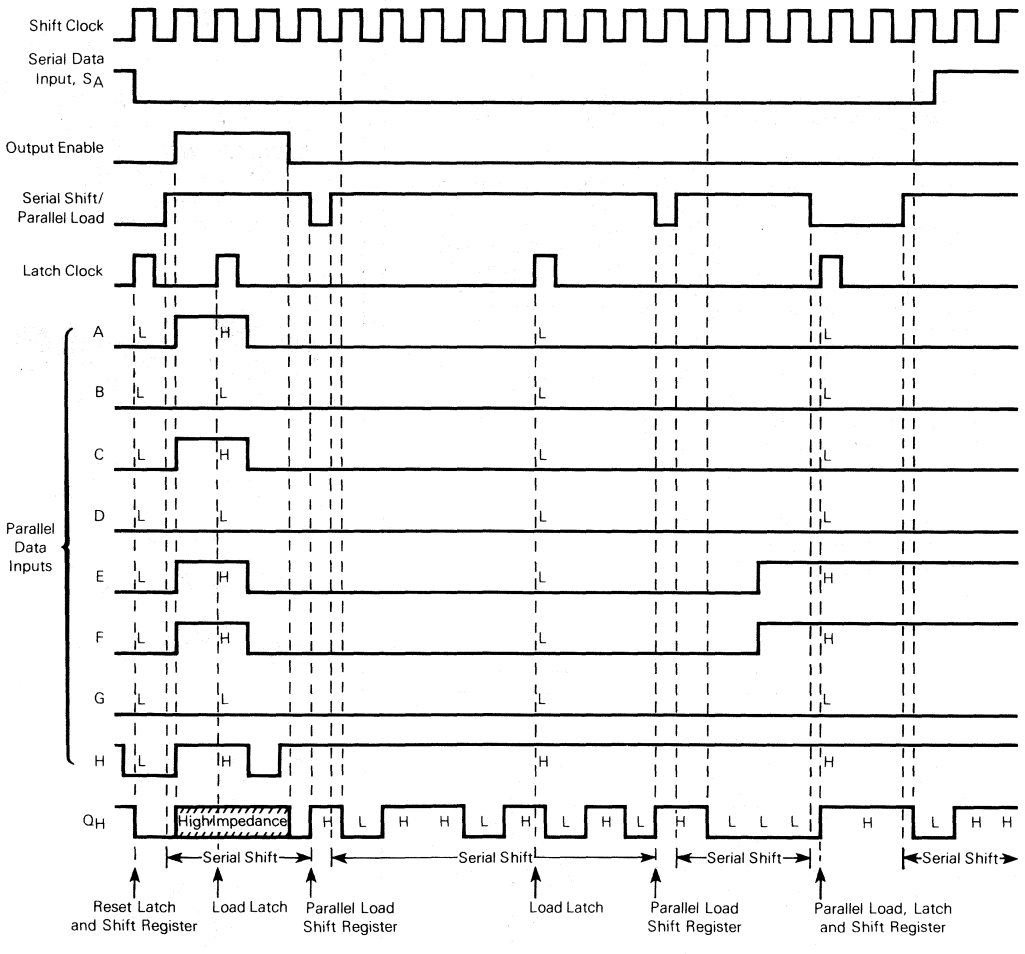
LOGIC DIAGRAM



*NOTE: Stages C thru G (not shown in detail) are identical to stages A and B above.

TIMING DIAGRAM



MOTOROLA

MC54/74HC595

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

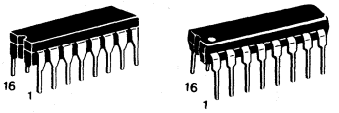
8-BIT SERIAL-INPUT/SERIAL- OR PARALLEL-OUTPUT SHIFT REGISTER WITH LATCHED 3-STATE OUTPUTS

8-BIT SERIAL-INPUT/SERIAL- OR PARALLEL-OUTPUT SHIFT REGISTER WITH LATCHED 3-STATE OUTPUTS

The MC54/74HC595 is identical in pinout to the LS595. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC595 consists of an 8-bit serial shift register and an 8-bit D-type latch with three-state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8-bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum for SQ_H
- Output Drive Capability: 15 LSTTL Loads Minimum for Q_A-Q_H
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620

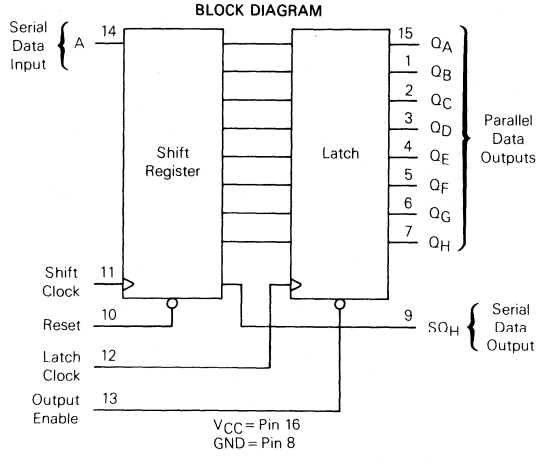
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

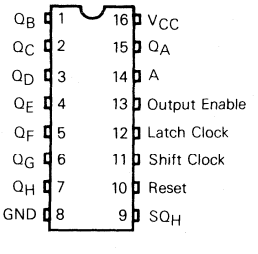
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin, Q_A-Q_H	±35	mA
I_{out}	DC Output Current, per Pin, SQ_H	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C 54HC and 74HC		85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed			Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage, Q_A-Q_H	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage, Q_A-Q_H	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
V_{OH}	Minimum High-Level Output Voltage, SQ_H	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage, SQ_H	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Shift Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	C_L = 50 pF		30	MHz
t_{PLH}	Maximum Propagation Delay, Shift Clock to SQ_H	C_L = 15 pF		35	ns
t_{PHL}	(Figures 1 and 7)			35	
t_{PHL}	Maximum Propagation Delay, Reset to SQ_H (Figures 2 and 7)	C_L = 15 pF		30	ns
t_{PLH}	Maximum Propagation Delay, Latch Clock to Q	C_L = 50 pF		30	ns
t_{PHL}	(Figures 3 and 7)			30	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Q	C_L = 5 pF		25	ns
t_{PHZ}	(Figures 4 and 8)			25	
t_{PZL}	Maximum Propagation Delay, Output Enable to Q			28	ns
t_{PZH}	(Figures 4 and 8)	C_L = 50 pF		28	
t_{TLH},	Maximum Output Transition Time, SQ_H	C_L = 15 pF	5	10	ns
t_{THL}	(Figures 1 and 7) Q_A-Q_H	C_L = 50 pF	5	10	

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Shift Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	C_L = 50 pF	2.0	11	5	4	4	MHz
			4.5	54	27	21	18	
			6.0	64	32	25	21	
t_{PLH}	Maximum Propagation Delay, Shift Clock to SQ_H (Figures 1 and 7)	C_L = 50 pF	2.0	105	210	265	313	ns
			4.5	21	42	53	63	
			6.0	18	36	45	53	
t_{PHL}			2.0	105	210	265	313	ns
			4.5	21	42	53	63	
			6.0	18	36	45	53	
t_{PHL}	Maximum Propagation Delay, Reset to SQ_H (Figures 2 and 7)	C_L = 50 pF	2.0	88	175	221	261	ns
			4.5	18	35	44	52	
			6.0	15	30	37	44	
t_{PLH}	Maximum Propagation Delay, Latch Clock to Q (Figures 3 and 7)	C_L = 50 pF	2.0	88	175	221	261	ns
		C_L = 150 pF		113	225	284	335	
		C_L = 50 pF	4.5	18	35	44	52	
		C_L = 150 pF		23	45	57	67	
		C_L = 50 pF	6.0	15	30	37	44	
		C_L = 150 pF		19	38	48	57	
t_{PHL}		C_L = 50 pF	2.0	88	175	221	261	ns
		C_L = 150 pF		113	225	284	335	
		C_L = 50 pF	4.5	18	35	44	52	
		C_L = 150 pF		23	45	57	67	
		C_L = 50 pF	6.0	15	30	37	44	
		C_L = 150 pF		19	38	48	57	

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SWITCHING CHARACTERISTICS (Input $t_r = t_f = 6$ ns) (Continued)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLZ}	Maximum Propagation Delay, Output Enable to Q (Figures 4 and 8)	$C_L = 50$ pF	2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PHZ}			2.0	75	150	189	224	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t_{PZL}	Maximum Propagation Delay, Output Enable to Q (Figures 4 and 8)	$C_L = 50$ pF	2.0	75	150	189	224	ns
		$C_L = 150$ pF		100	200	252	298	
		$C_L = 50$ pF	4.5	15	30	38	45	
		$C_L = 150$ pF		20	40	50	60	
		$C_L = 50$ pF	6.0	13	26	32	38	
		$C_L = 150$ pF		17	34	43	51	
t_{PZH}		$C_L = 50$ pF	2.0	75	150	189	224	ns
		$C_L = 150$ pF		100	200	252	298	
		$C_L = 50$ pF	4.5	15	30	38	45	
		$C_L = 150$ pF		20	40	50	60	
		$C_L = 50$ pF	6.0	13	26	32	38	
		$C_L = 150$ pF		17	34	43	51	
t_{TLH}, t_{THL}	Maximum Output Transition Time, SQ_H (Figures 1 and 7)	$C_L = 50$ pF	2.0	38	75	95	110	ns
			4.5	8	15	19	22	
			6.0	6	13	16	19	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Q_A-Q_H (Figures 1 and 7)	$C_L = 50$ pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{out}	Three-State Output Capacitance (Output Enable = V_{CC})		–	7.5	15	15	15	pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		–	310	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_{su}	Minimum Setup Time, Shift Clock to Latch Clock (Figure 8)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0	– 10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0	25	50	63	75	ns
		4.5	5	10	13	15	
		6.0	4	9	11	13	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Shift Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Latch Clock (Figure 8)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

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FUNCTION TABLE

Inputs					Resulting Function
Reset	A	Shift Clock	Latch Clock	Output Enable	
L	X	X	X	X	Shift register contents are cleared.
H	L	↑	X	X	A low logic level is shifted into the shift register.
H	H	↑	X	X	A high logic level is shifted into the shift register.
H	X	↓	X	X	Shift register remains unchanged.
H	X	L	↑	X	Shift register data stored in the 8-bit latch.
H	X	L	↓	X	Data latch remains unchanged.
H	X	L	L	L	Latch Outputs, Q_A-Q_H, are enabled.
H	X	L	L	H	Outputs Q_A-Q_H are in the high impedance state.

PIN DESCRIPTIONS

INPUTS

A (Pin 14) — Serial Data Input. The data on this pin is shifted into the 8-bit serial shift register.

CONTROL INPUTS

Shift Clock (Pin 11) — Shift Register Clock Input. A low-to-high transition on this input causes the data at the Serial Input pin to be shifted into the 8-bit shift register.

Reset (Pin 10) — Active-low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8-bit latch is not affected.

Latch Clock (Pin 12) — Storage Latch Clock Input. A low-to-high transition on this input latches the shift register data.

Output Enable (Pin 13) — Active-low Output Enable. A low on this input allows the data from the latches to be presented at the outputs. A high on this input forces the outputs (Q_A-Q_H) into the high-impedance state. The serial output is not affected by this control input.

OUTPUTS

Q_A-Q_H (Pins 15, 1, 2, 3, 4, 5, 6, 7) — Noninverted, 3-state, latch outputs.

SQ_H (Pin 9) — Noninverted, Serial Data Output. This is the output of the eighth stage of the 8-bit shift register. This output does not have three-state capability.

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SWITCHING WAVEFORMS

FIGURE 1

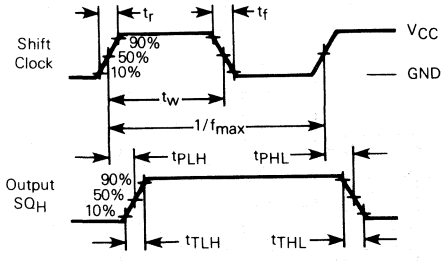


FIGURE 2

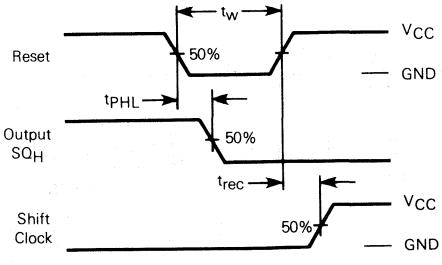


FIGURE 3

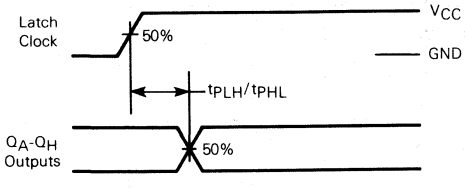


FIGURE 4

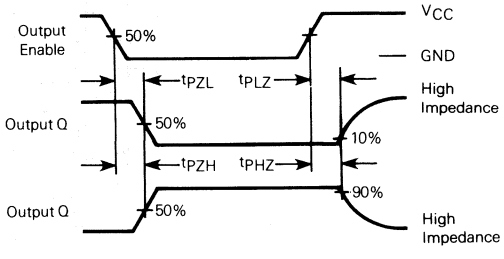


FIGURE 5

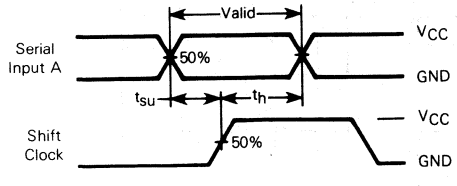


FIGURE 6

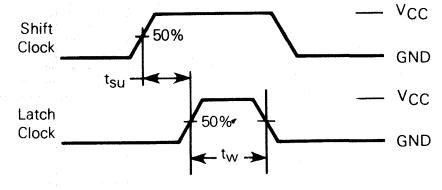


FIGURE 7 — TEST CIRCUIT

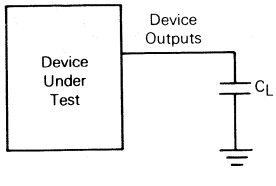
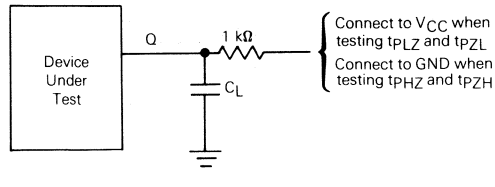
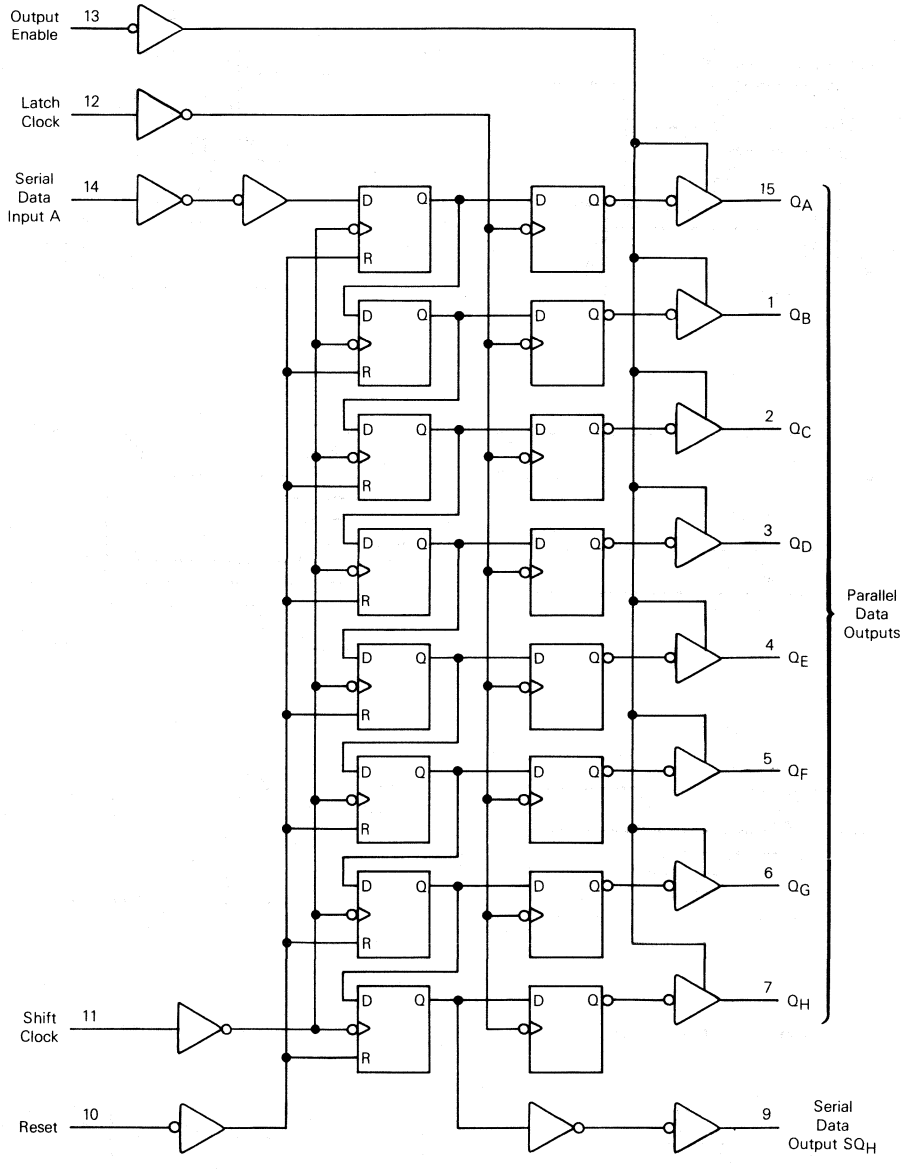


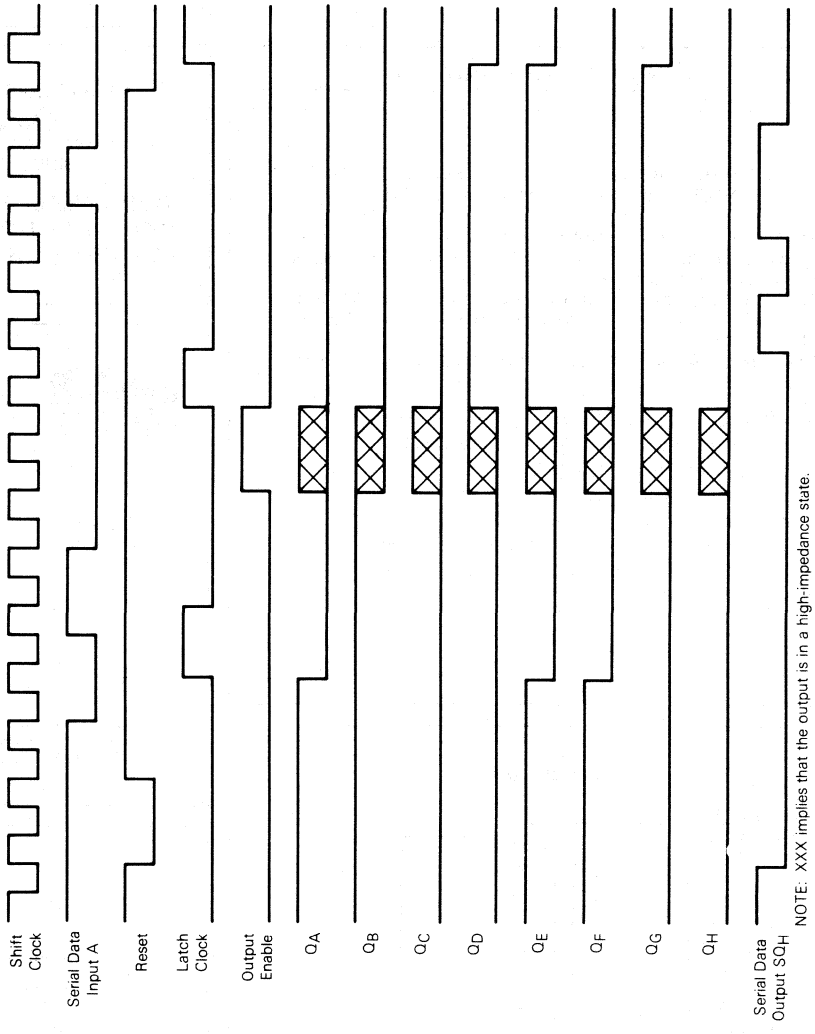
FIGURE 8 — TEST CIRCUIT



LOGIC DIAGRAM



TIMING DIAGRAM



NOTE: XXX implies that the output is in a high-impedance state.

MOTOROLA

MC54/74HC597

Advance Information

8-BIT SERIAL- OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH INPUT LATCH

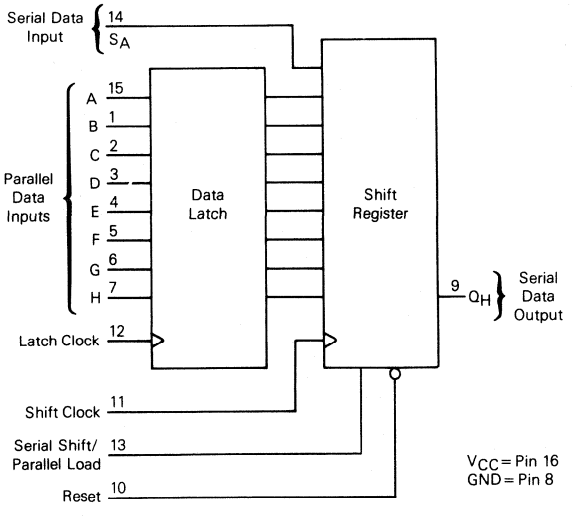
The MC54/74HC597 is identical in pinout to the LS597. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of an 8-bit input latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table).

The HC597 is similar in function to the HC589, which is a 3-state device.

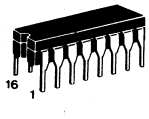
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM

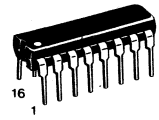


HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

8-BIT SERIAL- OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH INPUT LATCH



J SUFFIX
CERAMIC PACKAGE
CASE 620



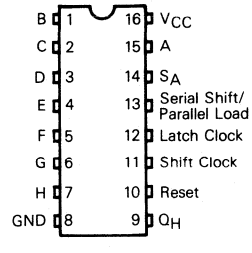
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 8)		30	MHz
t_{PLH}	Maximum Propagation Delay, Latch Clock to Q_H		35	ns
t_{PHL}	(Figures 1 and 8)		35	
t_{PLH}	Maximum Propagation Delay, Shift Clock to Q_H		30	ns
t_{PHL}	(Figures 2 and 8)		30	
t_{PHL}	Maximum Propagation Delay, Reset to Q_H (Figures 3 and 8)		30	ns
t_{PLH}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q_H		30	ns
t_{PHL}	(Figures 4 and 8)		30	
t_{TLH}, t_{THL}	Maximum Output Transition Time (Figures 1 and 8)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 8)	2.0	11	5	4	4	MHz
		4.5	54	27	21	18	
		6.0	64	32	25	21	
t_{PLH}	Maximum Propagation Delay, Latch Clock to Q_H (Figures 1 and 8)	2.0	105	210	265	313	ns
		4.5	21	42	53	63	
		6.0	18	36	45	53	
t_{PHL}		2.0	105	210	265	313	ns
		4.5	21	42	53	63	
		6.0	18	36	45	53	
t_{PLH}	Maximum Propagation Delay, Shift Clock to Q_H (Figures 2 and 8)	2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PHL}		2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PHL}	Maximum Propagation Delay, Reset to Q_H (Figures 3 and 8)	2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PLH}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q_H (Figures 4 and 8)	2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PHL}		2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{TLH}, t_{THL}	Maximum Output Transition Time (Figures 1 and 8)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	45	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{su}	Minimum Setup Time, A-H to Latch Clock (Figure 5)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_{su}	Minimum Setup Time, Serial Data Input, S_A to Shift Clock (Figure 6)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_{su}	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock (Figure 7)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Latch Clock to A-H (Figure 5)	2.0	13	25	32	37	ns
		4.5	3	5	6	7	
		6.0	2	4	5	6	
t_h	Minimum Hold Time, Shift Clock to Serial Data Input, S_A (Figure 6)	2.0	−10	5	5	5	ns
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_h	Minimum Hold Time, Shift Clock to Serial Shift/Parallel Load (Figure 7)	2.0					ns
		4.5					
		6.0					
t_{rec}	Minimum Recovery Time, Reset (Inactive) to Shift Clock (Figure 3)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_w	Minimum Pulse Width, Shift Clock (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Latch Clock, Reset and Serial Shift/ Parallel Load (Figures 1, 3, and 4)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

FUNCTION TABLE

Inputs						Output	
Reset	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	S_A	A-H	Q_H	Resulting Function
L	X	X	X	X	X	L	Shift register is reset. Input latch is unaffected.
H	H	⌐	L, H, ¬	X	a-h	no change	Parallel Data is stored in Input Latch. The state of the shift register is unaffected.
H	L	⌐	X	X	a-h	h	Parallel Data is stored in the input latch and loaded into the shift register.
H	L	L, H, ¬	L, H, ¬	X	X	h_L*	Parallel Data stored in the input latch is loaded into the shift register.
H	H	X	⌐	L	X	Q_{Gn}	A low logic level is shifted into the shift register.
H	H	X	⌐	H	X	Q_{Gn}	A high logic level is shifted into the shift register.
H	H	⌐	⌐	L, H	a-h	Q_{Gn}	Serial data is shifted into the shift register and parallel data is stored in the input latch.

* h_L = the data stored in stage H of the input latch.
X = don't care
Q_{Gn} = Data shifted from stage G
a-h = Data at inputs A-H, respectively

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SWITCHING WAVEFORMS AND TEST CIRCUIT

FIGURE 1 — (Serial Shift Parallel Load = L)

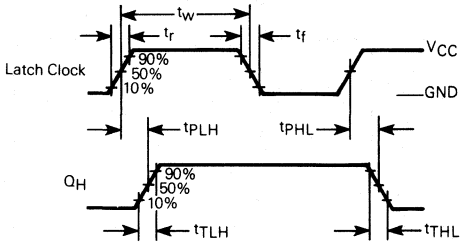

FIGURE 2 — (Serial Shift Parallel Load = H)

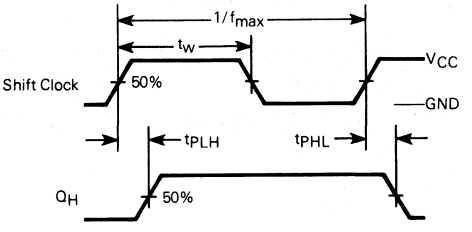

FIGURE 3

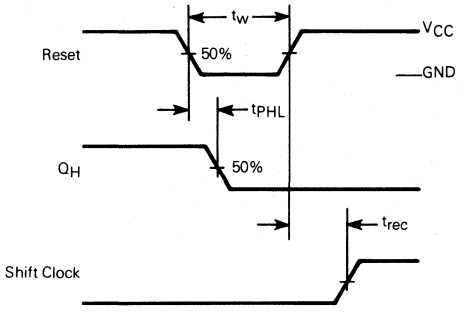

FIGURE 4

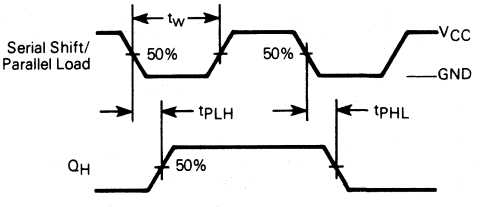

FIGURE 5

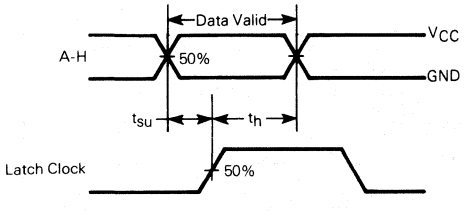

FIGURE 6

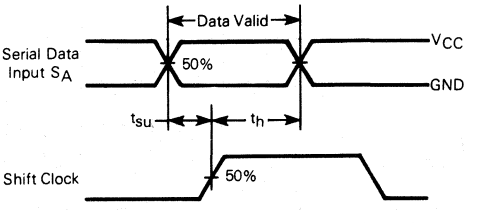

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FIGURE 7

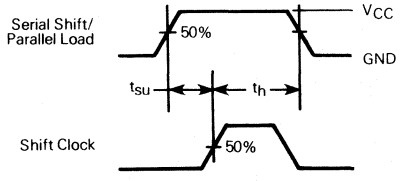
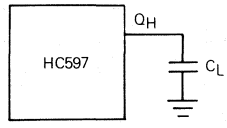


FIGURE 8 — TEST CIRCUIT



PIN DESCRIPTIONS

DATA INPUTS

A, B, C, D, E, F, G, H (PINS 15, 1, 2, 3, 4, 5, 6, 7) — Parallel data inputs. Data on these inputs is stored in the input latch on the rising edge of the Latch Clock input.

S_A (PIN 14) — Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift /Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

CONTROL INPUTS

SERIAL SHIFT/PARALLEL LOAD (PIN 13) — Shift register mode control. When a high logic level is applied to this pin, the shift register is allowed to serially shift data. When a low logic level is applied to this pin, the shift register accepts parallel data from the iput latch, and serial shifting is inhibited.

RESET (PIN 10) — Asynchronous, Active-low shift register reset. A low logic level applied to this input resets the shift register to a low level, but does not change the data in the input latch.

SHIFT CLOCK (PIN 11) — Serial shift register clock. A low-to-high transition on this input shifts data on the Serial Data Input into the shift register and data in stage H is shifted out Q_H, being replaced by the data previously stored in stage G.

LATCH CLOCK (PIN 12) — Latch clock. A low-to-high transition on this input loads the parallel data on inputs A-H into the input latch.

OUTPUT

Q_H (PIN 9) — Serial data output. This pin is the output from the last stage of the shift register.

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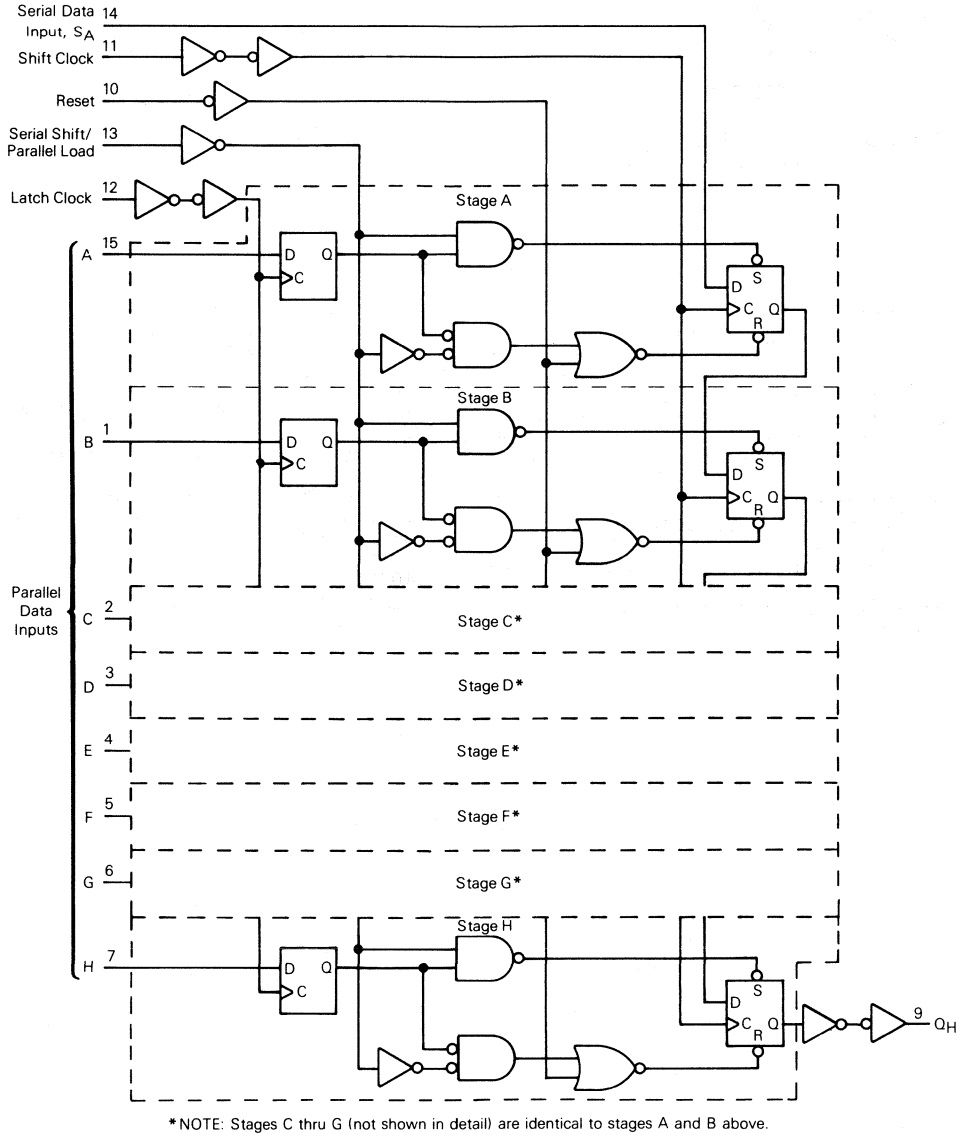
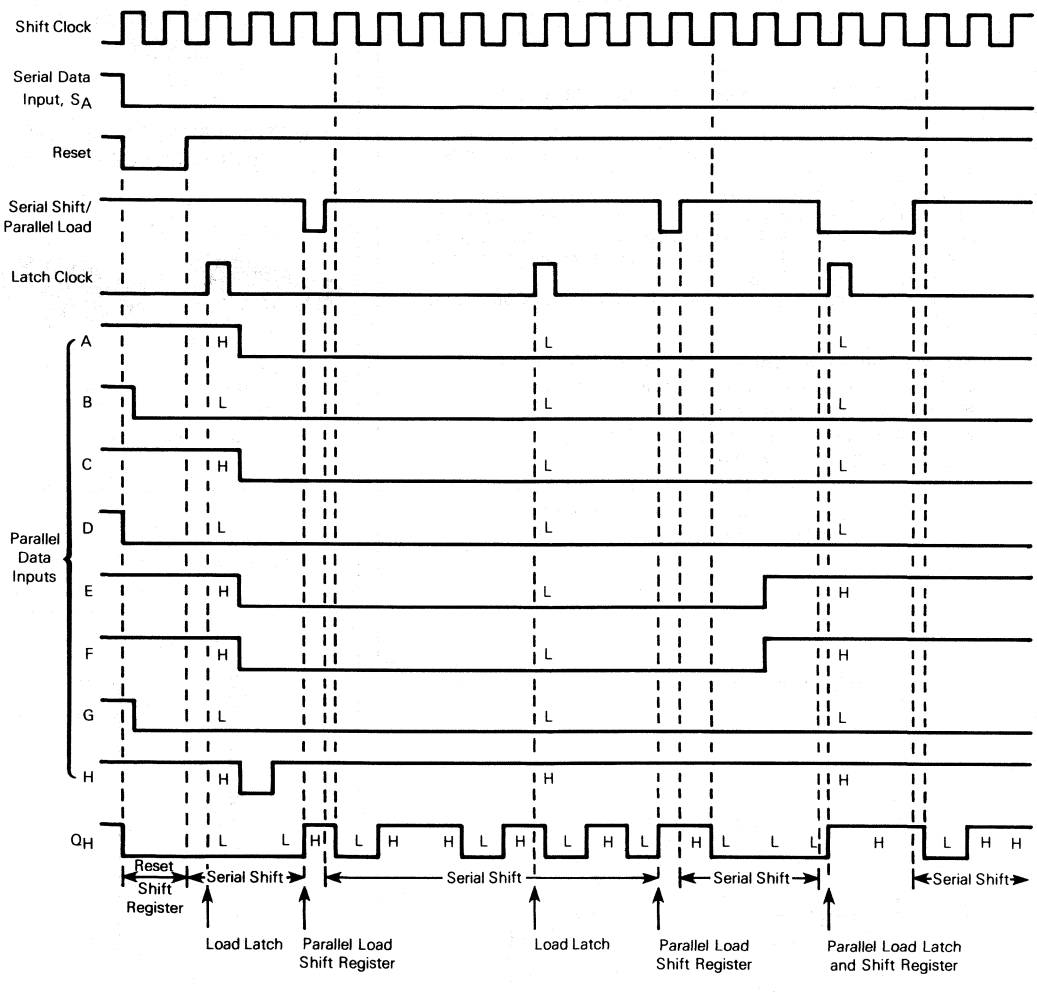
LOGIC DIAGRAM



*NOTE: Stages C thru G (not shown in detail) are identical to stages A and B above.

TIMING DIAGRAM



MOTOROLA

MC54/74HC640

Product Preview

OCTAL 3-STATE INVERTING BUS TRANSCEIVER

The MC54/74HC640 is identical in pinout to the LS640. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

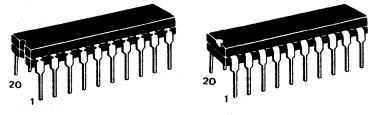
The HC640 is a 3-state inverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HC640 performs functions similar to those of the HC245 and the HC643.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE INVERTING BUS TRANSCEIVER



J SUFFIX
CERAMIC PACKAGE
CASE 732

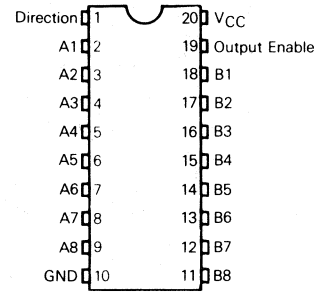
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

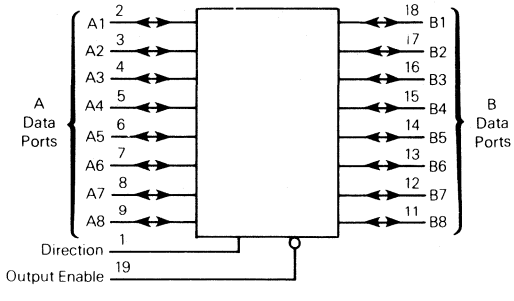
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

PIN ASSIGNMENT



BLOCK DIAGRAM



FUNCTION TABLE

Control Inputs		
Output Enable	Direction	Operation
L	L	Data transmitted from Bus B to Bus A (inverted)
L	H	Data transmitted from Bus A to Bus B (inverted)
H	X	Buses Isolated (High-Impedance State)

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

MC54/74HCT640

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE INVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

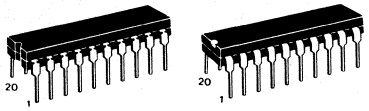
OCTAL 3-STATE INVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

The HCT640 may be used as a level converter for interfacing LSTTL to High-Speed CMOS. The inputs of HCT devices are compatible with both LSTTL and CMOS output voltage levels.

The HCT640 is a 3-state inverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HCT640 performs functions similar to those of the HCT245 and the HCT643.

- Compatible with LSTTL Outputs — No Pullup Resistor Required
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Voltage Range: 4.5 to 5.5 Volts
- Low Quiescent Current Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 732

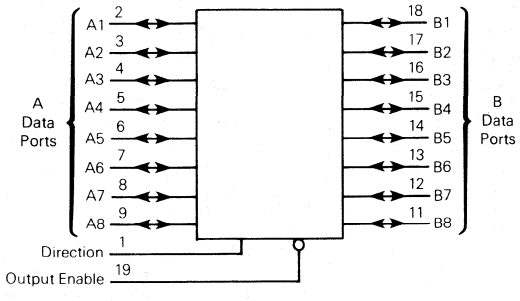
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

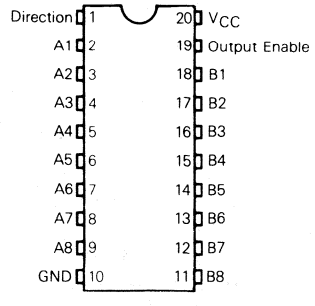
54 Series: −55°C to +125°C
MC54HCTXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCTXXXN (Plastic Package)
MC74HCTXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs		
Output Enable	Direction	Operation
L	L	Data transmitted from Bus B to Bus A (inverted)
L	H	Data transmitted from Bus A to Bus B (inverted)
H	X	Buses Isolated (High-Impedance State)

X = Don't Care

MOTOROLA

MC54/74HC643

Product Preview

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

The MC54/74HC643 is identical in pinout to the LS643. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC643 is a 3-state transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

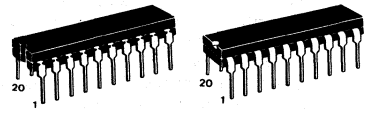
The HC643 performs functions similar to those of the HC245 and the HC640.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE CMOS

LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER



J SUFFIX
CERAMIC PACKAGE
CASE 732

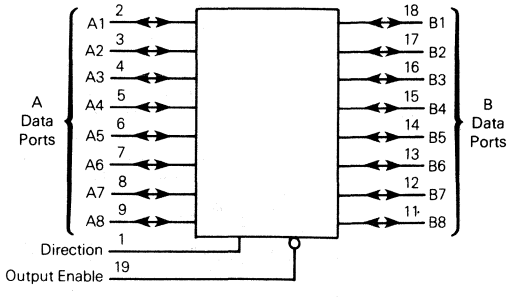
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

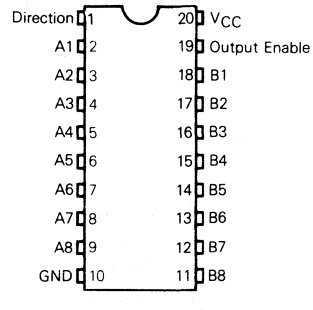
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs		
Output Enable	Direction	Operation
L	L	Data transmitted from Bus B to Bus A (not inverted)
L	H	Data transmitted from Bus A to Bus B (inverted)
H	X	Buses Isolated (High-Impedance State)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MOTOROLA

MC54/74HCT643

Product Preview

OCTAL 3-STATE INVERTING AND NONINVERTING) BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS

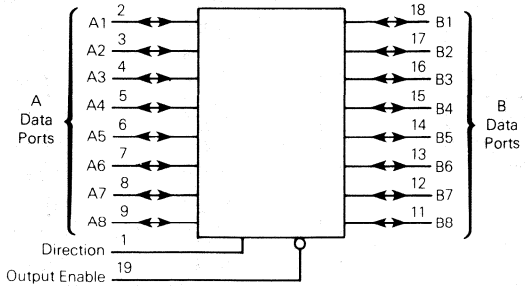
The HCT643 may be used as a level converter for interfacing LSTTL to High-Speed CMOS. The inputs of HCT devices are compatible with both LSTTL and CMOS output voltage levels.

The HCT643 is a 3-state transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HCT643 performs functions similar to those of the HCT245 and the HCT640.

- Compatible with LSTTL Outputs — No Pullup Resistor Required
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Voltage Range: 4.5 to 5.5 Volts
- Low Quiescent Current Characteristic of CMOS Devices
- Diode Protection on All Inputs

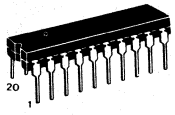
BLOCK DIAGRAM



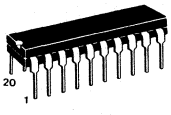
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER WITH LSTTL-COMPATIBLE INPUTS



J SUFFIX
CERAMIC PACKAGE
CASE 732



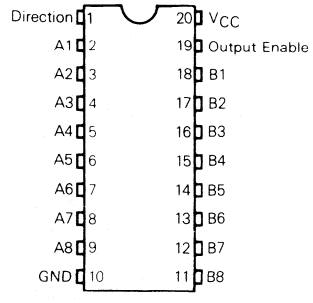
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCTXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCTXXXN (Plastic Package)
MC74HCTXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs		
Output Enable	Direction	Operation
L	L	Data transmitted from Bus B to Bus A (not inverted)
L	H	Data transmitted from Bus A to Bus B (inverted)
H	X	Buses Isolated (High-Impedance State)

X = Don't Care

5

MOTOROLA

MC54/74HC646
MC54/74HC648

Advance Information

OCTAL 3-STATE BUS TRANSCEIVERS AND D-TYPE FLIP-FLOPS

The MC54/74HC646 and the MC54/74HC648 are identical in pinout to the LS646 and LS648. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices are bus transceivers with D-type flip-flops. Depending upon the states of the Data-Source Selection inputs, data may be routed to the outputs either from the flip-flops or directly from the inputs (see Function Table and Pin Descriptions).

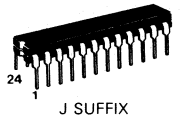
The Output Enable and the Direction pins control the transceiver function. Only one of the two buses, A or B, may be enabled as outputs at any time. However, when either or both of the outputs are in the high-impedance state, the pins may be used as inputs to the D-type flip-flops for storage of data.

The user should note that, because the clocks are not gated with the Direction and Output Enable pins, data at the A and B pins may be clocked into the storage flip-flops at any time.

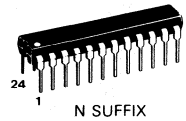
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 15 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

OCTAL 3-STATE BUS TRANSCEIVERS AND D-TYPE FLIP-FLOPS



J SUFFIX
CERAMIC PACKAGE
CASE 758



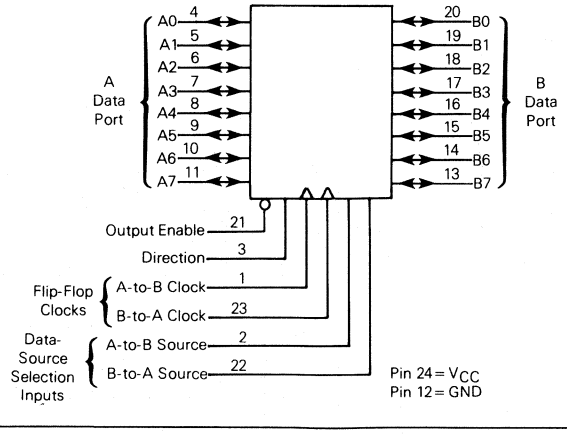
N SUFFIX
PLASTIC PACKAGE
CASE 724

ORDERING INFORMATION

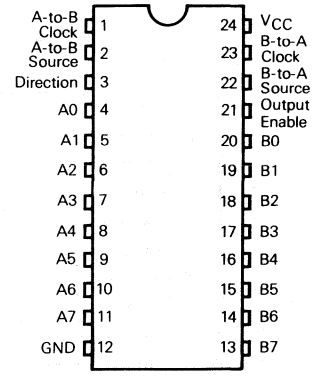
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



HC646 — Noninverting Outputs
HC648 — Inverting Outputs

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.001 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=6.0 mA I_{out}=7.8 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output Enable=V_{IH} V_{out}=V_{CC} or GND	6.0	—	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

5

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 6)	C_L = 50 pF	70	30	MHz
t_{PLH}	Maximum Propagation Delay, Input A to Output B	C_L = 50 pF	15	30	ns
t_{PHL}	(also Input B to Output A) (Figures 1 and 6)		15	30	
t_{PLH}	Maximum Propagation Delay, A-to-B Clock to Output B	C_L = 50 pF	20	40	ns
t_{PHL}	(also B-to-A Clock to Output A) (Figures 2 and 6)		20	40	
t_{PLH}	Maximum Propagation Delay, A-to-B Source to Output B	C_L = 50 pF	15	30	ns
t_{PHL}	(also B-to-A Source to Output A)* (Figures 3 and 6)		15	30	
t_{PHZ}	Maximum Propagation Delay, Direction to Outputs A or B	C_L = 5 pF	15	30	ns
t_{PLZ}	(Figures 4 and 7)		15	30	
t_{PZH}		C_L = 50 pF	16	33	ns
t_{PZL}			16	33	
t_{PHZ}	Maximum Propagation Delay, Output Enable to Outputs A or B	C_L = 5 pF	15	30	ns
t_{PLZ}	(Figures 5 and 7)		15	30	
t_{PZH}		C_L = 50 pF	16	33	ns
t_{PZL}			16	33	
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time (Figures 1 and 6)	C_L = 50 pF	5	10	ns

*These parameters are measured with the state of the storage flip-flop opposite to that of the input.

SWITCHING CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 6)	C_L = 50 pF	2.0	11	5	4	4	MHz
			4.5	54	27	21	18	
			6.0	64	32	25	21	
t_{PLH}	Maximum Propagation Delay, Input A to Output B (also Input B to Output A) (Figures 1 and 6)	C_L = 50 pF	2.0	85	170	214	253	ns
		C_L = 150 pF		110	220	277	328	
		C_L = 50 pF	4.5	17	34	43	51	
		C_L = 150 pF		22	44	55	66	
		C_L = 50 pF	6.0	14	29	36	43	
		C_L = 150 pF		19	37	47	56	
t_{PHL}		C_L = 50 pF	2.0	85	170	214	253	ns
		C_L = 150 pF		110	220	277	328	
		C_L = 50 pF	4.5	17	34	43	51	
		C_L = 150 pF		22	44	55	66	
		C_L = 50 pF	6.0	14	29	36	43	
		C_L = 150 pF		19	37	47	56	
t_{PLH}	Maximum Propagation Delay, A-to-B Clock to Output B (also B-to-A Clock to Output A) (Figures 2 and 6)	C_L = 50 pF	2.0	110	220	277	328	ns
		C_L = 150 pF		135	270	340	402	
		C_L = 50 pF	4.5	22	44	55	66	
		C_L = 150 pF		27	54	68	80	
		C_L = 50 pF	6.0	19	37	47	56	
		C_L = 150 pF		23	46	58	68	
t_{PHL}		C_L = 50 pF	2.0	110	220	277	328	ns
		C_L = 150 pF		135	270	340	402	
		C_L = 50 pF	4.5	22	44	55	66	
		C_L = 150 pF		27	54	68	80	
		C_L = 50 pF	6.0	19	37	47	56	
		C_L = 150 pF		23	46	58	68	

5

SWITCHING CHARACTERISTICS (Input $t_r = t_f = 6$ ns) (Continued)

Symbol	Parameter		V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{PLH}	Maximum Propagation Delay, A-to-B Source to Output B (also B-to-A Source to Output A)† (Figures 3 and 6)	$C_L = 50$ pF	2.0	85	170	214	253	ns
		$C_L = 150$ pF		110	220	277	328	
		$C_L = 50$ pF	4.5	17	34	43	51	
		$C_L = 150$ pF		22	44	55	66	
		$C_L = 50$ pF	6.0	14	29	36	43	
		$C_L = 150$ pF		19	37	47	56	
t_{PHL}		$C_L = 50$ pF	2.0	85	170	214	253	ns
		$C_L = 150$pF		110	220	277	328	
		$C_L = 50$ pF	4.5	17	34	43	51	
		$C_L = 150$ pF		22	44	55	66	
		$C_L = 50$ pF	6.0	14	29	36	43	
		$C_L = 150$ pF		19	37	47	56	
t_{PLZ}	Maximum Propagation Delay, Direction to Outputs A or B (Figures 4 and 7)	$C_L = 50$ pF	2.0	88	175	221	261	ns
			4.5	18	35	44	52	
			6.0	15	30	37	44	
t_{PHZ}			2.0	88	175	221	261	ns
			4.5	18	35	44	52	
			6.0	15	30	37	44	
t_{PZL}	Maximum Propagation Delay, Direction to Outputs A or B (Figures 4 and 7)	$C_L = 50$ pF	2.0	88	175	221	261	ns
		$C_L = 150$ pF		113	225	284	335	
		$C_L = 50$ pF	4.5	18	35	44	52	
		$C_L = 150$ pF		23	45	57	67	
		$C_L = 50$ pF	6.0	15	30	37	44	
		$C_L = 150$ pF		19	38	48	57	
t_{PZH}		$C_L = 50$ pF	2.0	88	175	221	261	ns
		$C_L = 150$ pF		113	225	284	335	
		$C_L = 50$ pF	4.5	18	35	44	52	
		$C_L = 150$ pF		23	45	57	67	
		$C_L = 50$ pF	6.0	15	30	37	44	
		$C_L = 150$ pF		19	38	48	57	
t_{PLZ}	Maximum Propagation Delay, Output Enable to Outputs A or B (Figures 5 and 7)	$C_L = 50$ pF	2.0	88	175	221	261	ns
			4.5	18	35	44	52	
			6.0	15	30	37	44	
t_{PHZ}			2.0	88	175	221	261	ns
			4.5	18	35	44	52	
			6.0	15	30	37	44	
t_{PZL}	Maximum Propagation Delay, Output Enable to Outputs A or B (Figures 5 and 7)	$C_L = 50$ pF	2.0	88	175	221	261	ns
		$C_L = 150$ pF		113	225	284	335	
		$C_L = 50$ pF	4.5	18	35	44	52	
		$C_L = 150$ pF		23	45	57	67	
		$C_L = 50$ pF	6.0	15	30	37	44	
		$C_L = 150$ pF		19	38	48	57	
t_{PZH}		$C_L = 50$ pF	2.0	88	175	221	261	ns
		$C_L = 150$ pF		113	225	284	335	
		$C_L = 50$ pF	4.5	18	35	44	52	
		$C_L = 150$ pF		23	45	57	67	
		$C_L = 50$ pF	6.0	15	30	37	44	
		$C_L = 150$ pF		19	38	48	57	
t_{TLH}, t_{THL}	Maximum Output Transition Time (Figures 1 and 6)	$C_L = 50$ pF	2.0	30	60	75	90	ns
			4.5	6	12	15	18	
			6.0	5	10	13	15	
C_{out}	Three-State Output Capacitance (Output Enable = V_{CC})		–	7.5	15	15	15	pF
C_{in}	Input Capacitance		–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		–	60	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

†These parameters are measured with the state of the storage flip-flop opposite to that of the input.

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
			Typical	Guaranteed Limit		
t_r, t_f	Maximum Input Rise and Fall time (Figure 1)	–	1000	500	500	500	ns
t_{su}	Minimum Setup Time, Input A to A-to-B Clock (or Input B to B-to-A Clock) (Figure 2)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, A-to-B Clock to Input A (or B-to-A Clock to Input B) (Figure 2)	2.0	−20	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−3	0	0	0	
t_w	Minimum Pulse Width, A-to-B Clock (or B-to-A Clock) (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	

PIN DESCRIPTIONS

INPUTS/OUTPUTS

A0-A7 (PINS 4-11) and B0-B7 (PINS 20-13) – A and B data ports. These pins may function either as inputs to or outputs from the transceivers.

CONTROL INPUTS

OUTPUT ENABLE (PIN 21) – Active-low output enable. When this pin is low, the outputs are enabled and function normally. When this pin is high, the A and B data ports are in high-impedance states. See the Function Table.

DIRECTION (PIN 3) – Data direction control. When the Output Enable pin is low, this control pin determines the direction of data flow. When Direction is high, the A data ports are inputs and the B data ports are outputs. When Direction is low, the A data ports are outputs and the B data ports are inputs.

A-TO-B CLOCK, B-TO-A CLOCK (PINS 1, 23) – Clocks for the internal D-type flip-flops. With a low-to-high voltage transition on the appropriate Clock pin, data on the A (or B) inputs are clocked into the internal A (or B) flip-flops. These clocks are not internally gated with the Output Enable or the Direction pins, therefore data at the A and B pins may be clocked into the storage flip-flops at any time.

A-TO-B SOURCE, B-TO-A SOURCE (PINS 2, 22) – Data-source selection pins. Depending upon the states of these pins (see the Function Table), data at the outputs may come either from the inputs or from the D-type flip-flops.

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FUNCTION TABLE – HC646
(The Function Table for the HC648 is the same as this, but with the outputs inverted)

Control Inputs						Data Port Status		Storage Flip-Flop States		Description of Operation
Output Enable	Direction	A-to-B Clock	B-to-A Clock	A-to-B Source	B-to-A Source	A	B	Q_A	Q_B	
H	X	H, L, ⌝⌞	H, L, ⌝⌞	X	X	Input: X	Input: X	no change	no change	The output functions of the A and B ports are disabled.
		⌐⌙	⌐⌙	X	X	L H X X	X X L H	L H X X	X X L H	The ports may be used as inputs to the storage flip-flops. Data at the inputs are clocked into the flip-flops with the rising edge of the Clocks.
L	H	H, L, ⌝⌞	X*	L	X	Input: L H	Output: L H	no change no change	no change no change	The outputs of the B data ports are enabled and behave according to the following logic equation: $B = [A \bullet (\overline{\text{A-to-B Source}})] + [Q_A \bullet \text{A-to-B Source})]$ 1.) When A-to-B Source is low; the data at the A data ports are displayed at the B data ports. The states of the storage flip-flops are not affected.
				H	X	X	Q_A	no change	no change	2.) When A-to-B Source is high, the states of the A storage flip-flops are displayed at the B data ports.
		⌐⌙	X*	L	X	L H	L H	L H	no change no change	3.) When A-to-B Source is low, the data at the A data ports are clocked into the A storage flip-flops by a rising-edge signal on the A-to-B Clock.
				H	X	L H	Q_A Q_A	L H	no change no change	4.) When A-to-B Source is high, the data at the A data ports are clocked into the A storage flip-flops by a rising-edge signal on the A-to-B Clock. The states, Q_A, of the storage flip-flops propagate directly to the B data ports.
L	L	X*	H, L, ⌝⌞	X	L	Output: L H	Input: L H	no change no change	no change no change	The outputs of the A data ports are enabled and behave according to the following logic equation: $A = [B \bullet (\overline{\text{B-to-A Source}})] + [Q_B \bullet (\text{B-to-A Source})]$ 1.) When B-to-A Source is low, the data at the B data ports are displayed at the A data ports. The states of the storage flip-flops are not affected.
				X	H	Q_B	X	no change	no change	2.) When B-to-A Source is high, the states of the B storage flip-flops are displayed at the A data ports.
		X*	⌐⌙	X	L	L H	L H	no change no change	L H	3.) When B-to-A Source is low, the data at the B data ports are clocked into the B storage flip-flops by a rising-edge signal on the B-to-A Clock.
				X	H	Q_B Q_B	L H	no change no change	L H	4.) When B-to-A Source is high, the data at the B data ports are clocked into the B storage flip-flops by a rising-edge signal on the B-to-A Clock. The states, Q_B, of the storage flip-flops propagate directly to the A data ports.

*The clocks are not internally gated with the Output Enable and Direction pins, therefore data at the A and B pins may be clocked into the storage flip-flops at any time.

TIMING DIAGRAMS AND SWITCHING DIAGRAMS — HC646
(The diagrams for the HC648 are the same as this, but with the outputs inverted)

FIGURE 1

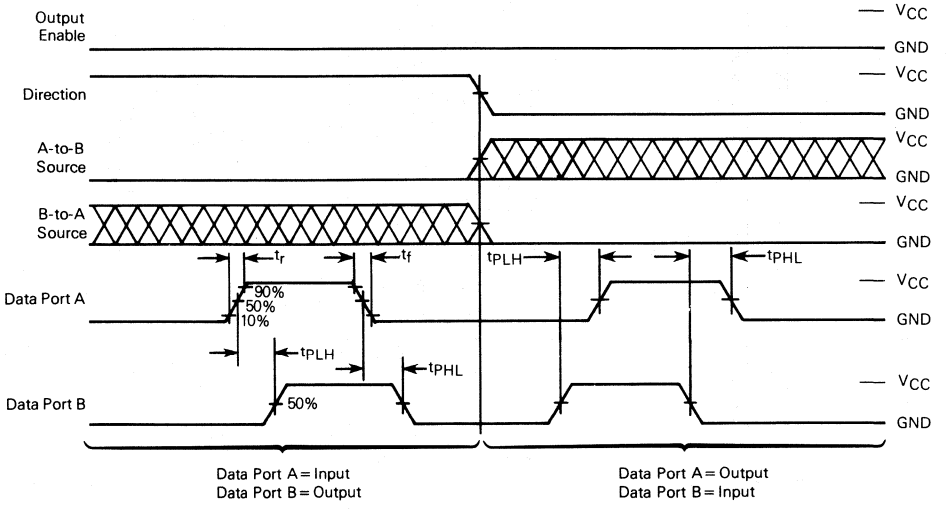

FIGURE 2

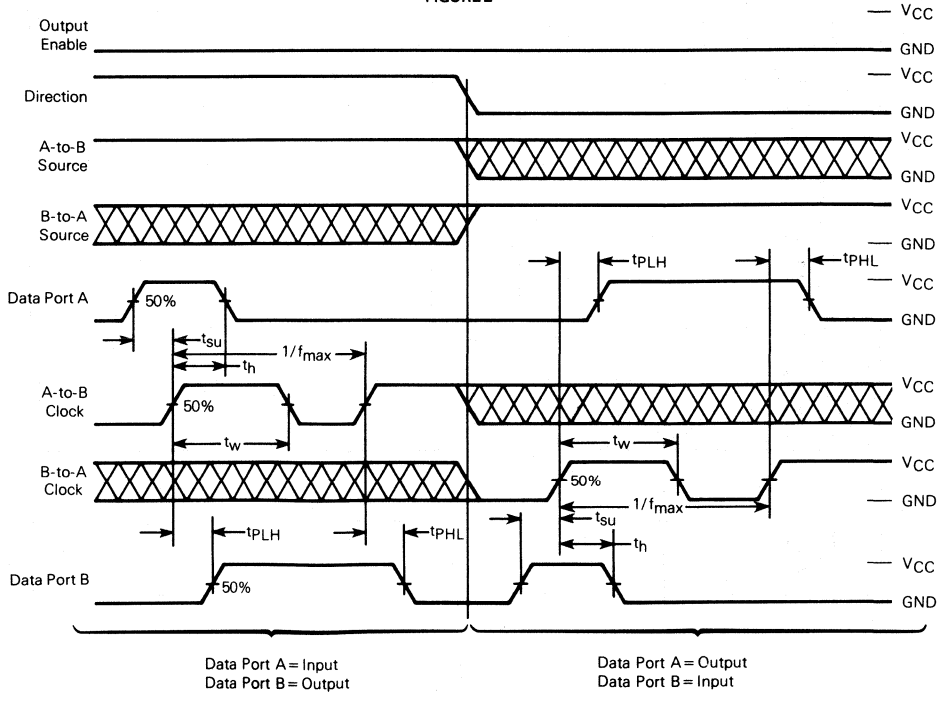

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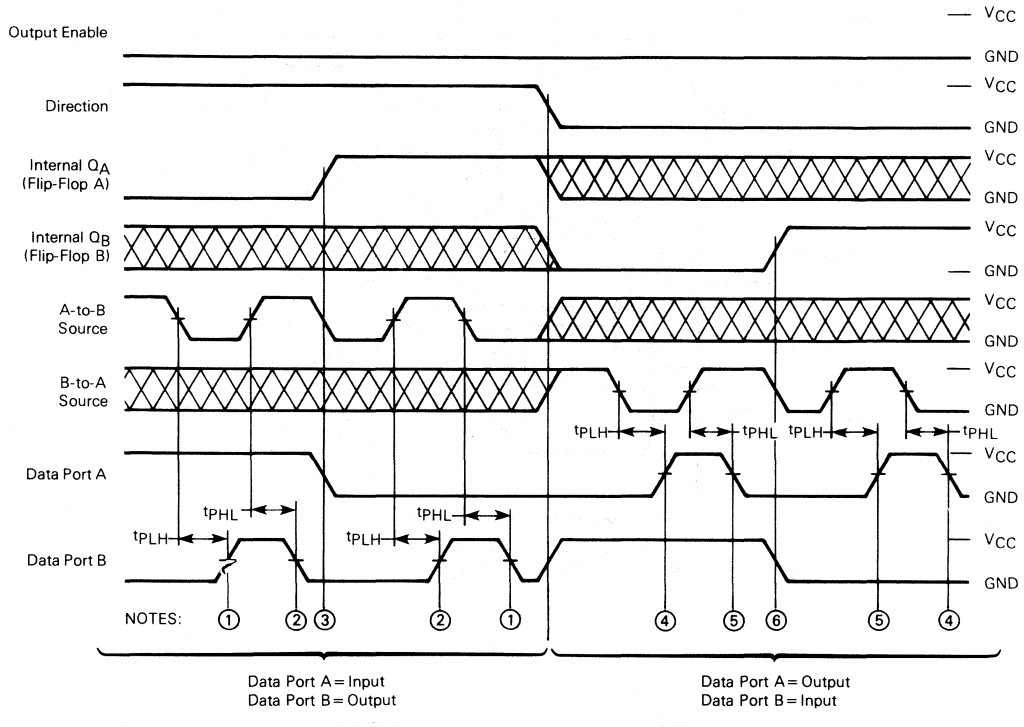
FIGURE 3



NOTES:

1. Output B changes from the level of the storage flip-flop, Q_A, to the level of Input A.
2. Output B changes from the level of input A to the level of the storage flip-flop, Q_A.
3. The A storage flip-flop, A-to-B Source, and Input A have simultaneously changed state for the purpose of this example. Output B is now displaying the voltage level of Input A.
4. Output A changes from the level of the storage flip-flop, Q_B, to the level of Input B.
5. Output A changes from the level of Input B to the level of the storage flip-flop, Q_B.
6. The B storage flip-flop, B-to-A Source, and Input B have simultaneously changed state for the purpose of this example. Output A is now displaying the voltage level of Input B.

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FIGURE 4

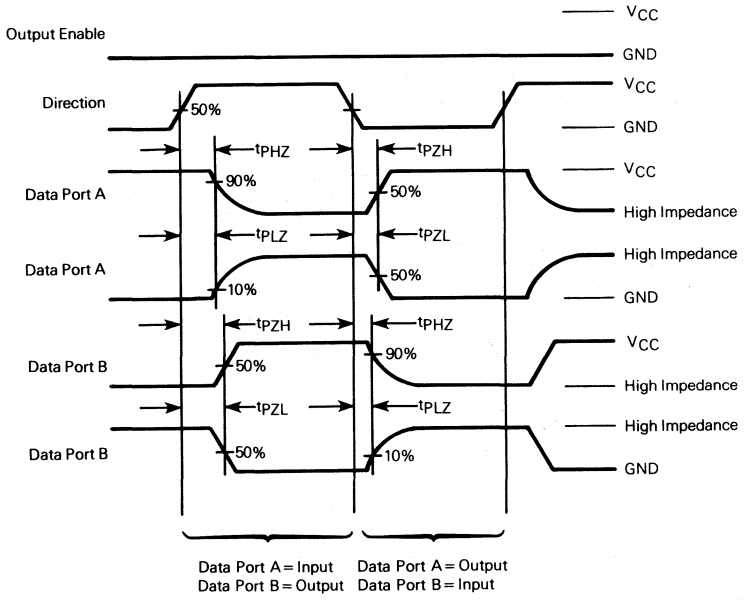


FIGURE 5

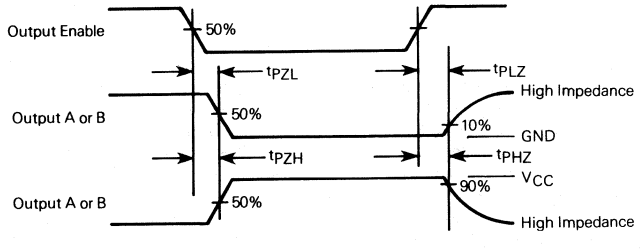


FIGURE 6

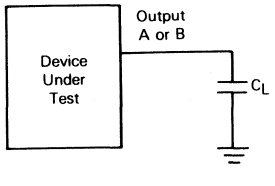
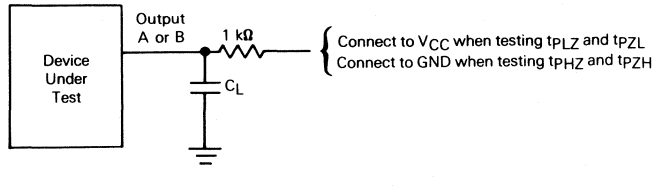
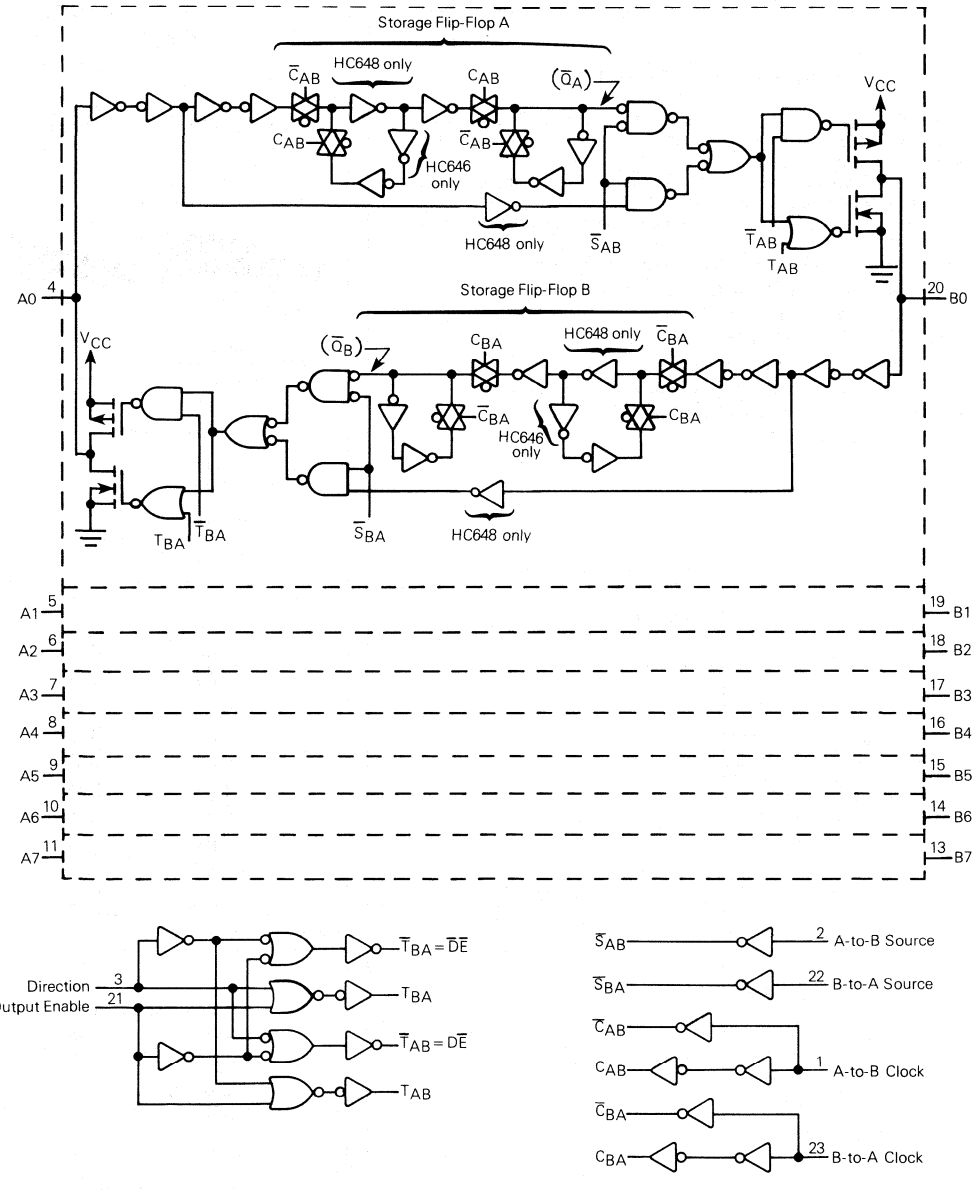


FIGURE 7



LOGIC DIAGRAM
HC646 and HC648



MOTOROLA

MC54/74HC688

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

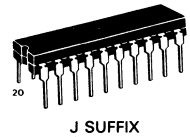
8-BIT EQUALITY COMPARATOR

8-BIT EQUALITY COMPARATOR

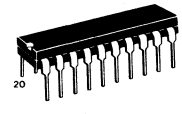
The MC54/74HC688 is identical in pinout to the LS688. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC688 compares two 8-bit binary or BCD words and indicates whether or not they are equal. By using the Cascade Input, two or more of the devices may be cascaded to compare words of more than 8 bits.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 732



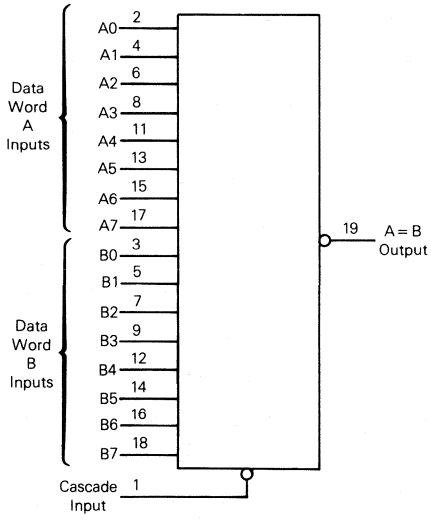
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

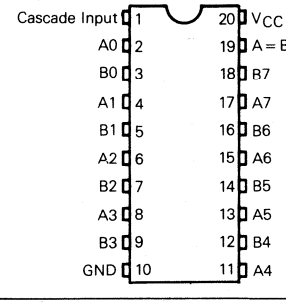
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
Data Words	Cascade	A = B
A = B	L	L
A > B	L	H
A < B	L	H
X	H	H

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 2)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output A = B	28	38	ns
t_{PHL}	(Figures 1 and 3)	28	38	
t_{PLH}	Maximum Propagation Delay, Cascade Input to Output A = B	14	22	ns
t_{PHL}	(Figures 2 and 3)	14	22	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 3)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Output A = B (Figures 1 and 3)	2.0	113	210	265	313	ns
		4.5	30	42	53	63	
		6.0	24	36	45	53	
t_{PHL}		2.0	113	210	265	313	ns
		4.5	30	42	53	63	
		6.0	24	36	45	53	
t_{PLH}	Maximum Propagation Delay, Cascade Input to Output A = B (Figures 2 and 3)	2.0	66	120	151	179	ns
		4.5	16	24	30	36	
		6.0	14	20	26	30	
t_{PHL}		2.0	66	120	151	179	ns
		4.5	16	24	30	36	
		6.0	14	20	26	30	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 3)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		45	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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SWITCHING WAVEFORMS

FIGURE 1

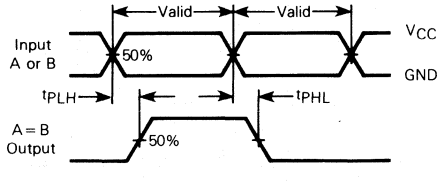


FIGURE 2

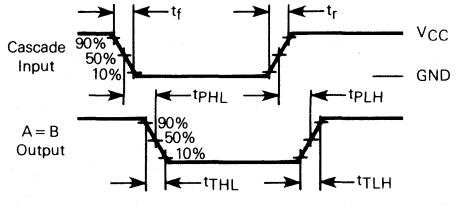
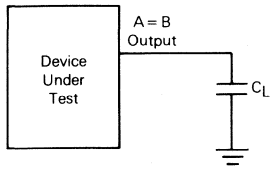
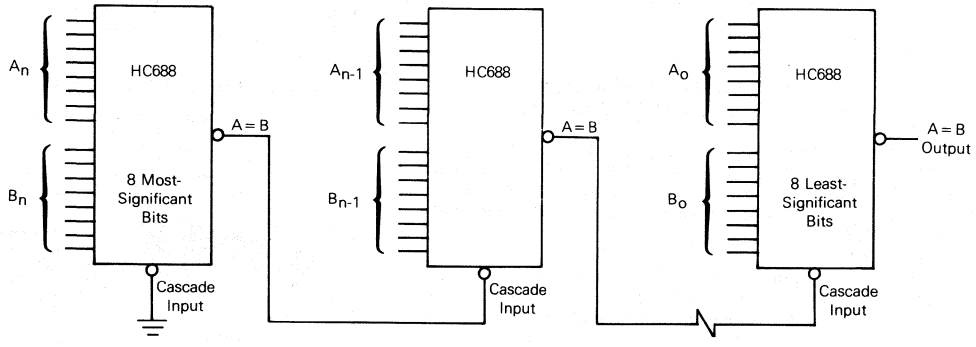


FIGURE 3 — TEST CIRCUIT

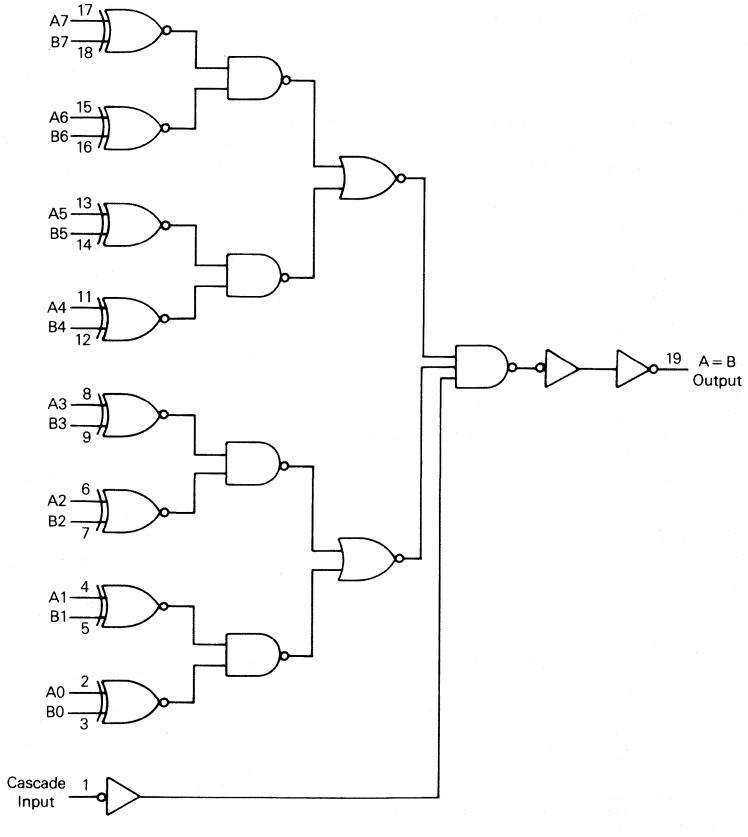


TYPICAL APPLICATION

Two or more HC688 8-bit Equality Comparators may be cascaded to compare binary or BCD numbers having more than 8 bits. One method of accomplishing this is shown here.



LOGIC DIAGRAM



5

MOTOROLA

MC54/74HCT688

Product Preview

8-BIT EQUALITY COMPARATOR (WITH LSTTL-COMPATIBLE INPUTS)

The MC54/74HCT688 may be used as a level converter for interfacing LSTTL to High-Speed CMOS. The inputs of HCT devices are compatible with both LSTTL and CMOS output voltage levels. Therefore, no pullup resistors are required at the inputs of the HCT688 when interfacing with LSTTL.

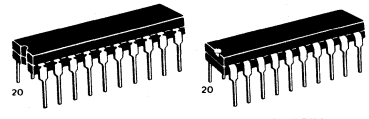
The HCT688 is identical in pinout to the LS688.

The HCT688 compares two 8-bit binary or BCD words and indicates whether or not they are equal. By using the Cascade Input, two or more of the devices may be cascaded to compare words of more than 8 bits.

- Compatible with LSTTL Outputs — No Pullup Resistor Required
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Voltage Range: 4.5 to 5.5 Volts
- Low Quiescent Current Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

8-BIT EQUALITY COMPARATOR (WITH LSTTL-COMPATIBLE INPUTS)



J SUFFIX
CERAMIC PACKAGE
CASE 732

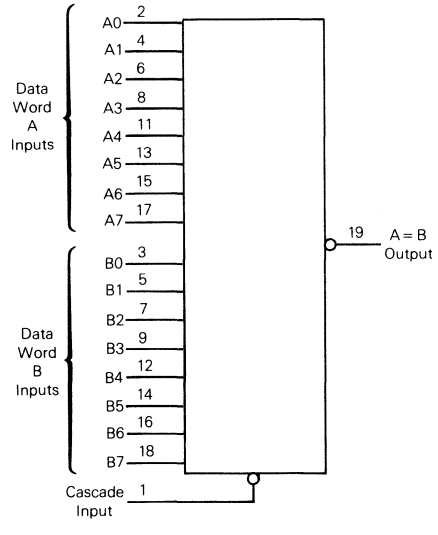
N SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCTXXJ (Ceramic Package Only)

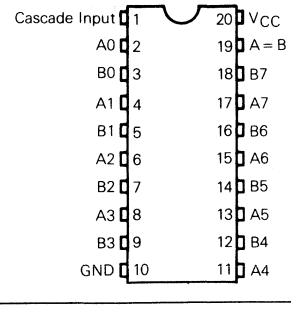
74 Series: −40°C to +85°C
MC74HCTXXN (Plastic Package)
MC74HCTXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
Data Words	Cascade	A = B
A = B	L	L
A > B	L	H
A < B	L	H
X	H	H

5

MOTOROLA

MC54/74HC4002

Advance Information

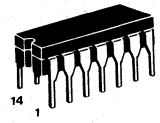
DUAL 4-INPUT NOR GATE

The MC54/74HC4002 is identical in pinout to the MC14002. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

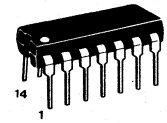
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL 4-INPUT NOR GATE



J SUFFIX
CERAMIC PACKAGE
CASE 632



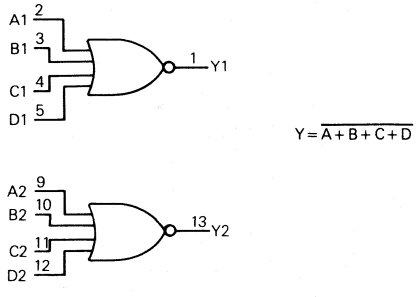
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: $-55°C$ to $+125°C$
MC54HCXXXXJ (Ceramic Package Only)

74 Series: $-40°C$ to $+85°C$
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

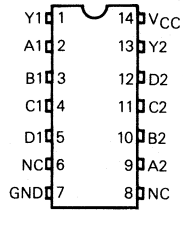
LOGIC DIAGRAM



$Y = \overline{A + B + C + D}$

V_{CC} = Pin 14
GND = Pin 7
No Connection = Pins 6, 8

PIN ASSIGNMENT



NC = No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

5

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

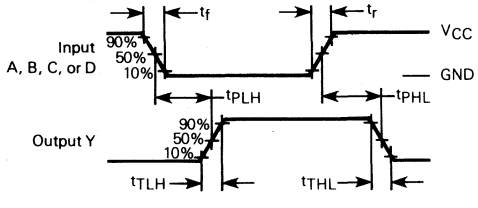
Symbol	Parameter	54HC and 74HC		Unit
		Typical	Guaranteed Limit	
t_{PLH}	Maximum Propagation Delay, Input A, B, C, or D to Output Y	10	20	ns
t_{PHL}	(Figures 1 and 2)	11	20	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

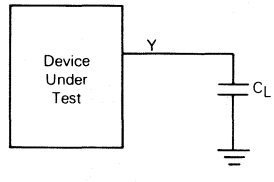
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
			Typical	Guaranteed Limit		
t_{PLH}	Maximum Propagation Delay, Input A, B, C, or D to Output Y (Figures 1 and 2)	2.0	60	120	151	179	ns
		4.5	12	24	30	36	
		6.0	10	20	26	30	
t_{PHL}		2.0	60	120	151	179	ns
		4.5	12	24	30	36	
		6.0	10	20	26	30	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–	26	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption per gate:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS





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MOTOROLA

MC54/74HC4015

Product Preview

DUAL 4-BIT SERIAL-INPUT/PARALLEL-OUTPUT SHIFT REGISTER

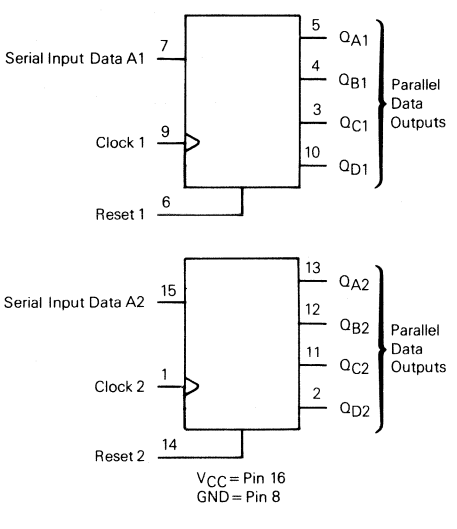
The MC54/74HC4015 is identical in pinout to the MC14015 metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC4015 consists of two independent 4-bit serial-input/parallel-output shift registers. Each register has independent Clock and Reset inputs with a single serial Data input. The registers are D-Type master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be reset when a high level is applied on the Reset line. These shift registers find use in buffer storage and serial-to-parallel conversion, where low power dissipation and/or noise immunity is desired.

PRODUCT CANCELED

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

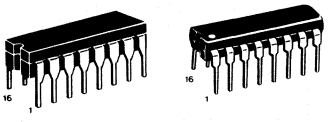
BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL 4-BIT SERIAL-INPUT/ PARALLEL-OUTPUT SHIFT REGISTER



J SUFFIX
CERAMIC PACKAGE
CASE 620

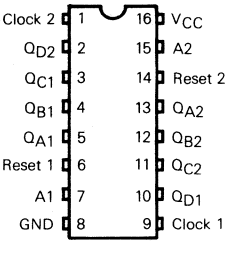
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs			
Reset	Data	Clock	Q_A	Q_B	Q_C	Q_D
H	X	X	L	L	L	L
L	L	↗	L	Q_{An}	Q_{Bn}	Q_{Cn}
L	H	↗	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↘	no change			

Q_{An}, Q_{Bn}, Q_{Cn} = the levels of Q_A, Q_B and Q_C before the clock transition.

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

MC54/74HC4016

Product Preview

QUAD ANALOG SWITCH/MULTIPLEXER/DEMULTIPLEXER

The MC54/74HC4016 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistance, and low OFF-channel leakage current. This analog switch/multiplexer/demultiplexer controls analog voltages that may vary across the full power-supply range (from V_{CC} to GND).

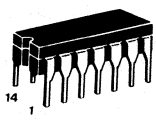
The HC4016 is identical in pinout to the metal-gate CMOS MC14016 and MC14066. Each device has four independent switches that may control either analog or digital signals. The device has been designed so that the ON resistances, R_{ON}, are much more linear than those of metal-gate CMOS analog switches.

This device is identical in both function and pinout to the HC4066. For analog switches with voltage-level translators, see the HC4316.

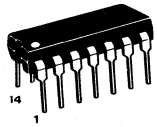
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power-Supply Voltage Range (V_{CC} – GND) = 3.0 to 12.0 Volts
- Digital (On/Off Control) Power-Supply Voltage Range (V_{CC} – GND) = 3.0 to 12.0 Volts
- Improved Linearity of ON Resistance
- Low Noise

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD ANALOG SWITCH/ MULTIPLEXER/DEMULTIPLEXER



J SUFFIX
CERAMIC PACKAGE
CASE 632



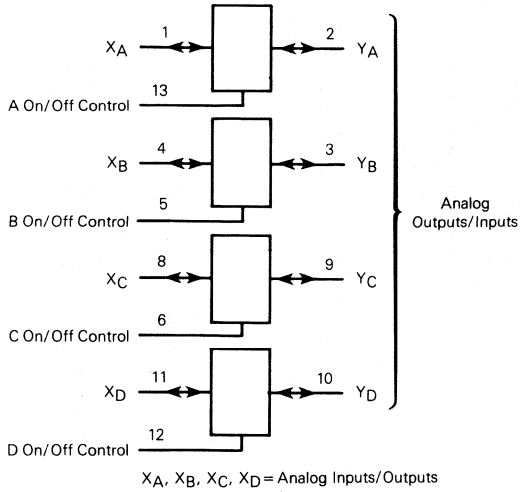
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: –55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

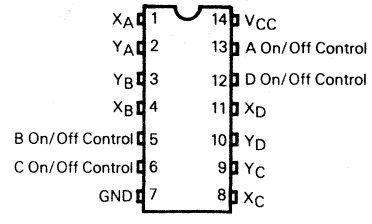
74 Series: –40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

BLOCK DIAGRAM



X_A, X_B, X_C, X_D = Analog Inputs/Outputs
V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	off
H	on

5

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

MC54/74HC4017

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

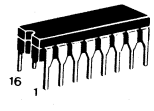
DECADE COUNTER/DIVIDER

DECADE COUNTER/DIVIDER

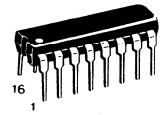
The MC54/74HC4017 is identical in pinout to the standard CMOS MC14017. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC4017 uses a five stage Johnson counter and decoding logic to provide high-speed operation. This device also has an active-high, as well as active-low clock input.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620



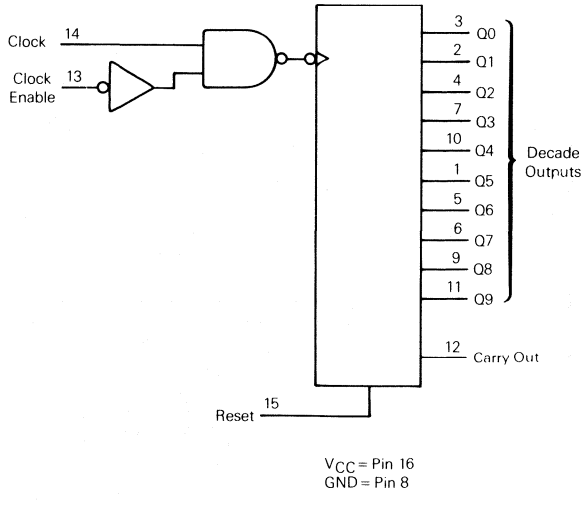
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

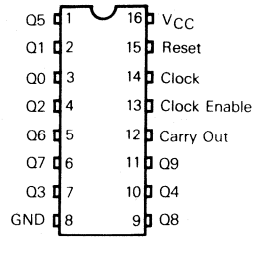
74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 9)		30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q (Figures 1 and 9)	18	40	ns
t_{PHL}		18	40	
t_{PLH}	Maximum Propagation Delay, Clock to Carry Out (Figures 2 and 9)	16	40	ns
t_{PHL}		16	40	
t_{PLH}	Maximum Propagation Delay, Reset to Carry Out (Figures 3 and 9)	15	40	ns
t_{PHL}		19	40	
t_{PLH}	Maximum Propagation Delay, Reset to Carry Out (Figures 3 and 9)	18	40	ns
t_{PLH}	Maximum Propagation Delay, Clock Enable to Q (Figures 4 and 9)	22	44	ns
t_{PHL}		22	44	
t_{PLH}	Maximum Propagation Delay, Clock Enable to Carry Out (Figures 5 and 9)	20	44	ns
t_{PHL}		20	44	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 8 and 9)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 9)	2.0	8	4	3	3	MHz
		4.5	40	20	16	13	
		6.0	47	24	19	16	
t_{PLH}	Maximum Propagation Delay, Clock to Q (Figures 1 and 9)	2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{PHL}		2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{PLH}	Maximum Propagation Delay, Clock to Carry Out (Figures 2 and 9)	2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{PHL}		2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{PLH}	Maximum Propagation Delay, Reset to Q (Figures 3 and 9)	2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{PHL}		2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{PLH}	Maximum Propagation Delay, Reset to Carry Out (Figures 3 and 9)	2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{PLH}	Maximum Propagation Delay, Clock Enable to Q (Figures 4 and 9)	2.0	125	250	315	373	ns
		4.5	25	50	63	75	
		6.0	21	43	54	63	
t_{PHL}		2.0	125	250	315	373	ns
		4.5	25	50	63	75	
		6.0	21	43	54	63	
t_{PLH}	Maximum Propagation Delay, Clock Enable to Carry Out (Figures 5 and 9)	2.0	125	250	315	373	ns
		4.5	25	50	63	75	
		6.0	21	43	54	63	
t_{PHL}		2.0	125	250	315	373	ns
		4.5	25	50	63	75	
		6.0	21	43	54	63	
t_{TLH}, t_{THL}	Output Transition Time, Any Output (Figures 8 and 9)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		110				pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

5

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
			Typical	Guaranteed Limit		
t_r, t_f	Maximum Input Rise and Fall Time (Figure 1)	–	1000	500	500	500	ns
t_{su}	Minimum Setup Time, Clock Enable to Clock (Figure 6)	2.0	25	50	63	75	ns
		4.5	5	10	13	15	
		6.0	4	9	11	13	
t_h	Minimum Hold Time, Clock to Clock Enable (Figure 6)	2.0	25	50	63	75	ns
		4.5	5	10	13	15	
		6.0	4	9	11	13	
t_w	Minimum Pulse Width, Clock Input (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Reset Input (Figure 3)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Clock Enable Input (Figure 6)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_{rec}	Minimum Reset Recovery Time, Reset to Clock (Figure 7)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_{su}	Minimum Setup Time, Clock Enable to Clock (Inhibit Count) (Figure 6)	2.0	25	50	63	75	ns
		4.5	5	10	13	15	
		6.0	4	9	11	13	

FUNCTION TABLE

Clock	Clock Enable	Reset	Output State*
L	X	L	no change
X	H	L	no change
X	X	H	reset counter, Q0 = H, Q1-Q9 = L
↗	L	L	advance to next state
↘	X	L	no change
X	↗	L	no change
H	↘	L	advance to next state

X = Don't Care

* Carry Out = H for Q0, Q1, Q2, Q3, or Q4 = H; Carry Out = L otherwise.

PIN DESCRIPTIONS

INPUTS

CLOCK (PIN 14) – Counter clock input. A low-to-high transition on this input advances the counter to its next state.

CONTROL INPUTS

RESET (PIN 15) – Asynchronous counter reset input. A high level at this input initializes the counter and forces Q0 and Carry Out to a logic high; Q1-Q9 are forced to a logic low level.

CLOCK ENABLE (PIN 13) – Active-low clock enable input. A low level on this input allows the device to count. A high level on this input inhibits the counting operation. This input may also be used as a negative-edge clock input, using Clock (Pin 14) as an active-high enable pin.

OUTPUTS

Q0-Q9 (PINS 3, 2, 4, 7, 10, 1, 5, 6, 9, 11) – Decoded decade counter outputs. Each of these outputs is high for one clock period only.

CARRY OUT (PIN 12) – Cascading output pin. This output is used either as a cascading output or a symmetrical divide-by-ten output. This output goes low when a count of five is reached and high when the counter advances to zero or when reset. When the counters are cascaded, this output provides a rising-edge signal for the clock input of the next counter stage.

SWITCHING WAVEFORMS

FIGURE 1

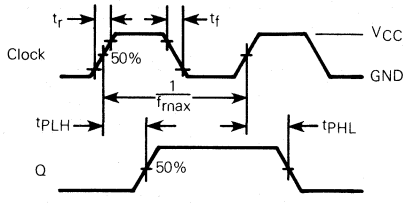


FIGURE 2

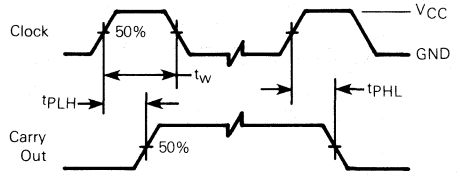


FIGURE 3

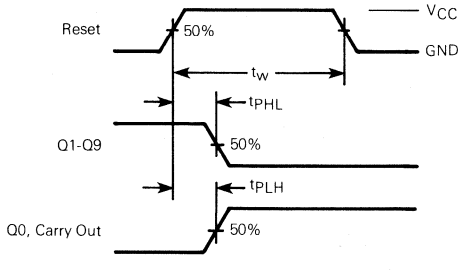


FIGURE 4

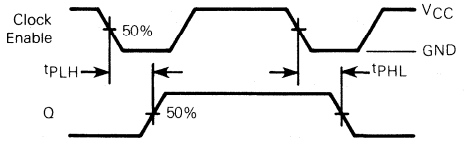


FIGURE 5

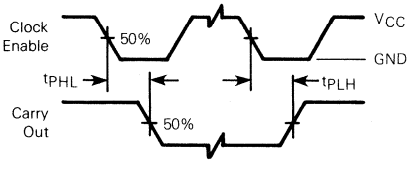


FIGURE 6

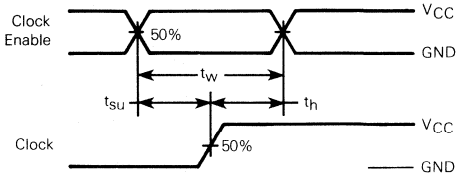


FIGURE 7

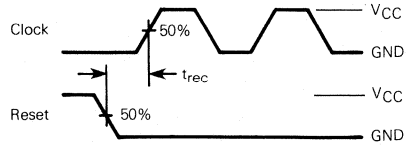


FIGURE 8

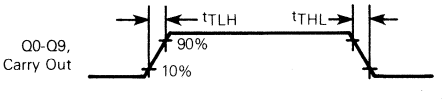
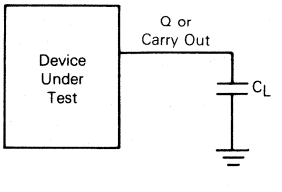


FIGURE 9 — TEST CIRCUIT



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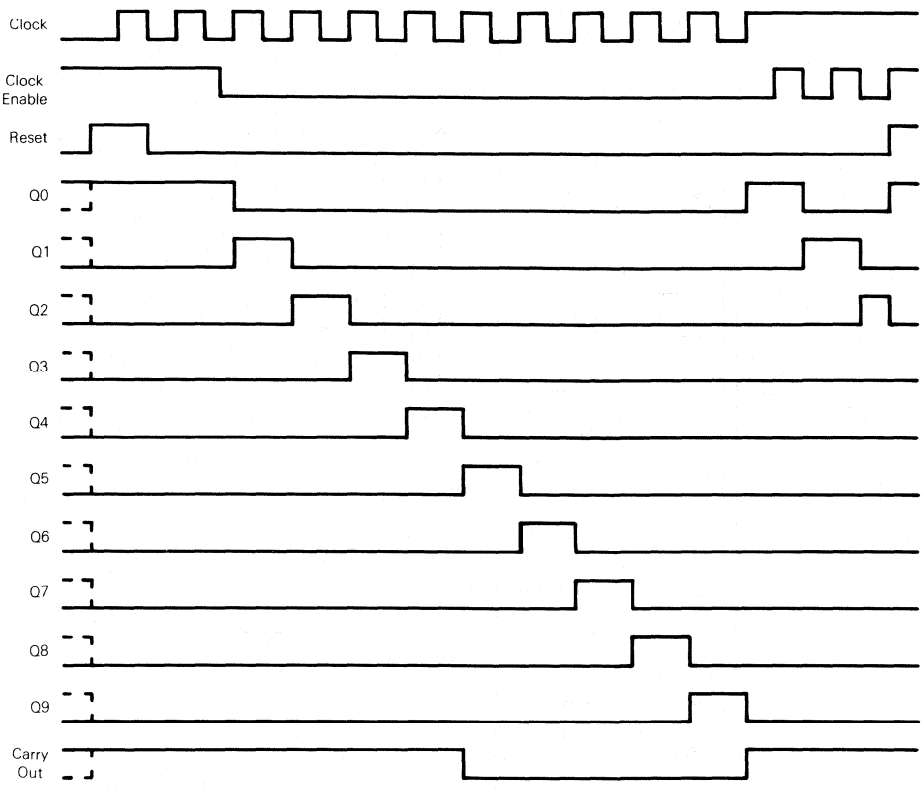
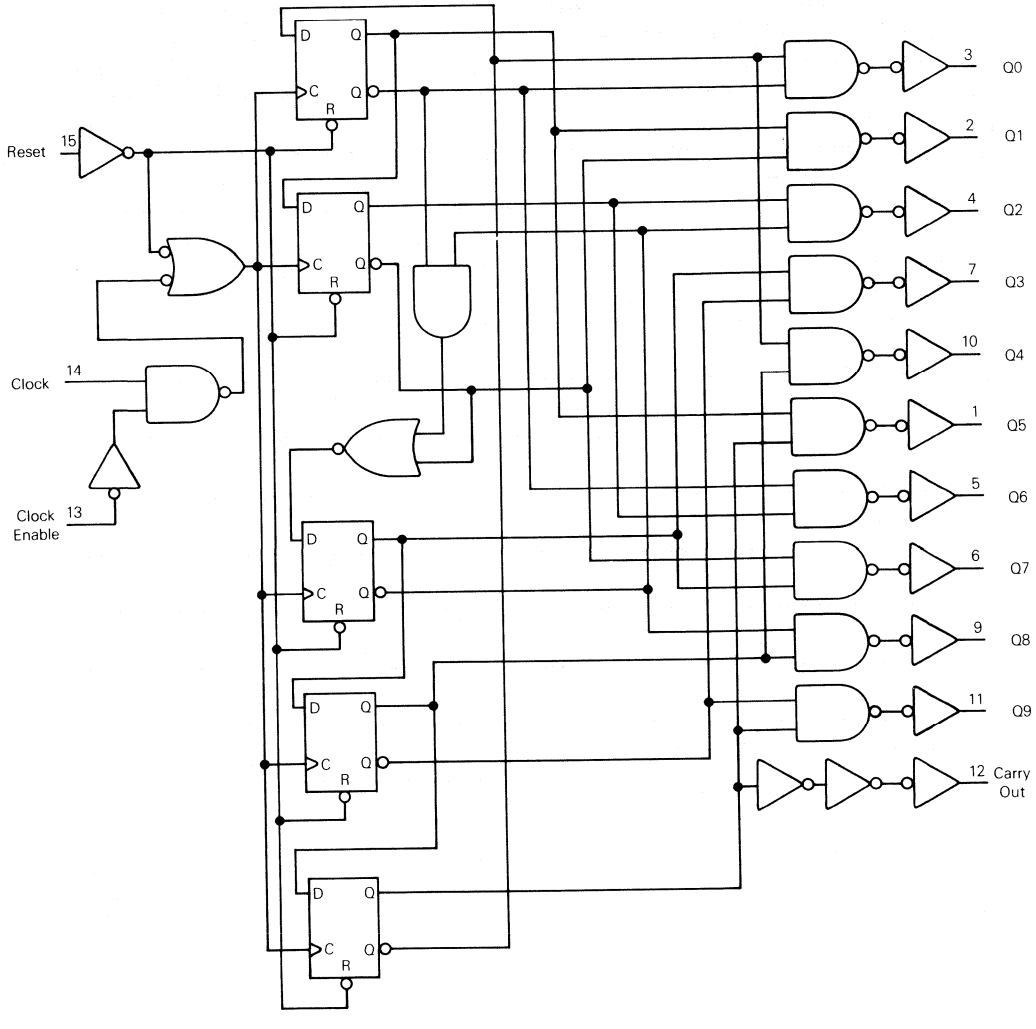
TIMING DIAGRAM



LOGIC DIAGRAM



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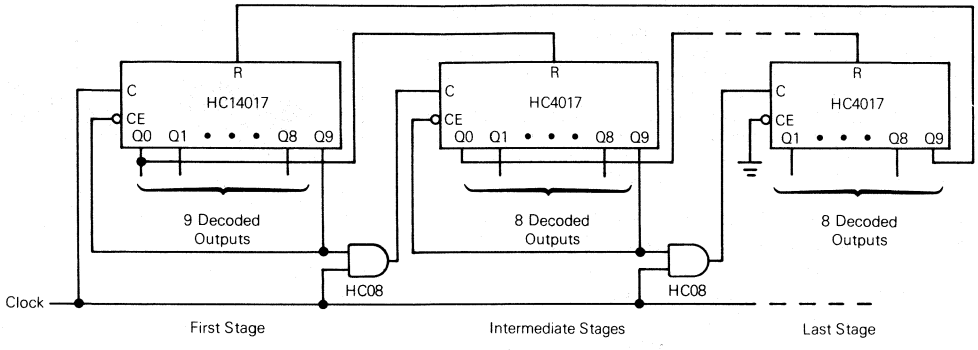
APPLICATIONS INFORMATION

Figure 10 shows a technique for cascading the counters to extend the number of decoded output states. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 10 — COUNTER EXPANSION



MOTOROLA

MC54/74HC4020

Advance Information

14-STAGE BINARY RIPPLE COUNTER

The MC54/74HC4020 is identical in pinout to the standard CMOS MC14020. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

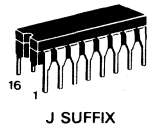
This device consists of 14 master-slave flip-flops with 12 stages brought out to pins. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC4020.

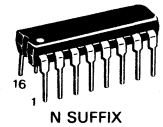
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

14-STAGE
BINARY RIPPLE COUNTER



J SUFFIX
CERAMIC PACKAGE
CASE 620



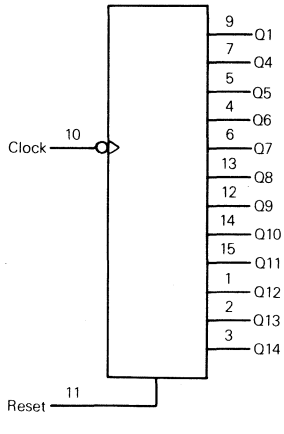
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

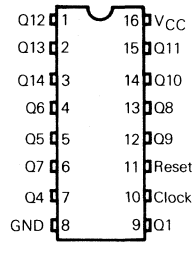
74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



FUNCTION TABLE

Clock	Reset	Output State
⌐‾	L	No Change
‾⌐	L	Advance to next state
X	H	All Outputs are low

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

5

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	40	30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q1*	17	35	ns
t_{PHL}	(Figures 1 and 3)	17	35	
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 3)	16	40	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	5	10	ns

* For V_{CC} = 5 V, T_A = 25°C and C_L = 15 pF maximum propagation delay from Clock to any output can be calculated with the following equation: $t_p = [35 + 19.5(N-1)]$ns
(N is the number of the output, QN, in question)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0	8	4	3	3	MHz
		4.5	40	20	16	13	
		6.0	47	24	19	16	
t_{PLH}	Maximum Propagation Delay, Clock to Q1 (Figures 1 and 3)	2.0	105	210	265	313	ns
		4.5	21	42	53	63	
		6.0	18	36	45	53	
t_{PHL}		2.0	105	210	265	313	ns
		4.5	21	42	53	63	
		6.0	18	36	45	53	
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 3)	2.0	120	240	302	358	ns
		4.5	24	48	60	72	
		6.0	20	41	51	61	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*			–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

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PIN DESCRIPTIONS

INPUTS

Clock (Pin 10) – Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter.

Reset (Pin 11) – Active-high reset. A high logic level applied to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

OUTPUTS

Q1, Q4 – Q14 (Pins 9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3) – Active-high outputs. Each QN output divides the Clock input frequency by 2^N.

SWITCHING WAVEFORMS

FIGURE 1

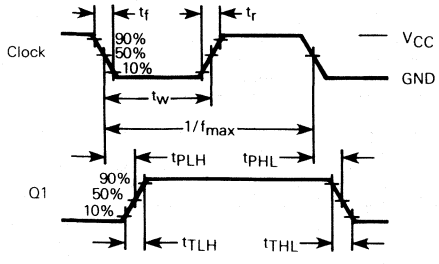


FIGURE 2

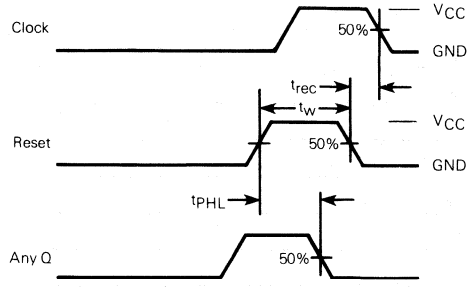
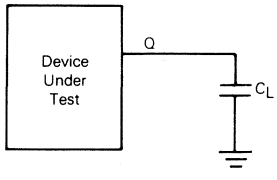
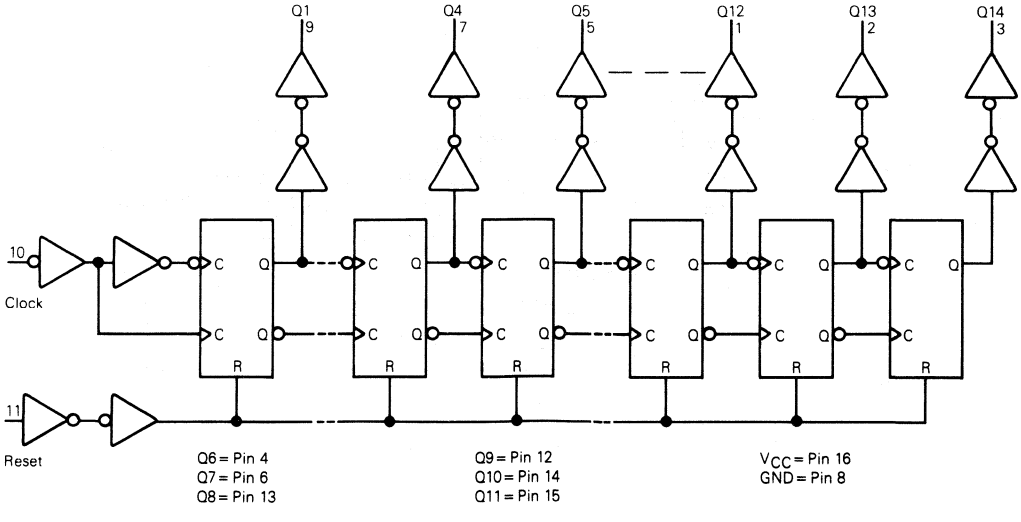


FIGURE 3 — TEST CIRCUIT



LOGIC DIAGRAM



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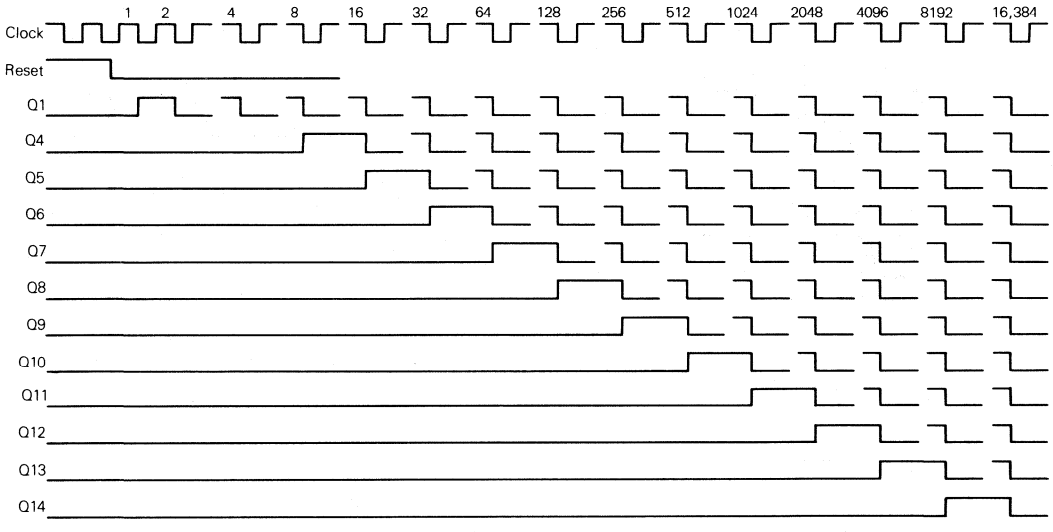
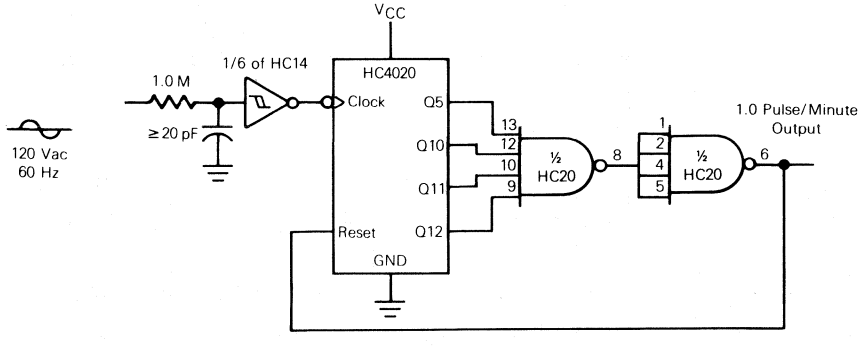
TIMING DIAGRAM



APPLICATIONS INFORMATION

TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the input of the MC54/74HC14, Schmitt-trigger inverter. The MC54/74HC14 squares-up the input waveform making it compatible with the MC54/74HC4020. By selecting outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC54/74HC20 decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



MOTOROLA

MC54/74HC4024

Advance Information

7-STAGE BINARY RIPPLE COUNTER

The MC54/74HC4024 is identical in pinout to the standard CMOS MC14024. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

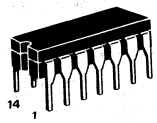
This device consists of 7 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative going edge of the Clock input. Reset is asynchronous and active high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC4024.

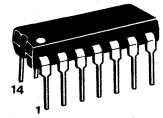
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

7-STAGE
BINARY RIPPLE COUNTER



J SUFFIX
CERAMIC PACKAGE
CASE 632



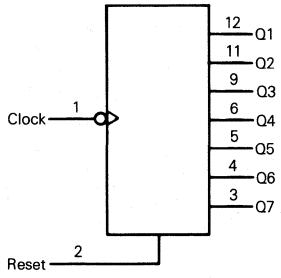
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

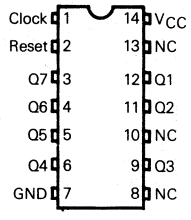
74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
No Connection = Pins 8, 10 and 13

PIN ASSIGNMENT



FUNCTION TABLE

Clock	Reset	Output State
⌐	L	No Change
⌐	L	Advance to next state
X	H	All Outputs are low

5

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	70	30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q1*	17	35	ns
t_{PHL}	(Figures 1 and 3)	15	35	
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 3)	13	35	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	5	10	ns

*For V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF maximum propagation delay from Clock to any output can be calculated with the following equation:
$t_p = [29 + 20(N - 1)]$ns
(N is the number of the output, QN, in question)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0	10	5	4	3	MHz
		4.5	50	27	21	18	
		6.0	59	32	25	21	
t_{PLH}	Maximum Propagation Delay, Clock to Q1 (Figures 1 and 3)	2.0	105	210	265	313	ns
		4.5	21	42	53	63	
		6.0	18	36	45	53	
t_{PHL}		2.0	105	210	265	313	
		4.5	21	42	53	63	
		6.0	18	36	45	53	
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 3)	2.0	105	210	265	313	ns
		4.5	21	42	53	63	
		6.0	18	36	45	53	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*			–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

PIN DESCRIPTIONS

INPUTS

Clock (Pin 1) – Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter.

Reset (Pin 2) – Active-high asynchronous reset. A high logic level applied to this input resets the counter to its zero state, thus forcing all Q outputs low.

OUTPUTS

Q1-Q7 (Pins 12, 11, 9, 6, 5, 4, 3) – Active-high outputs. Each QN output divides the Clock input frequency by 2^N.

SWITCHING WAVEFORMS

FIGURE 1

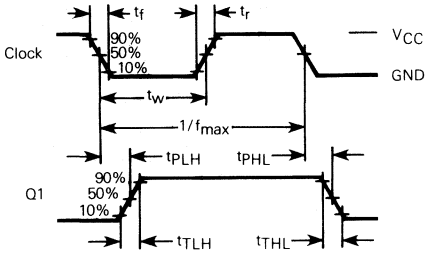


FIGURE 2

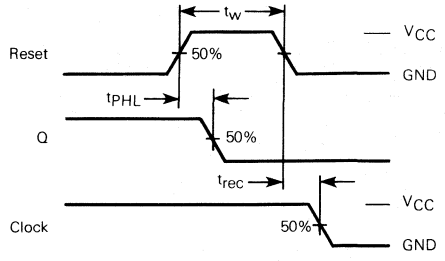
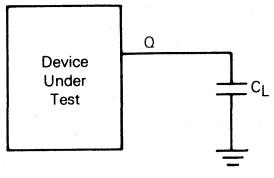
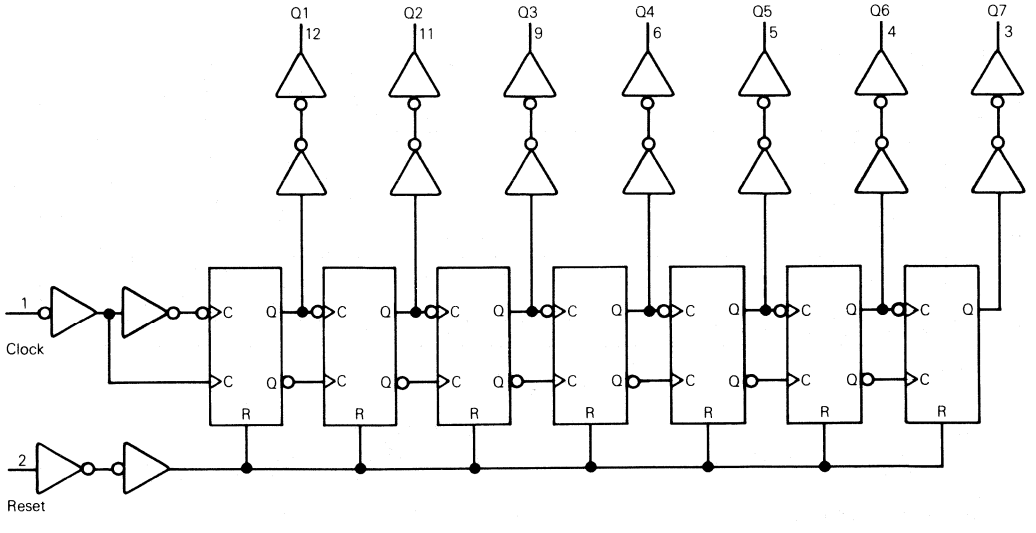


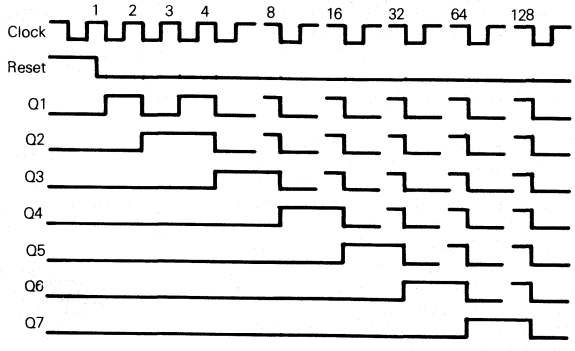
FIGURE 3 — TEST CIRCUIT



LOGIC DIAGRAM



TIMING DIAGRAM



MOTOROLA

MC54/74HC4040

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

12-STAGE
BINARY RIPPLE COUNTER

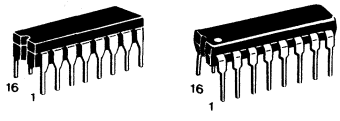
12-STAGE BINARY RIPPLE COUNTER

The MC54/74HC4040 is identical in pinout to the standard CMOS MC14040. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 12 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC4040.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620

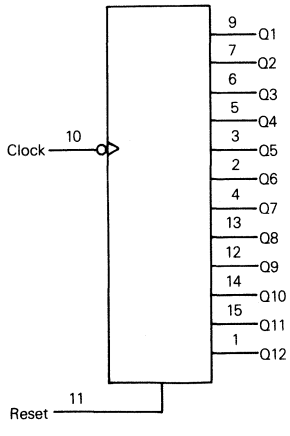
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

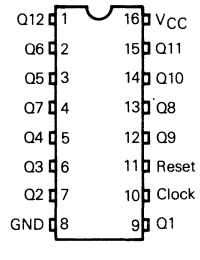
74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



FUNCTION TABLE

Clock	Reset	Output State
⎍	L	No Change
⎍	L	Advance to next state
X	H	All Outputs are low

This document contains information on a new product. Specifications and information herein are subject to change without notice.

5

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

5

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	40	30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q1* (Figures 1 and 3)	17	35	ns
t_{PHL}		17	35	
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 3)	16	40	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	5	10	ns

*For V_{CC} = 5 V, T_A = 25°C and C_L = 15 pF maximum propagation delay from Clock to any output can be calculated with the following equation: $t_p = [35 + 19.5(N-1)]$ns
(N is the number of the output, QN, in question)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0	8	4	3	3	MHz
		4.5	40	20	16	13	
		6.0	47	24	19	16	
t_{PLH}	Maximum Propagation Delay, Clock to Q1 (Figures 1 and 3)	2.0	105	210	265	313	ns
		4.5	21	42	53	63	
		6.0	18	36	45	53	
t_{PHL}		2.0	105	210	265	313	ns
		4.5	21	42	53	63	
		6.0	18	36	45	53	
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 3)	2.0	120	240	302	358	ns
		4.5	24	48	60	72	
		6.0	20	41	51	61	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*			–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

5

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25 C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

PIN DESCRIPTIONS

INPUTS

CLOCK (PIN 10) – Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter.

RESET (PIN 11) – Active-high reset. A high logic level applied to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

OUTPUTS

Q1 THRU Q12 (PINS 9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1) – Active-high outputs. Each QN output divides the Clock input frequency by 2^N.

SWITCHING WAVEFORMS

FIGURE 1

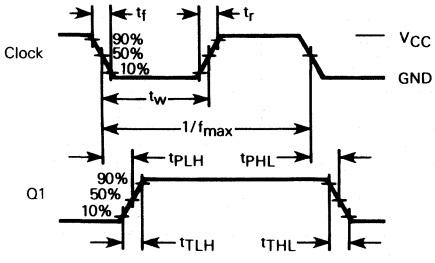


FIGURE 2

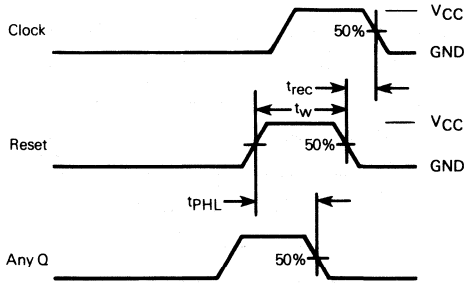
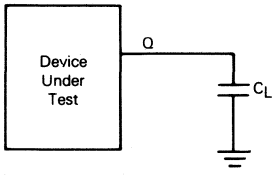
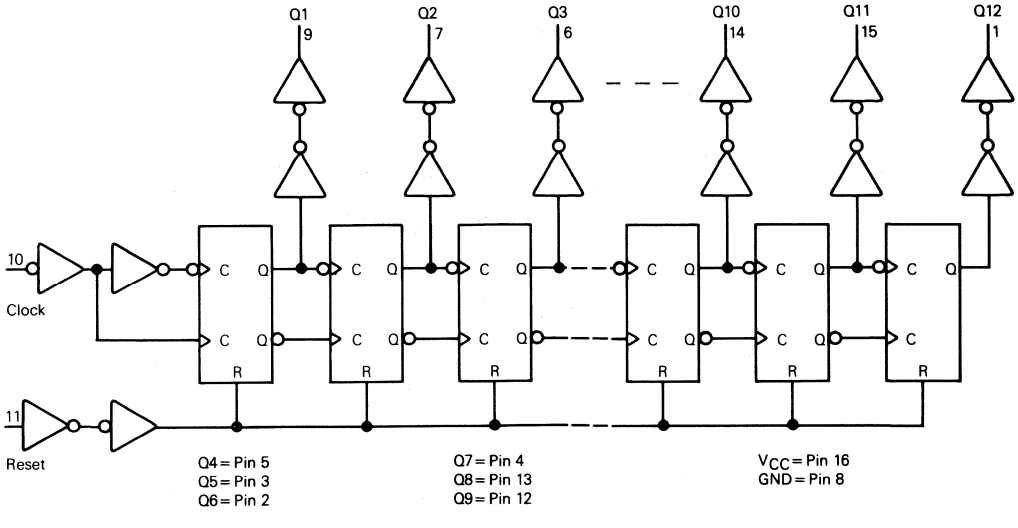


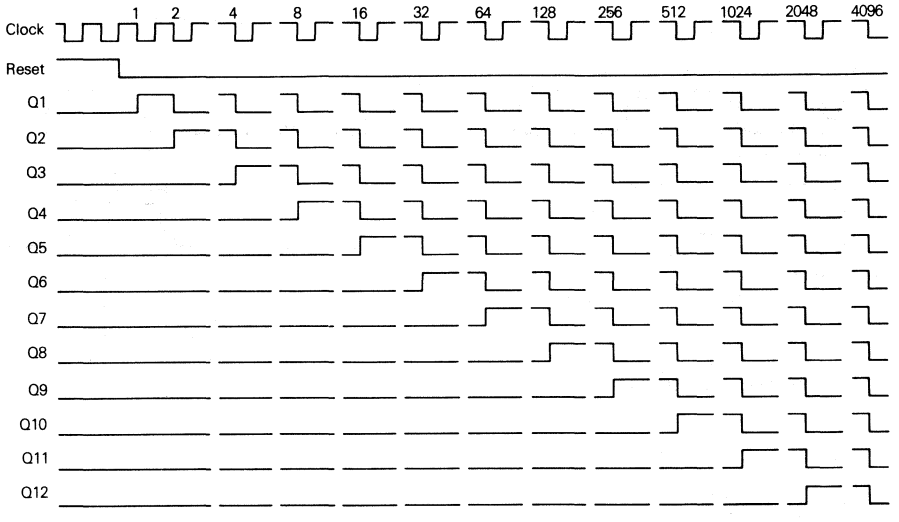
FIGURE 3 — TEST CIRCUIT



LOGIC DIAGRAM



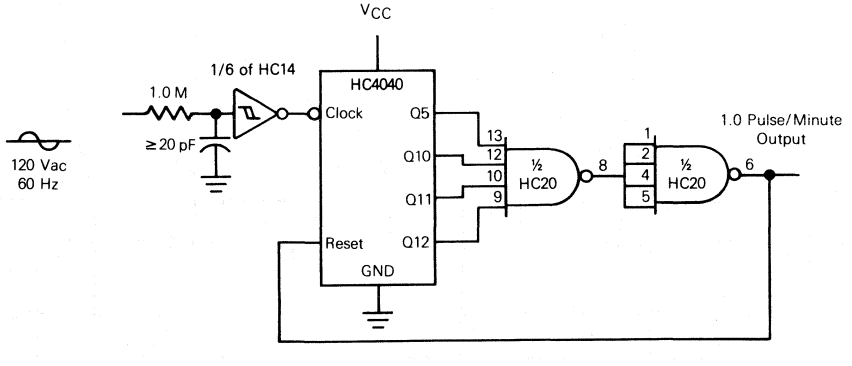
TIMING DIAGRAM



APPLICATIONS INFORMATION

TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the input of the MC54/74HC14, Schmitt-trigger inverter. The MC54/74HC14 squares-up the input waveform making it compatible with the MC54/74HC4040. By selecting outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC54/74HC20 decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



MOTOROLA

MC54/74HC4046

Product Preview

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

PHASE-LOCKED LOOP

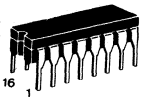
PHASE-LOCKED LOOP

The MC54/74HC4046 is identical in pinout to the MC14046 metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

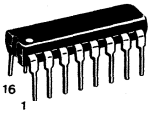
The HC4046 phase-locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs, PCA_{in} and PCB_{in}. Input PCA_{in} can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal $PC1_{out}$, and maintains 90° phase shift at the center frequency between PCA_{in} and PCB_{in} signals (both at 50% duty cycle). Phase comparator 2 (with leading-edge sensing logic) provides digital error signals $PC2_{out}$ and PCP_{out}, and maintains a 0° phase shift between PCA_{in} and PCB_{in} signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins $C1_A$, $C1_B$, R1, and R2. The source-follower output SF_{out} with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power-supply regulations.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620



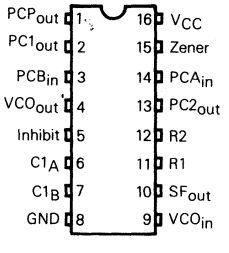
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

PIN ASSIGNMENT



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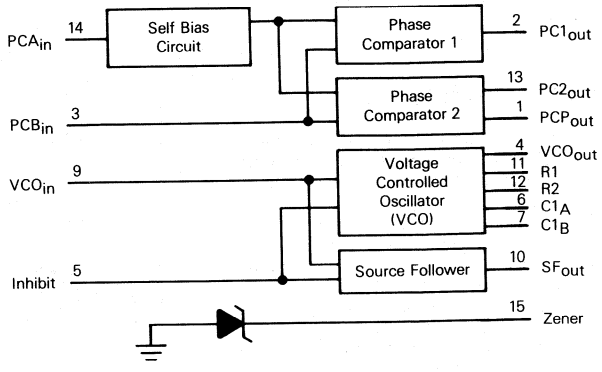
BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

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MOTOROLA

MC54/74HC4049
MC54/74HC4050

Product Preview

HEX BUFFERS/LOGIC-LEVEL DOWN CONVERTERS

The MC54/74HC4049 consists of six inverting buffers, and the MC54/74HC4050 consists of six noninverting buffers. They are identical in pinout to the MC14049 and MC14050 metal-gate CMOS buffers. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The input protection circuitry on these devices has been modified, by eliminating the protection diodes to V_{CC}, to allow the use of input voltages up to 15 volts. Thus the devices may be used as logic-level translators that will convert from a high voltage to a low voltage, while operating at the low-voltage power supply. They allow MC14000-series CMOS operating up to 15 volts to be interfaced with High-Speed CMOS at 2 to 6 volts. The protection diodes to GND are Zener diodes, which protect the inputs from both positive and negative voltage transients.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
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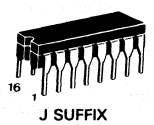
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

HEX BUFFERS/ LOGIC-LEVEL DOWN CONVERTERS



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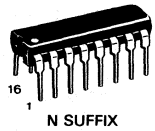
CERAMIC PACKAGE
CASE 620



N SUFFIX
PLASTIC PACKAGE
CASE 648

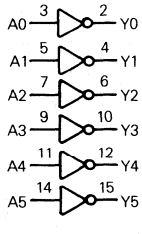
ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

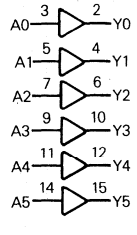
74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

LOGIC DIAGRAMS

HC4049
(inverting buffer)

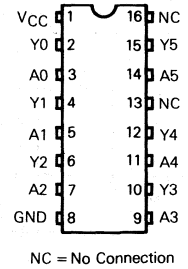


HC4050
(noninverting buffer)



V_{CC} = Pin 1
GND = Pin 8
No Connection = Pins 13, 16

PIN ASSIGNMENT



NC = No Connection

TRUTH TABLE

A Inputs	Y Outputs	
	HC4049	HC4050
L	H	L
H	L	H

5

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MOTOROLA

MC54/74HC4051

Product Preview

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

The MC54/74HC4051 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistance, and low OFF leakage current. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The HC4051 is identical in pinout to the metal-gate MC14051B. The Binary Channel-Select control inputs determine which one of the 8 Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin (active-low) is high, all 8 analog switches are turned OFF. The device has been designed so that the ON resistances, R_{ON}, are much more linear than those of metal-gate CMOS analog switches.

For other analog switch configurations, see the HC4052 and HC4053. For analog switches with latched Binary Channel-Select inputs, see the HC4351, HC4352, and HC4353.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power-Supply Voltage Range ($V_{CC} - V_{EE}$) = 3.0 to 12.0 Volts
- Digital (Control) Power-Supply Voltage Range ($V_{CC} - GND$) = 2.0 to 6.0 Volts
- Improved Linearity of ON Resistance
- Low Noise

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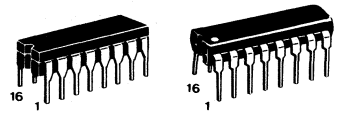
8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER



J SUFFIX
CERAMIC PACKAGE
CASE 620

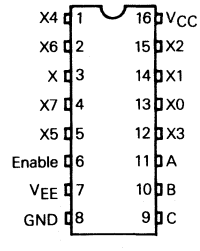
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

PIN ASSIGNMENT



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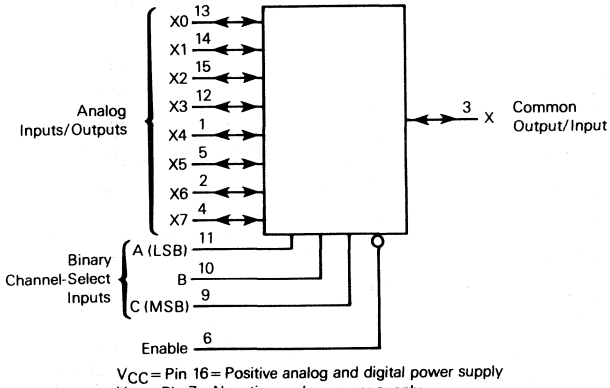


V_{CC} = Pin 16 = Positive analog and digital power supply
V_{EE} = Pin 7 = Negative analog power supply
GND = Pin 8 = Negative digital power supply

NOTE: Control inputs are referenced to GND. Analog inputs/outputs are referenced to V_{EE}. V_{EE} must be ≤ GND.

FUNCTION TABLE

Control Inputs				
	Select			
Enable	C	B	A	ON Switches
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	None

X = Don't Care

5

MOTOROLA

MC54/74HC4052

Product Preview

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

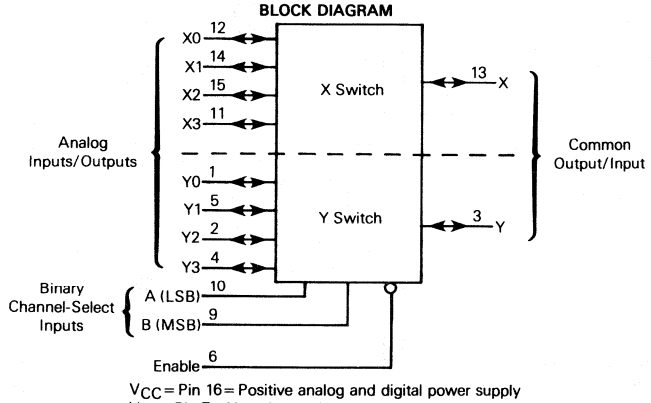
The MC54/74HC4052 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistance, and low OFF leakage current. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The HC4052 is identical in pinout to the metal-gate MC14052B. The binary Channel-Select control inputs select one switch from each of the two independent four-channel multiplexers (X and Y). The two selected Analog Inputs/Outputs are connected, by means of analog switches, to the two Common Outputs/Inputs. When the Enable pin (active-low) is high, all 8 analog switches are turned OFF. The device has been designed so that the ON resistances, R_{ON}, are much more linear than those of metal-gate CMOS analog switches.

For other analog switch configurations, see the HC4051 and HC4053. For analog switches with latched Binary Channel-Select inputs, see the HC4351, HC4352, and HC4353.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power-Supply Voltage Range ($V_{CC} - V_{EE}$) = 3.0 to 12.0 Volts
- Digital (Control) Power-Supply Voltage Range ($V_{CC} - GND$) = 2.0 to 6.0 Volts
- Improved Linearity of ON Resistance
- Low Noise

BLOCK DIAGRAM



V_{CC} = Pin 16 = Positive analog and digital power supply
V_{EE} = Pin 7 = Negative analog power supply
GND = Pin 8 = Negative digital power supply

NOTE: Control inputs are referenced to GND. Analog inputs/outputs are referenced to V_{EE}. V_{EE} must be ≤ GND.

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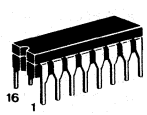
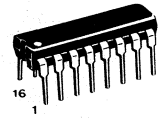
SILICON-GATE

DUAL 4-CHANNEL ANALOG MULTIPLEXER/ DEMULTIPLEXER



J SUFFIX
CERAMIC PACKAGE
CASE 620



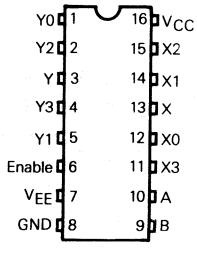
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs			
	Select		
Enable	B	A	ON Switches
L	L	L	Y0 X0
L	L	H	Y1 X1
L	H	L	Y2 X2
L	H	H	Y3 X3
H	X	X	None

X = Don't Care

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MOTOROLA

MC54/74HC4053

Product Preview

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

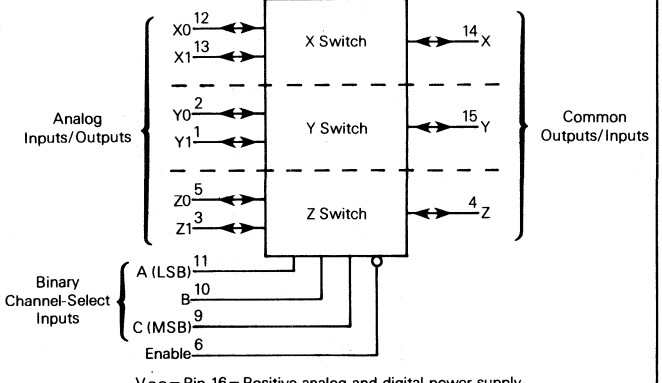
The MC54/74HC4053 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistance, and low OFF leakage current. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The HC4053 is identical in pinout to the metal-gate MC14053B. The binary Channel-Select control inputs determine which combination of the 8 Analog Inputs/Outputs is to be connected, by means of analog switches, to the Common Outputs/Inputs. When the Enable pin (active-low) is high, all 8 analog switches are turned OFF. The device has been designed so that the ON resistance, R_{ON}, are much more linear than those of metal-gate CMOS analog switches.

For other analog switch configurations, see the HC4051 and HC4052. For analog switches with latched Binary Channel-Select inputs, see the HC4351, HC4352, and HC4353.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power-Supply Voltage Range ($V_{CC} - V_{EE}$) = 3.0 to 12.0 Volts
- Digital (Control) Power-Supply Voltage Range ($V_{CC} - GND$) = 2.0 to 6.0 Volts
- Improved Linearity of ON Resistance
- Low Noise

BLOCK DIAGRAM



V_{CC} = Pin 16 = Positive analog and digital power supply
V_{EE} = Pin 7 = Negative analog power supply
GND = Pin 8 = Negative digital power supply

NOTE: Control inputs are referenced to GND. Analog inputs/outputs are referenced to V_{EE}. V_{EE} must be ≤ GND.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
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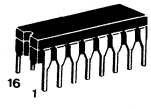
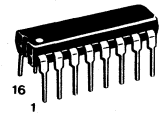
TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/ DEMULTIPLEXER



J SUFFIX
CERAMIC PACKAGE
CASE 620



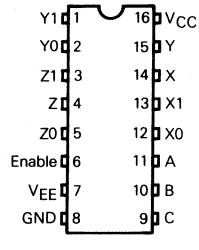
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs						
	Select					
Enable	C	B	A	ON Switches		
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	None		

X = Don't Care

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MOTOROLA

MC54/74HC4060

Advance Information

14-STAGE BINARY RIPPLE COUNTER WITH OSCILLATOR

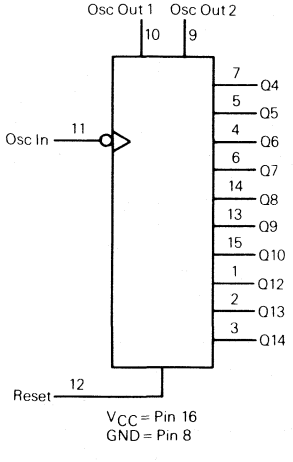
The MC54/74HC4060 is identical in pinout to the standard CMOS MC14060B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 14 master-slave flip-flops and an oscillator with a frequency that is controlled either by a crystal or by an RC circuit connected externally. The output of each flip-flop feeds the next, and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of Osc In. The active-high Reset is asynchronous and disables the oscillator to allow very low power consumption during standby operation.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with Osc Out 2 of the HC4060.

- On-Chip RC or Crystal Oscillator Provisions
- May Be Driven by External Frequency Source
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum (Q Outputs)
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2.5 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs
- Chip Complexity: 390 FETs

BLOCK DIAGRAM



HIGH-PERFORMANCE
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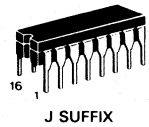
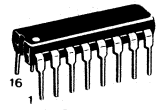
14-STAGE BINARY RIPPLE COUNTER WITH OSCILLATOR



J SUFFIX
CERAMIC PACKAGE
CASE 620



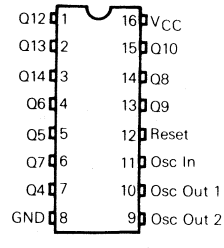
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Osc In	Reset	Output State
⌐	L	No Change
¬	L	Advance to next state
X	H	All Outputs are low

ADI-917

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.5*	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	No Limit	ns

* The oscillator is guaranteed to function at 2.5 V minimum. However, parametrics are tested at 2.0 V by driving Pin 11 with an external clock source.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C 54HC and 74HC		85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed Limit			Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage (Q4-Q10, Q12-Q14)	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage (Q4-Q10, Q12-Q14)	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
V_{OH}	Maximum High-Level Output Voltage (Osc Out 1, Osc Out 2)	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.99 4.49 5.99	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−1.0 mA I_{out}=−1.3 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low Level Output Voltage (Osc Out 1, Osc Out 2)	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.01 0.01 0.01	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=1.0 mA I_{out}=1.3 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	45	25	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Osc In to Q4† (Figures 1 and 3)	47	94	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Osc In to Q14† (Figures 1 and 3)	145	289	ns
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 3)	16	40	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Q (Figures 1 and 3)	5	10	ns

†Note: For V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF maximum propagation delay from Osc In to other Q outputs can be calculated with the following equation:

$t_P = [35 + 19.5(N - 1)]$ns

(N is the number of the output, QN, in question)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0	8	4	3	2	MHz
		4.5	40	20	16	13	
		6.0	47	24	19	16	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Osc In to Q4* (Figures 1 and 3)	2.0	265	530	670	790	ns
		4.5	53	106	134	158	
		6.0	45	90	114	134	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Osc In to Q14* (Figures 1 and 3)	2.0	800	1600	2015	2385	ns
		4.5	160	320	403	477	
		6.0	136	272	343	405	
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 3)	2.0	120	240	300	360	ns
		4.5	24	48	60	72	
		6.0	20	41	51	61	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Q (Figures 1 and 3)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance**		30	–	–	–	pF

*Note: For T_A = 25°C and C_L = 50 pF, maximum propagation delay from Osc In to other Q outputs may be calculated with the following equations:

V_{CC} = 2.0 V: $t_P = [205 + 107.5(N - 1)]$ns

V_{CC} = 4.5 V: $t_P = [41 + 21.5(N - 1)]$ns

V_{CC} = 6.0 V: $t_P = [35 + 18.3(N - 1)]$ns

For performance over temperature, see the "Design Considerations" section of the Motorola High-Speed CMOS Logic Data Book (DL129).

** C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{rec}	Minimum Recovery Time, Reset Inactive to Osc In* (Figure 2)	2.0	50	100	125	150	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_w	Minimum Pulse Width, Osc In (Figure 1)	2.0	40	80	100	120	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	40	80	100	120	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–		No Limit			ns

*Osc In driven with external clock.

PIN DESCRIPTIONS

INPUTS

Osc In (Pin 11) – Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter. Osc In may be driven by an external clock source.

Reset (Pin 12) – Active-high reset. A high logic level applied to this input asynchronously resets the counter to its zero state (forcing all Q outputs low) and disables the oscillator.

OUTPUTS

Q4-Q10, Q12-Q14, (Pins 7, 5, 4, 6, 14, 13, 15, 1, 2, 2) – Active-high outputs. Each QN output divides the oscillator frequency by 2^N. The user should note that Q1, Q2, Q3, and Q11 are not available as outputs.

Osc Out 1, Osc Out 2 (Pins 10, 9) – Oscillator outputs. These pins are used in conjunction with Osc In and the external components to form an oscillator. (See Figures 4 and 5). When Osc In is being driven with an external clock source, Osc Out 1 and Osc Out 2 may be left open circuited or may be used to drive 2.5 LSTTL loads, maximum.

SWITCHING WAVEFORMS

FIGURE 1

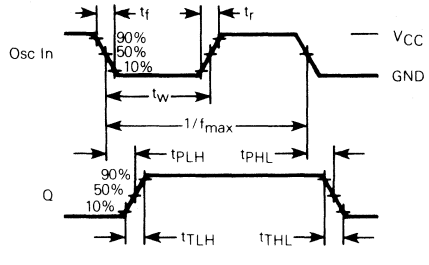


FIGURE 2

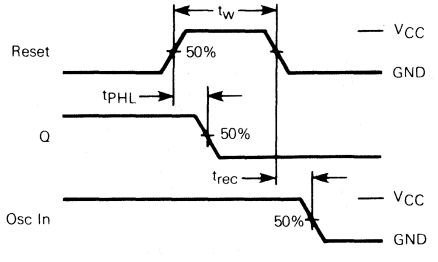
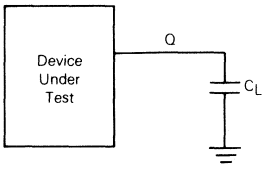


FIGURE 3 – TEST CIRCUIT



LOGIC DIAGRAM

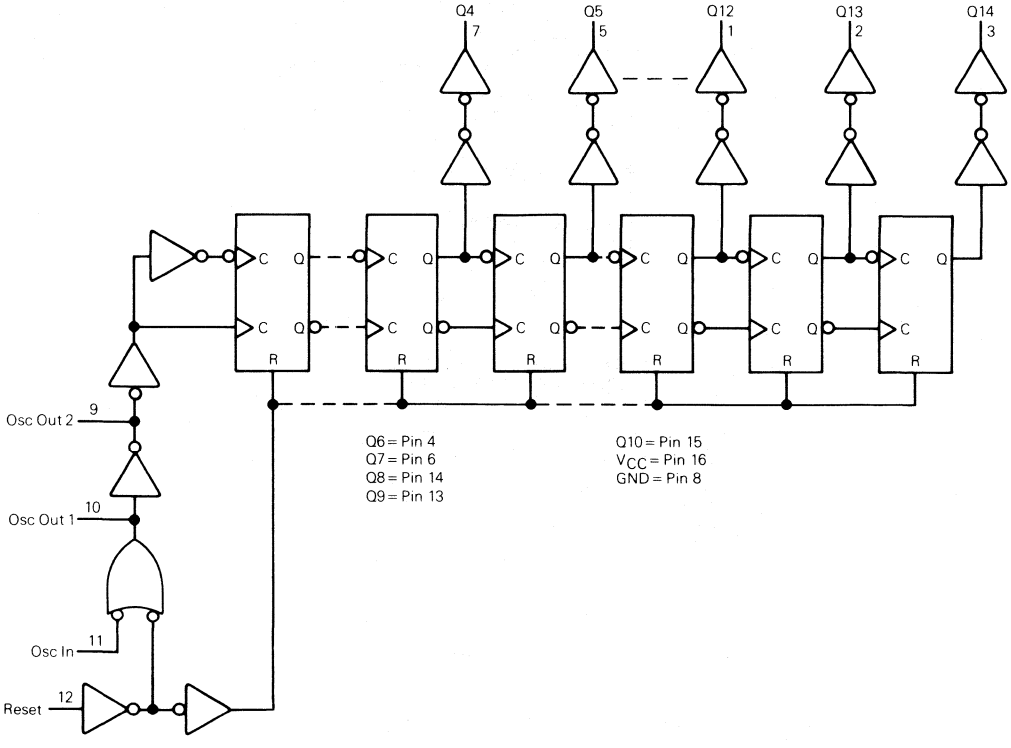
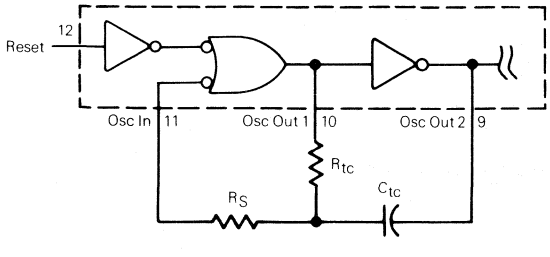


FIGURE 4 — OSCILLATOR CIRCUIT USING RC CONFIGURATION



For $2.0\ V \leq V_{CC} \leq 6.0\ V$
$R_S > 2\ R_{tc}$
$400\ Hz \leq f \leq 400\ kHz$:

$$f \approx \frac{1}{3\ R_{tc} C_{tc}}$$ (f in Hz, R_{tc} in ohms, C_{tc} in farads)

The formula may vary for other frequencies.

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FIGURE 5 – PIERCE CRYSTAL OSCILLATOR CIRCUIT

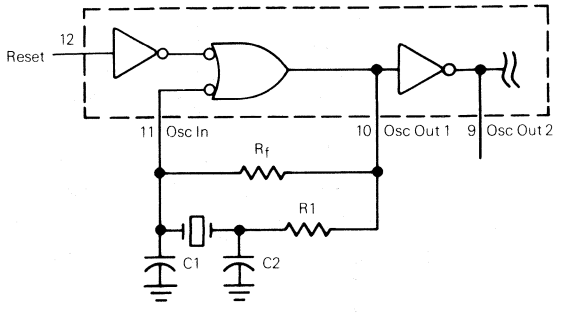


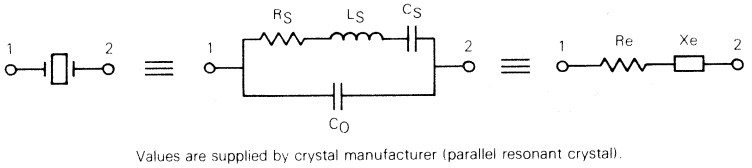
TABLE 1 – CRYSTAL OSCILLATOR AMPLIFIER SPECIFICATIONS

$T_A = 25°C$ (Input = Pin 11, Output = Pin 10)

Type		Positive Reactance (Pierce)
Input Resistance, R_{in}		60 MΩ minimum
Output Impedance, Z_{out} (4.5 V supply)		200 Ω (see text)
Input Capacitance, C_{in}		5 pF typical
Output Capacitance, C_{out}		7 pF typical
Series Capacitance, C_a		5 pF typical
Open loop voltage gain with output at full swing, α	2 Vdc supply	2.00 expected minimum
	3 Vdc supply	1.75 expected minimum
	4 Vdc supply	1.65 expected minimum
	5 Vdc supply	1.45 expected minimum
	6 Vdc supply	1.42 expected minimum

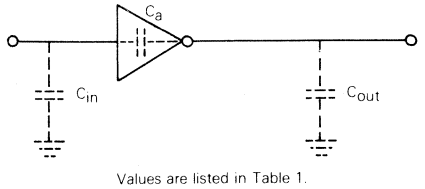
PIERCE CRYSTAL OSCILLATOR DESIGN

FIGURE 6 – EQUIVALENT CRYSTAL NETWORKS



Values are supplied by crystal manufacturer (parallel resonant crystal).

FIGURE 7 – PARASITIC CAPACITANCES OF THE AMPLIFIER



Values are listed in Table 1.

TABLE 2 — DESIGN EQUATIONS

(1) $K = \frac{1}{1-S} + \frac{\tan(\triangle\phi)}{(1-S)\left(\frac{X_{L(eff)}}{R_e}\right)}$

(2) $X_{L(eff)} = \frac{X_e}{1+\beta K}$

(3) $X_{C2} = X_{L(eff)} = X_e - X_{C1} - X_{C_{in}}$

(4) $X_{C1} + X_{C_{in}} = \beta X_{L(eff)} K$ at $\phi = 180°$

(5) $R = X_{C1}\left(\frac{X_{L(eff)}}{R_e}\right)(K-1)$

(6) $C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_O + \frac{C1C2}{C1+C2}$

Notes on equation 1: $S \equiv$ the stability factor of the oscillator. A value of 0.75 provides good stability with low power consumption.
$\triangle\phi \equiv 180°$ minus the phase shift through the amplifier at the desired frequency and power supply voltage. $\triangle\phi$ should be measured by the user.
$X_{L(eff)} \equiv$ the effective inductance of the circuit is parallel with C_2.
$R_e \equiv$ the equivalent resistance of the crystal. See Figure 6.

Notes on equation 2: $X_e \equiv$ the effective reactance of the crystal.
$\beta \equiv$ the attenuation of the feedback network. $\beta > \frac{1}{\alpha}$ where α is defined in Table 1. To minimize power consumption, β should be large.

Notes on equation 5: $R \equiv R1 + Z_{out}$ where R1 is shown in Figure 5 and Z_{out} is the output impedance of the amplifier. $Z_{out} \approx 200\ \Omega$ is a reasonable assumption @ $V_{CC} = 4.5$ V and $V_{out} = V_{CC}/2$. Z_{out} is dependent on the supply voltage, output voltage, temperature, and date code (batch number), and may be assumed to be resistive (not varying with frequency) when equation 5 is considered.

Notes on equation 6: $C_L \equiv$ the shunt load capacitance (must be specified when ordering a crystal). Common values for C_L are 20 pF or 32 pF.

CHOOSING R1

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 limits the drive level.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at Osc Out 2 (Pin 9). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

SELECTING R_f

The feedback resistor, R_f, typically ranges up to 20 MΩ. R_f determines the gain and bandwidth of the amplifier. Proper bandwidth insures oscillation at the correct frequency plus roll-off to minimize gain at undesirable frequencies, such as the first overtone. R_f must be large enough so as to not affect the phase of the feedback network in an appreciable manner.

ACKNOWLEDGEMENTS AND RECOMMENDED REFERENCES

The following publications were used in preparing this data sheet and are hereby acknowledged and recommended for reading:

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

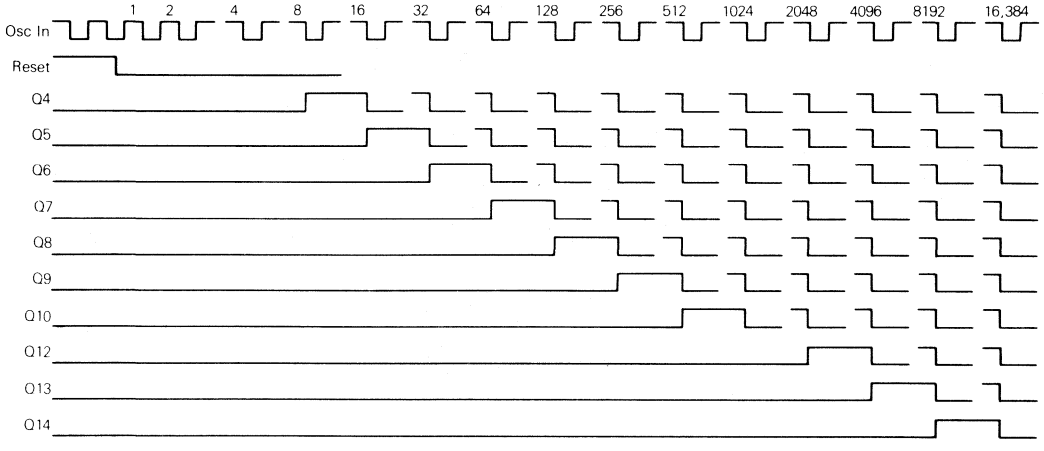
ALSO RECOMMENDED FOR READING:

E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", Proc. IEEE, Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", Electro-Technology, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", Electronic Design, May, 1966.

TIMING DIAGRAM



MOTOROLA

MC54/74HC4066

Product Preview

QUAD ANALOG SWITCH/MULTIPLEXER/DEMULTIPLEXER WITH ENHANCED ON-RESISTANCE LINEARITY

The MC54/74HC4066 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistance, and low OFF-channel leakage current. This analog switch/multiplexer/demultiplexer controls analog voltages that may vary across the full power-supply range (from V_{CC} to GND).

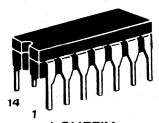
The HC4066 is identical in pinout to the metal-gate CMOS MC14016 and MC14066. Each device has four independent switches that may control either analog or digital signals. The device has been designed so that the ON resistances, R_{ON}, are more linear than those found in the HC4016 and much more linear than those of metal-gate CMOS analog switches.

This device is identical in both function and pinout to the HC4016. For analog switches with voltage-level translators, see the HC4316.

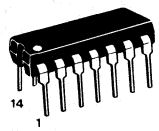
- Near Linear R_{ON}, Ideal for Switched-Capacitor Filter Designs
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power-Supply Voltage Range (V_{CC} – GND) = 3.0 to 12.0 Volts
- Digital (On/Off Control) Power-Supply Voltage Range (V_{CC} – GND) = 3.0 to 12.0 Volts
- Low Noise

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD ANALOG SWITCH/ MULTIPLEXER/DEMULTIPLEXER WITH ENHANCED ON-RESISTANCE LINEARITY



J SUFFIX
CERAMIC PACKAGE
CASE 632



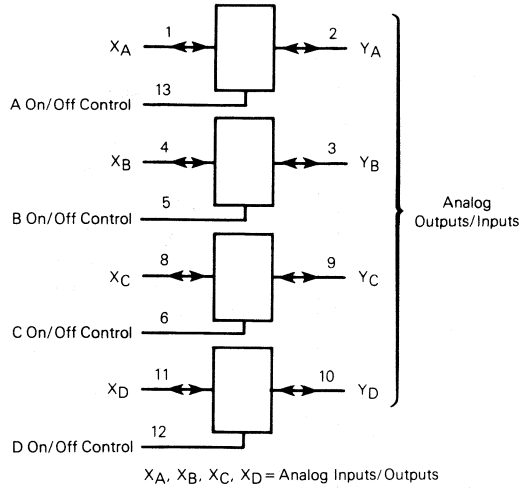
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: –55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

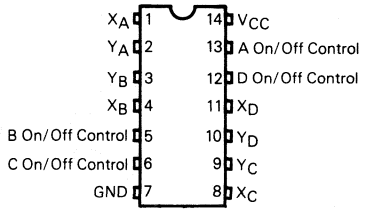
74 Series: –40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

BLOCK DIAGRAM



X_A, X_B, X_C, X_D = Analog Inputs/Outputs
V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	off
H	on

MOTOROLA

MC54/74HC4075

Advance Information

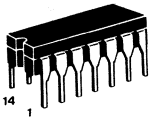
HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

TRIPLE 3-INPUT OR GATE

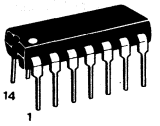
TRIPLE 3-INPUT OR GATE

The MC54/74HC4075 is identical in pinout to the MC14075. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 632



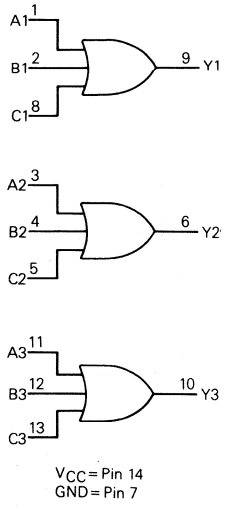
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

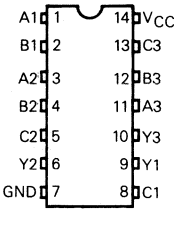
LOGIC DIAGRAM



Y = A + B + C

V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	2	20	40	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A, B, or C to Output Y	10	20	ns
t_{PHL}	(Figures 1 and 2)	11	20	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 1 and 2)	2.0	58	115	145	171	ns
		4.5	12	23	29	34	
		6.0	10	20	25	29	
t_{PHL}		2.0	58	115	145	171	ns
		4.5	12	23	29	34	
		6.0	10	20	25	29	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance	–	5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*	–		–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption per gate:
$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

FIGURE 1 — SWITCHING WAVEFORMS

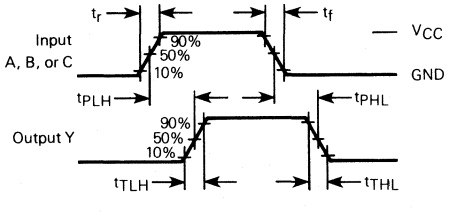
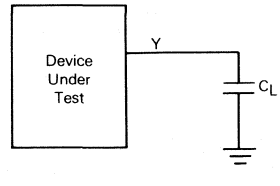


FIGURE 2 — TEST CIRCUIT



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MOTOROLA

MC54/74HC4078

Advance Information

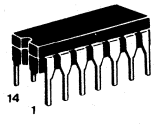
HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

8-INPUT NOR/OR GATE

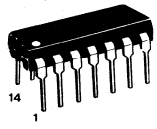
8-INPUT NOR/OR GATE

The MC54/74HC4078 is identical in pinout to the CD4078B metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 20 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs
- Chip Complexity: 30 FETs or 7.5 Equivalent Gates



J SUFFIX
CERAMIC PACKAGE
CASE 632



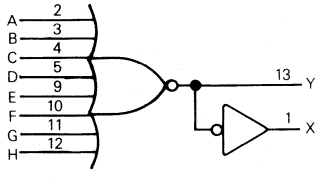
N SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

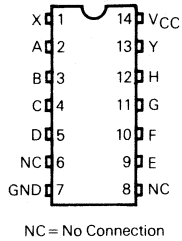
FUNCTION DIAGRAM



$Y = \overline{A+B+C+D+E+F+G+H}$
$X = A+B+C+D+E+F+G+H$

V_{CC} = Pin 14
GND = Pin 7
No Connection = Pins 6, 8

PIN ASSIGNMENT



NC = No Connection

ADI-1016

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12 mW/°C from 65°C to 85°C
Ceramic "J" Package: −12 mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				25°C ★ 54HC and 74HC	85°C 74HC	125°C 54HC	
Symbol	Parameter	Test Conditions	V_{CC}	Typical	Guaranteed Limit		Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	 4.5 6.0	 4.20 5.80	 3.98 5.48	 3.84 5.34	 3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	 4.5 6.0	 0.22 0.18	 0.26 0.26	 0.33 0.33	 0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	0.01	2	20	40	μA

★ The 25°C Guaranteed Limits are also valid for the 74HC series at −40°C and the 54HC series at −55°C.

5

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 3)	14	22	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Any Input to Output X (Figures 2 and 3)	16	24	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1, 2, and 3)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C ★ 54HC and 74HC Typical	25°C ★ 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Any Input to Ouput Y (Figures 1 and 3)	2.0	47	130	165	195	ns
		4.5	17	26	33	39	
		6.0	14	22	28	33	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Any Input to Output X (Figures 2 and 3)	2.0	50	140	175	210	ns
		4.5	20	28	35	42	
		6.0	17	24	30	36	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1, 2, and 3)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		100	–	–	–	pF

★ The 25°C Guaranteed Limits are also valid for the 74HC series at −40°C and the 54HC series at −55°C.

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

SWITCHING WAVEFORMS AND TEST CIRCUIT

FIGURE 1

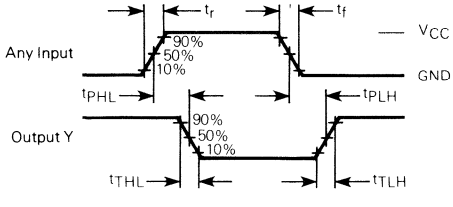


FIGURE 2

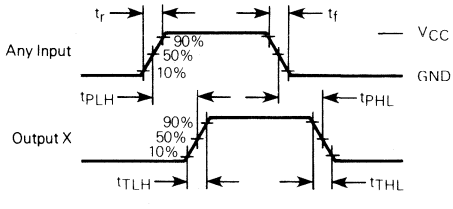
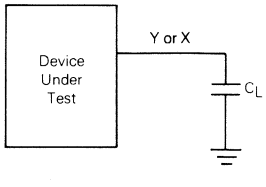
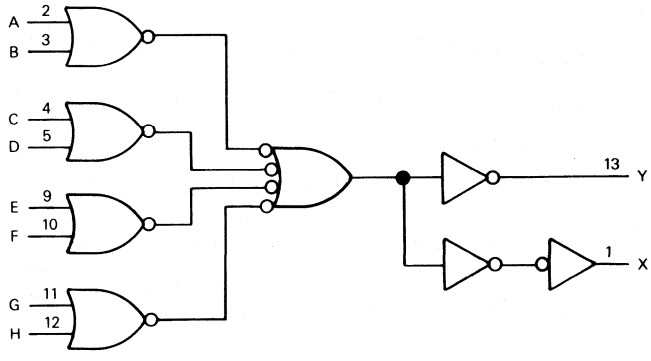


FIGURE 3 — TEST CIRCUIT



5

LOGIC DIAGRAM



MOTOROLA

MC54/74HC4316

Product Preview

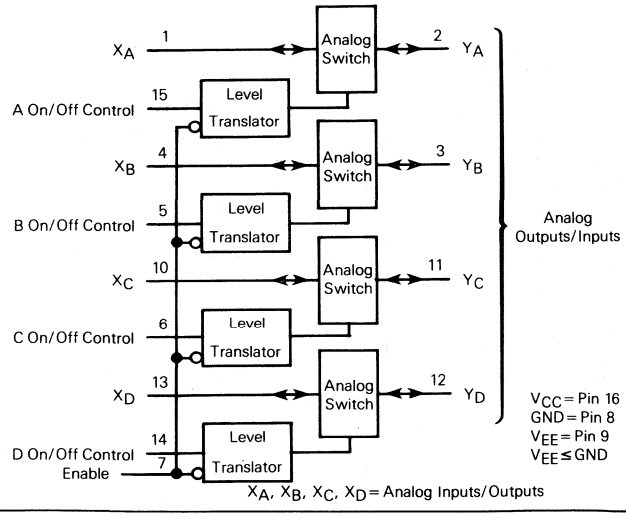
QUAD ANALOG SWITCH/MULTIPLEXER/DEMULTIPLEXER WITH SEPARATE ANALOG AND DIGITAL POWER SUPPLIES

The MC54/74HC4316 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistance, and low OFF-channel leakage current. This analog switch/multiplexer/demultiplexer controls analog voltages that may vary across the full analog power-supply range (from V_{CC} to V_{EE}).

The HC4316 is similar in function to the metal-gate CMOS MC14016 and MC14066, and to the High-Speed CMOS HC4016 and HC4066. Each device has four independent switches that may control either analog or digital signals. The device has been designed so that the ON resistances, R_{ON}, are much more linear than those of metal-gate CMOS analog switches. Logic-level translators are provided so that the On/Off Control and Enable logic-level voltages need only be V_{CC} and GND, while the switch is passing signals ranging between V_{CC} and V_{EE}. When the Enable pin (active-low) is high, all four analog switches are turned off.

- Logic-Level Translator for On/Off Control and Enable Inputs
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Quiescent Current: 80 μA Maximum Over Full Temperature Range (74HC series)
- Diode Protection on All Inputs/Outputs
- Analog Power-Supply Voltage Range ($V_{CC} - V_{EE}$) = 3.0 to 12.0 Volts
- Digital (Control) Power-Supply Voltage Range (V_{CC} – GND) = 3.0 to 6.0 Volts, Independent of V_{EE}
- Improved Linearity of ON Resistance

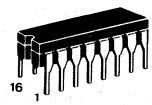
BLOCK DIAGRAM



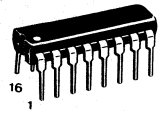
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

QUAD ANALOG SWITCH/ MULTIPLEXER/DEMULTIPLEXER WITH SEPARATE ANALOG AND DIGITAL POWER SUPPLIES



J SUFFIX
CERAMIC PACKAGE
CASE 620



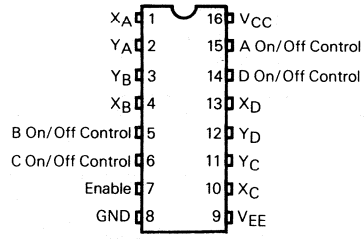
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: –55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: –40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		State of
Enable	On/Off Control	Analog Switch
L	H	on
L	L	off
H	X	off

5

MOTOROLA

MC54/74HC4351

Product Preview

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH ADDRESS LATCH

The MC54/74HC4351 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistance, and low OFF leakage current. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The binary Channel-Select control inputs determine which one of the 8 Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. The data at the Channel-Select inputs may be latched by using the active-low Latch Enable pin. When Latch Enable is high, the latch is transparent.

When either of the two Enable pins, Enable 1 (active-low) and Enable 2 (active-high), is inactive, all 8 analog switches are turned OFF. The device has been designed so that the ON resistances, R_{ON}, are much more linear than those of metal-gate CMOS analog switches.

For other latched analog switch configurations, see the HC4352 and HC4353. For analog switches without Channel-Select input latches, see the HC4051, HC4052, and HC4053.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Quiescent Current: 80 μA Maximum Over Full Temperature Range (74 series)
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power-Supply Voltage Range ($V_{CC} - V_{EE}$) = 3.0 to 12.0 Volts
- Digital (Control) Power-Supply Voltage Range ($V_{CC} - GND$) = 2.0 to 6.0 Volts
- Improved Linearity of ON Resistance
- Low Noise

FUNCTION TABLE

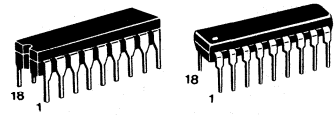
Control Inputs					ON Switches (LE = H)*
		Select			
Enable 1	Enable 2	C	B	A	
L	H	L	L	L	X0
L	H	L	L	H	X1
L	H	L	H	L	X2
L	H	L	H	H	X3
L	H	H	L	L	X4
L	H	H	L	H	X5
L	H	H	H	L	X6
L	H	H	H	H	X7
H	L	X	X	X	None

X = Don't Care

*When Latch Enable is low, the Channel-Select data is latched, and the switches do not change state.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH ADDRESS LATCH



J SUFFIX
CERAMIC PACKAGE
CASE 726

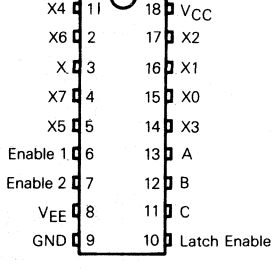
N SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

PIN ASSIGNMENT



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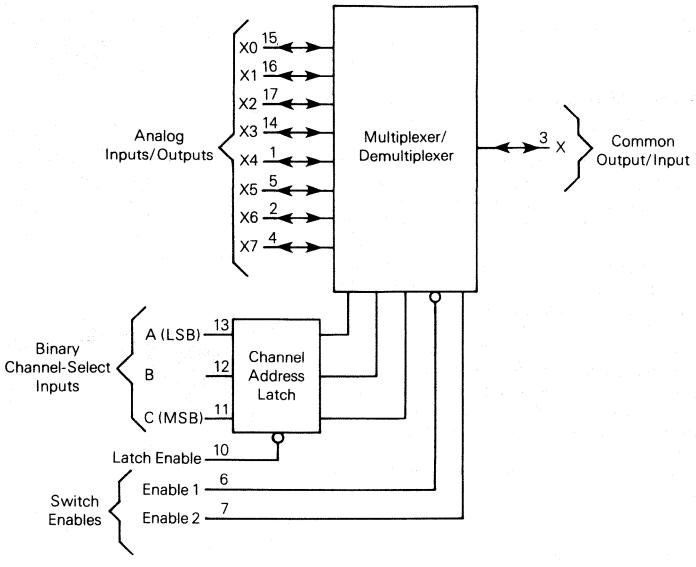
This document contains information on a product under development. Motorola reserves the right the change or discontinue this product without notice.

BLOCK DIAGRAM



V_{CC} = Pin 18 = Postive analog and digital power supply
V_{EE} = Pin 8 = Negative analog power supply
GND = Pin 9 = Negative digital power supply

NOTE: Control inputs are referenced to GND. Analog inputs/outputs are referenced to V_{EE}. V_{EE} must be $\leq$ GND.

5

MOTOROLA

MC54/74HC4352

Product Preview

DUAL 4-CHANNEL ANALOG MULTIPLEXER/ DEMULTIPLEXER WITH ADDRESS LATCH

The MC54/74HC4352 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistance, and low OFF leakage current. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The binary Channel-Select control inputs select one switch from each of the two independent four-channel multiplexers (X and Y). The two selected Analog Inputs/Outputs are connected, by means of analog switches, to the two Common Outputs/Inputs. The data at the Channel-Select inputs may be latched by using the active-low Latch Enable pin. When Latch Enable is high, the latch is transparent.

When either of the two Enable pins, Enable 1 (active-low) and Enable 2 (active-high), is inactive, all 8 analog switches are turned OFF. The device has been designed so that the ON resistances, R_{ON}, are much more linear than those of metal-gate CMOS analog switches.

For other latched analog switch configurations, see the HC4351 and HC4353. For analog switches without Channel-Select input latches, see the HC4051, HC4052, and HC4053.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Quiescent Current: 80 μA Maximum Over Full Temperature Range (74 series)
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power-Supply Voltage Range ($V_{CC} - V_{EE}$) = 3.0 to 12.0 Volts
- Digital (Control) Power-Supply Voltage Range ($V_{CC} - GND$) = 2.0 to 6.0 Volts
- Improved Linearity of ON Resistance
- Low Noise

FUNCTION TABLE

Control Inputs				
		Select		ON Switches
Enable 1	Enable 2	B	A	(LE = H)*
L	H	L	L	Y0 X0
L	H	L	H	Y1 X1
L	H	H	L	Y2 X2
L	H	H	H	Y3 X3
H	L	X	X	None

X = Don't Care

*When Latch Enable is low, the Channel-Select data is latched, and the switches do not change state.

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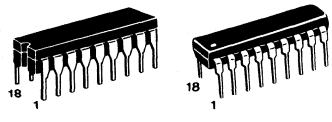
HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL 4-CHANNEL ANALOG MULTIPLEXER/ DEMULTIPLEXER WITH ADDRESS LATCH



J SUFFIX
CERAMIC PACKAGE
CASE 726

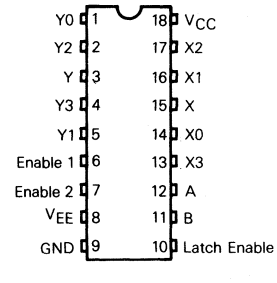
N SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

PIN ASSIGNMENT



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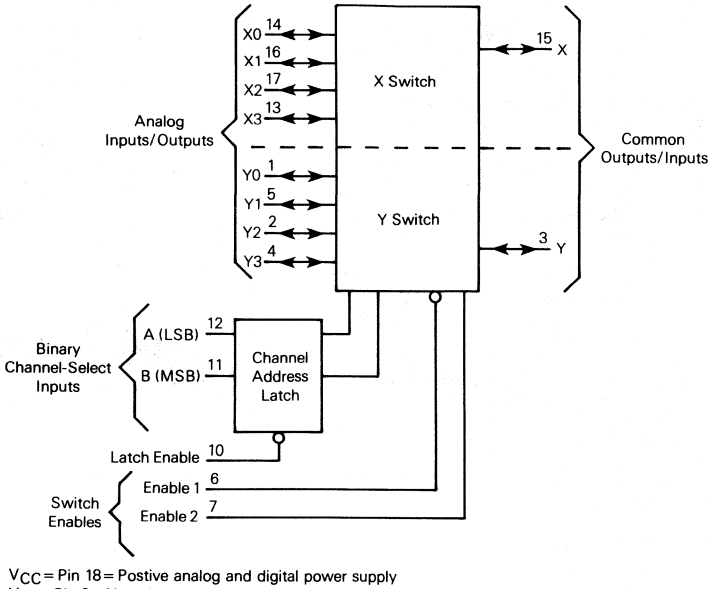
BLOCK DIAGRAM



V_{CC} = Pin 18 = Postive analog and digital power supply
V_{EE} = Pin 8 = Negative analog power supply
GND = Pin 9 = Negative digital power supply

NOTE: Control inputs are referenced to GND. Analog inputs/outputs are referenced to V_{EE}. V_{EE} must be ≤ GND.

5

MOTOROLA

MC54/74HC4353

Product Preview

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/ DEMULTIPLEXER WITH ADDRESS LATCH

The MC54/74HC4353 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistance, and low OFF leakage current. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The binary Channel-Select control inputs determine which combination of the 8 Analog Inputs/Outputs is to be connected, by means of analog switches, to the Common Outputs/Inputs. The data at the Channel-Select inputs may be latched by using the active-low Latch Enable pin. When Latch Enable is high, the latch is transparent.

When either of the two Enable pins, Enable 1 (active-low) and Enable 2 (active-high), is inactive, all 8 analog switches are turned OFF. The device has been designed so that the ON resistances, R_{ON}, are much more linear than those of metal-gate CMOS analog switches.

For other latched analog switch configurations, see the HC4351 and HC4352. For analog switches without Channel-Select input latches, see the HC4051, HC4052, and HC4053.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Quiescent Current: 80 μA Maximum Over Full Temperature Range (74 series)
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power-Supply Voltage Range ($V_{CC} - V_{EE}$) = 3.0 to 12.0 Volts
- Digital (Control) Power-Supply Voltage Range ($V_{CC} - GND$) = 2.0 to 6.0 Volts
- Improved Linearity of ON Resistance
- Low Noise

FUNCTION TABLE

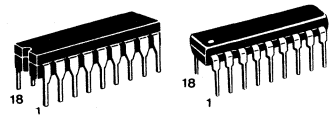
Control Inputs					ON Switches (LE = H)*		
		Select					
Enable 1	Enable 2	C	B	A			
L	H	L	L	L	Z0	Y0	X0
L	H	L	L	H	Z0	Y0	X1
L	H	L	H	L	Z0	Y1	X0
L	H	L	H	H	Z0	Y1	X1
L	H	H	L	L	Z1	Y0	X0
L	H	H	L	H	Z1	Y0	X1
L	H	H	H	L	Z1	Y1	X0
L	H	H	H	H	Z1	Y1	X1
H	L	X	X	X	None		

X = Don't Care

*When Latch Enable is low, the Channel-Select data is latched, and the switches do not change state.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/ DEMULTIPLEXER WITH ADDRESS LATCH



J SUFFIX
CERAMIC PACKAGE
CASE 726

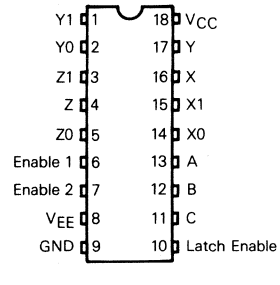
N SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

PIN ASSIGNMENT



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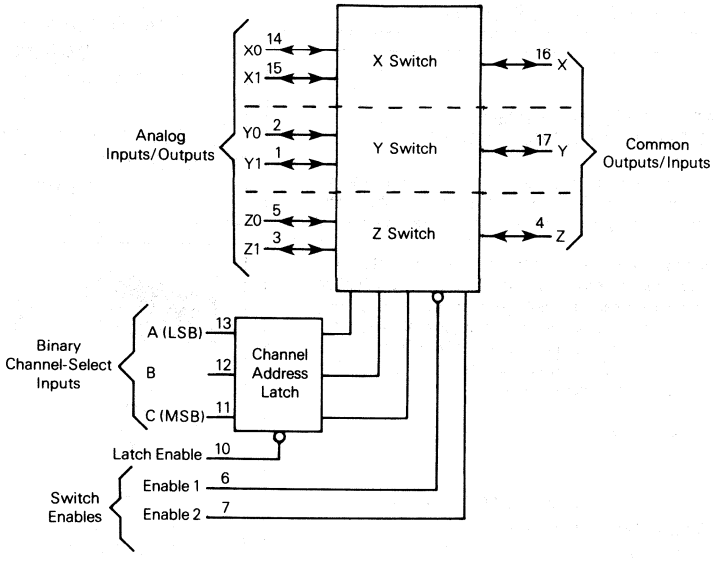
This document contains information on a product under development. Motorola reserves the right the change or discontinue this product without notice.

BLOCK DIAGRAM



V_{CC} = Pin 18 = Postive analog and digital power supply
V_{EE} = Pin 8 = Negative analog power supply
GND = Pin 9 = Negative digital power supply

NOTE: Control inputs are referenced to GND. Analog inputs/outputs are referenced to V_{EE}. V_{EE} must be ≤ GND.

5

MOTOROLA

MC54/74HC4511

Advance Information

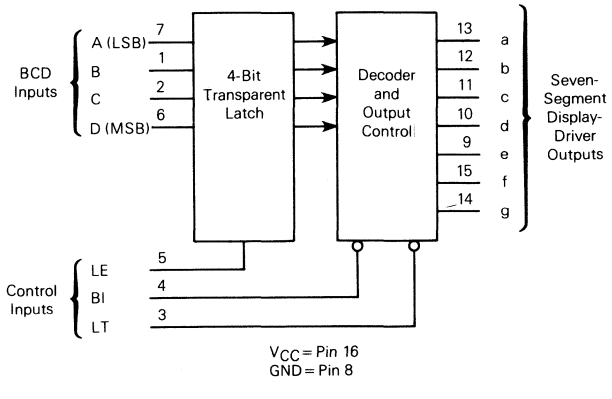
BCD-TO-SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER

The MC54/74HC4511 is identical in pinout to the MC14511 metal-gate CMOS decoder/driver. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC4511 provides the functions of a 4-bit storage latch, a BCD-to-seven-segment decoder, and a display driver. It can be used either directly or indirectly with seven-segment light-emitting diode (LED), incandescent, fluorescent, gas discharge, or liquid-crystal readouts. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn off or pulse modulate the brightness of the display, and to store a BCD code, respectively.

- Latch Storage of BCD Inputs
- Blanking Input
- Lamp Test Input
- Low Power Consumption Characteristic of CMOS Devices
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM

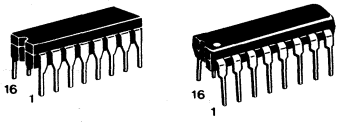


V_{CC} = Pin 16
GND = Pin 8

This document contains information on a new product. Specifications and information herein are subject to change without notice.

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

BCD-TO-SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER



J SUFFIX
CERAMIC PACKAGE
CASE 620

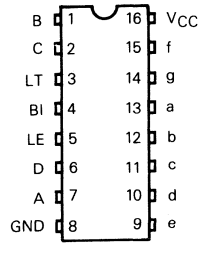
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

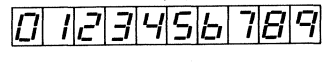
54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

PIN ASSIGNMENT



Display



5

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 3)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.999 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−6.0 mA I_{out}=−7.8 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

5

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A, B, C, or D to Output	55	100	ns
t_{PHL}	(Figures 1 and 6)	55	100	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Output	55	100	ns
t_{PHL}	(Figures 2 and 6)	55	100	
t_{PLH}	Maximum Propagation Delay, Blanking Input to Output	40	100	ns
t_{PHL}	(Figures 3 and 6)	40	100	
t_{PLH}	Maximum Propagation Delay, Lamp Test to Output	30	100	ns
t_{PHL}	(Figures 4 and 6)	30	100	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 6)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A, B, C, or D to Output (Figures 1 and 6)	2.0	300	600	756	894	ns
		4.5	60	120	151	179	
		6.0	51	102	129	152	
t_{PHL}		2.0	300	600	756	894	ns
		4.5	60	120	151	179	
		6.0	51	102	129	152	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Output (Figures 2 and 6)	2.0	300	600	756	894	ns
		4.5	60	120	151	179	
		6.0	51	102	129	152	
t_{PHL}		2.0	300	600	756	894	ns
		4.5	60	120	151	179	
		6.0	51	102	129	152	
t_{PLH}	Maximum Propagation Delay, Blanking Input to Output (Figures 3 and 6)	2.0	225	600	756	894	ns
		4.5	45	120	151	179	
		6.0	38	102	129	152	
t_{PHL}		2.0	225	600	756	894	ns
		4.5	45	120	151	179	
		6.0	38	102	129	152	
t_{PLH}	Maximum Propagation Delay, Lamp Test to Output (Figures 4 and 6)	2.0	175	600	756	894	ns
		4.5	35	120	151	179	
		6.0	30	102	129	152	
t_{PHL}		2.0	175	600	756	894	ns
		4.5	35	120	151	179	
		6.0	30	102	129	152	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 6)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*			–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, Input A, B, C, or D to Latch Enable (Figure 5)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Latch Enable to Input A, B, C, or D (Figure 5)	2.0	−20	0	0	0	ns
		4.5	−5	0	0	0	
		6.0	−3	0	0	0	
t_w	Minimum Pulse Width, Latch Enable (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 2)	–	1000	500	500	500	ns

SWITCHING WAVEFORMS

FIGURE 1

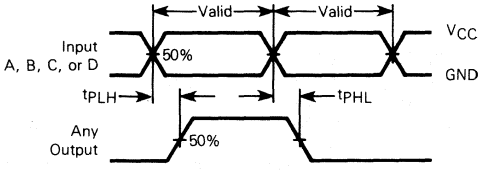


FIGURE 2

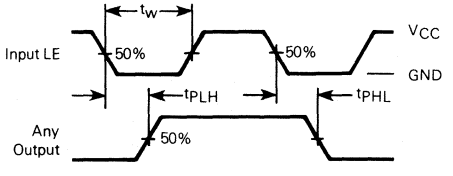


FIGURE 3

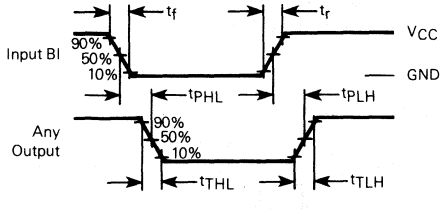


FIGURE 4

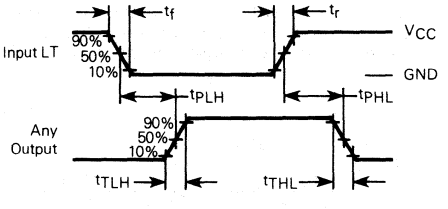


FIGURE 5

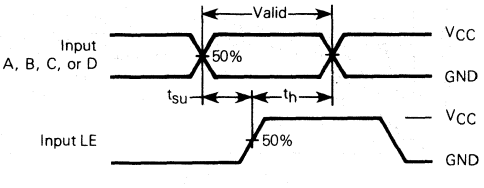
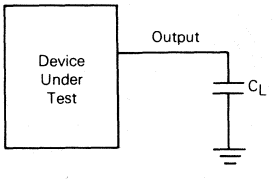


FIGURE 6 — TEST CIRCUIT



FUNCTION TABLE

Inputs							Outputs							
LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X	*							*

* = Depends upon the BCD code previously applied while LE was at a logic low.

INPUTS

A, B, C, D (Pins 7, 1, 2, 6) — BCD inputs. A (pin 7) is the least-significant bit and D (pin 6) is the most-significant bit. Hexadecimal code A-F at these inputs will cause the outputs to assume a logic low, offering an alternate method of blanking the display.

OUTPUTS

a, b, c, d, e, f, g (Pins 13, 12, 11, 10, 9, 15, 14) — Decoded, buffered seven-segment display-driver outputs. These outputs, unlike the MC14511, have CMOS drivers, which will produce typical CMOS output voltage levels. These outputs are connected to various displays as shown in Figure 7.

CONTROL INPUTS

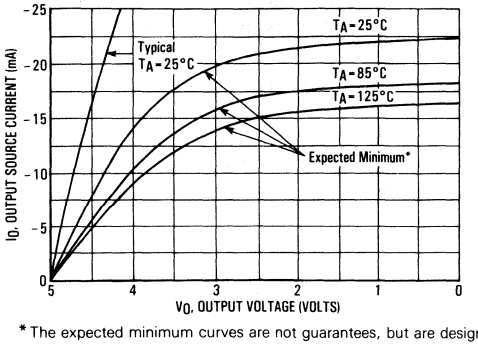
BI (Pin 4) — Active-low display blanking input. A logic low on this input will cause all outputs to be held at a logic low, thereby blanking the display. LT is the only input that will override the BI input.

LT (Pin 3) — Active-low lamp test. A low logic level on this input causes all outputs to assume a logic high. This input allows the user to test all segments of a display with a single control input. This input is independent of all other inputs.

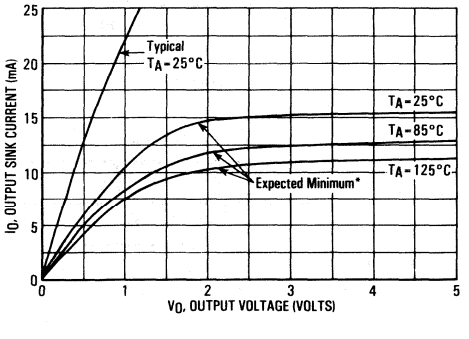
LE (Pin 5) — Latch enable input. This input controls the 4-bit transparent latch. A logic high on this input latches the code present at the A, B, C and D inputs; a logic low allows the code to be transmitted through the latch to the decoder.

OUTPUT CHARACTERISTIC CURVES (V_{CC} = 5 V)

SOURCE CURRENT



SINK CURRENT



* The expected minimum curves are not guarantees, but are design aids.

LOGIC DIAGRAM

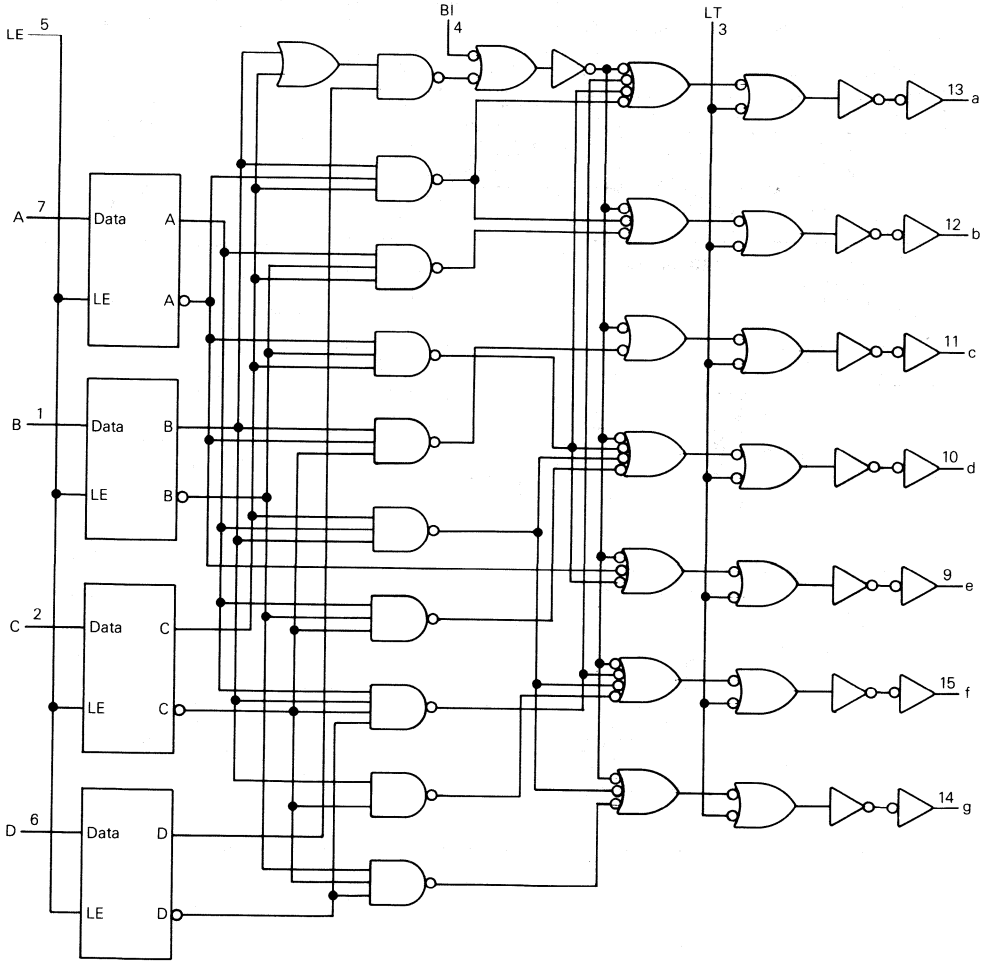
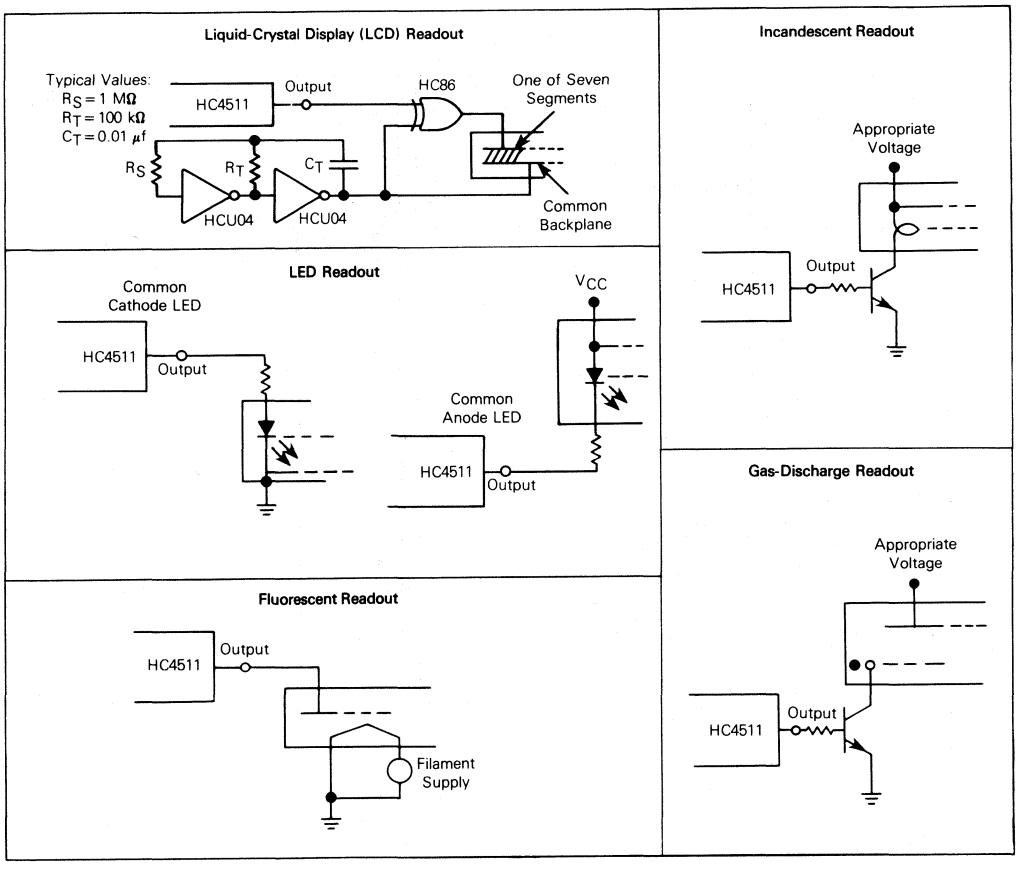


FIGURE 7 — CONNECTIONS TO VARIOUS DISPLAY READOUTS



5

MOTOROLA

MC54/74HC4514

Advance Information

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

The MC54/74HC4514 is identical in pinout to the MC14514B metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of a 4-bit storage latch with a Latch Enable and Chip-Select input. When a low signal is applied to the Latch Enable input, the Address is stored, and decoded. When the Chip-Select input is high, all sixteen outputs are forced to a low logic level.

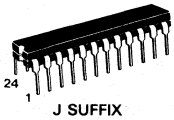
The Chip Select input is provided to facilitate the chip-select, demultiplexing, and cascading functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using the Chip Select as a data input.

- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

1-OF-16 DECODER/DEMULTIPLEXER WITH ADDRESS LATCH



J SUFFIX
CERAMIC PACKAGE
CASE 758

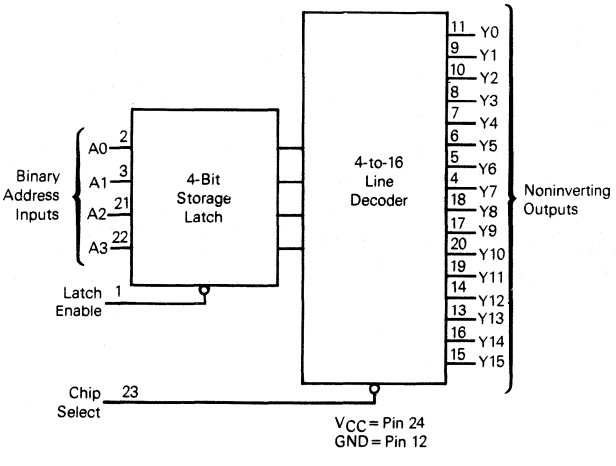
N SUFFIX
PLASTIC PACKAGE
CASE 724

ORDERING INFORMATION

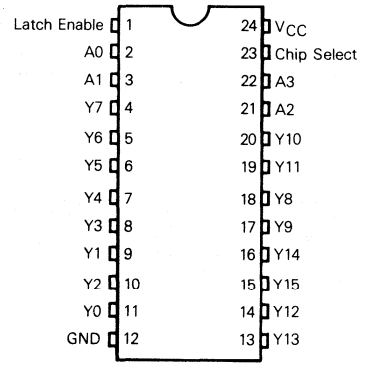
54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

5

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

5

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Chip Select to Output Y	18	30	ns
t_{PHL}	(Figures 1 and 5)	16	30	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y	24	40	ns
t_{PHL}	(Figures 2 and 5)	18	30	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Output Y	24	40	ns
t_{PHL}	(Figures 3 and 5)	18	30	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{PLH}	Maximum Propagation Delay, Chip Select to Output Y (Figures 1 and 5)	2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PHL}		2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 5)	2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{PHL}		2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Output Y (Figures 3 and 5)	2.0	115	230	290	343	ns
		4.5	23	46	58	69	
		6.0	20	39	49	58	
t_{PHL}		2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*			–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC	125°C 54HC	Unit
t_{su}	Minimum Setup Time, Input A to Latch Enable (Figure 4)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, Latch Enable to Input A (Figure 4)	2.0	– 10	5	5	5	
		4.5	0	5	5	5	
		6.0	1	5	5	5	
t_w	Minimum Pulse Width, Latch Enable (Figure 4)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

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SWITCHING WAVEFORMS

FIGURE 1

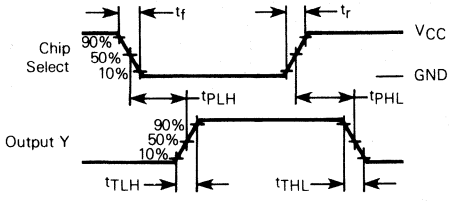


FIGURE 2

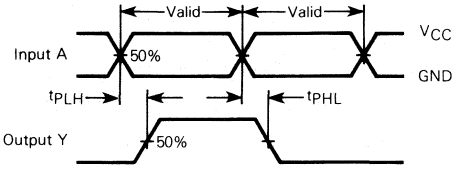


FIGURE 3

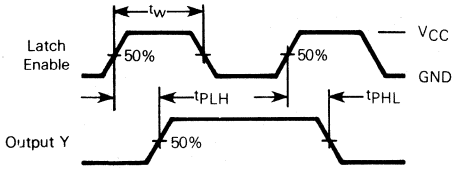


FIGURE 4

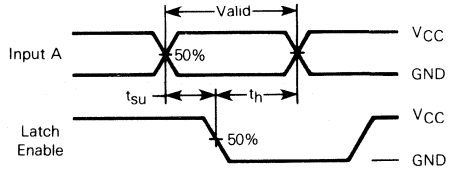
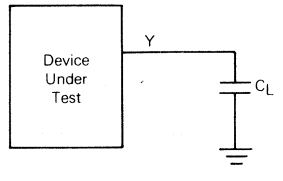


FIGURE 5



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FUNCTION TABLE

Latch Enable	Chip Select	Address Inputs				Selected Output (High)
		A3	A2	A1	A0	
H	L	L	L	L	L	Y0
H	L	L	L	L	H	Y1
H	L	L	L	H	L	Y2
H	L	L	L	H	H	Y3
H	L	L	H	L	L	Y4
H	L	L	H	L	H	Y5
H	L	L	H	H	L	Y6
H	L	L	H	H	H	Y7
H	L	H	L	L	L	Y8
H	L	H	L	L	H	Y9
H	L	H	L	H	L	Y10
H	L	H	L	H	H	Y11
H	L	H	H	L	L	Y12
H	L	H	H	L	H	Y13
H	L	H	H	H	L	Y14
H	L	H	H	H	H	Y15
X	H	X	X	X	X	All Outputs = L
L	L	X	X	X	X	Latched Data

PIN DESCRIPTIONS

INPUTS

A0, A1, A2, A3, (PINS 2, 3, 21, 22) — Address Inputs. These inputs are decoded to produce a high logic level on one of 16 outputs. The inputs are arranged such that A3 is the most-significant bit and A0 is the least-significant bit. The decimal equivalent of the binary input address indicates which of the 16 data outputs, Y0-Y15, will be selected.

OUTPUTS

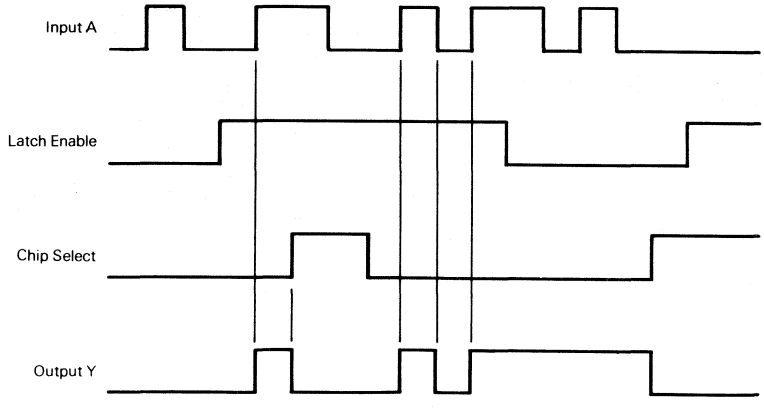
Y0-Y15 — Active High Outputs. These outputs produce a high logic level when selected (Latch Enable = H, Chip Select = L) and are at a low logic level when not selected.

CONTROLS

LATCH ENABLE (PIN 1) — Latch Enable Input. A low logic level on this input stores the data on the Address data inputs in the 4-bit latch. A high logic level on the Latch Enable input makes the latch transparent and allows the outputs to follow the inputs. Note that the data is latched only while the Latch Enable input is at a low logic level.

CHIP SELECT (PIN 23) — Chip-Select Input. A logic high on this input produces a low logic level on all outputs, regardless of what appears at the address or Latch Enable inputs. A low logic level on the Chip Select input allows the selected output to produce a high logic level.

TIMING DIAGRAM



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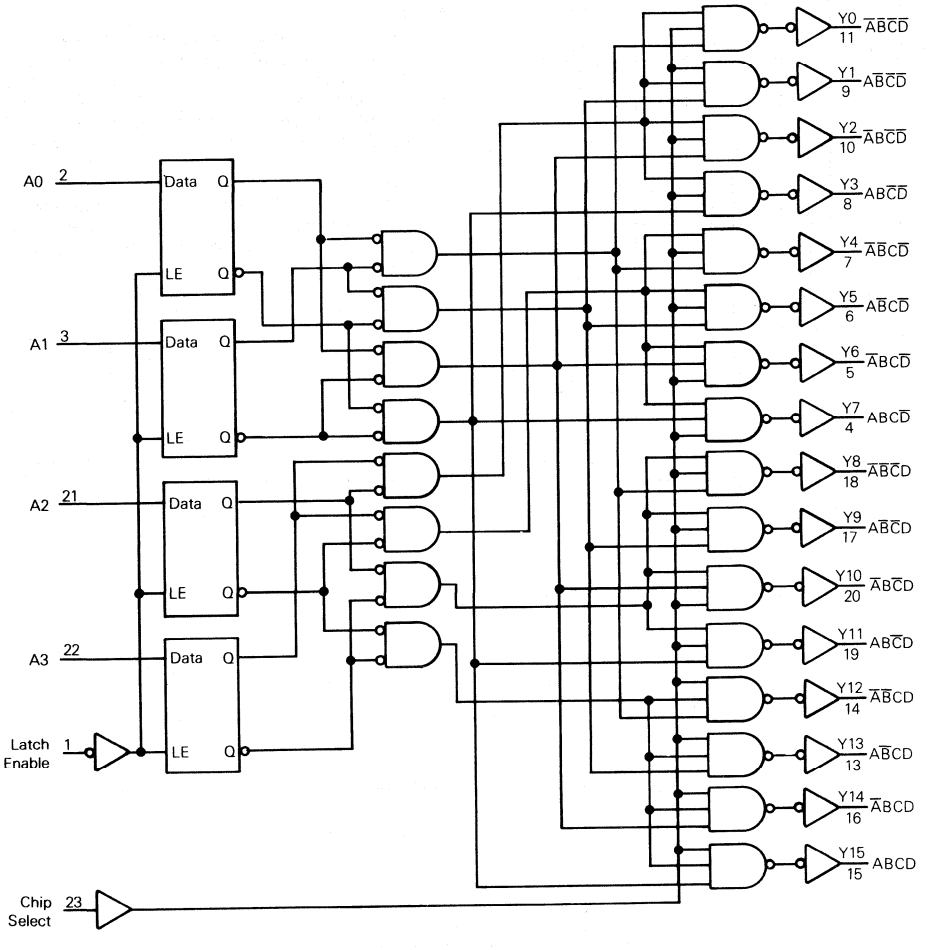
LOGIC DIAGRAM



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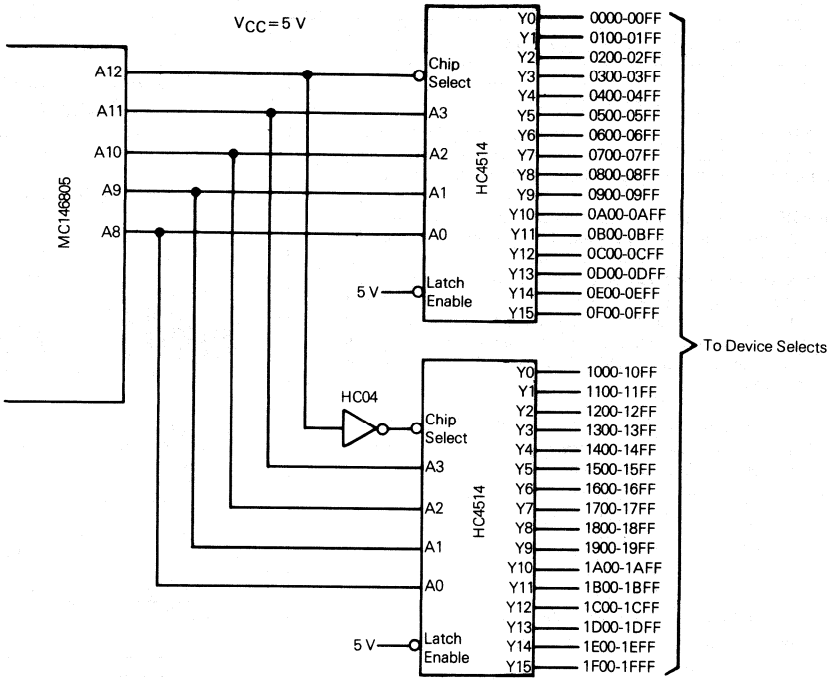
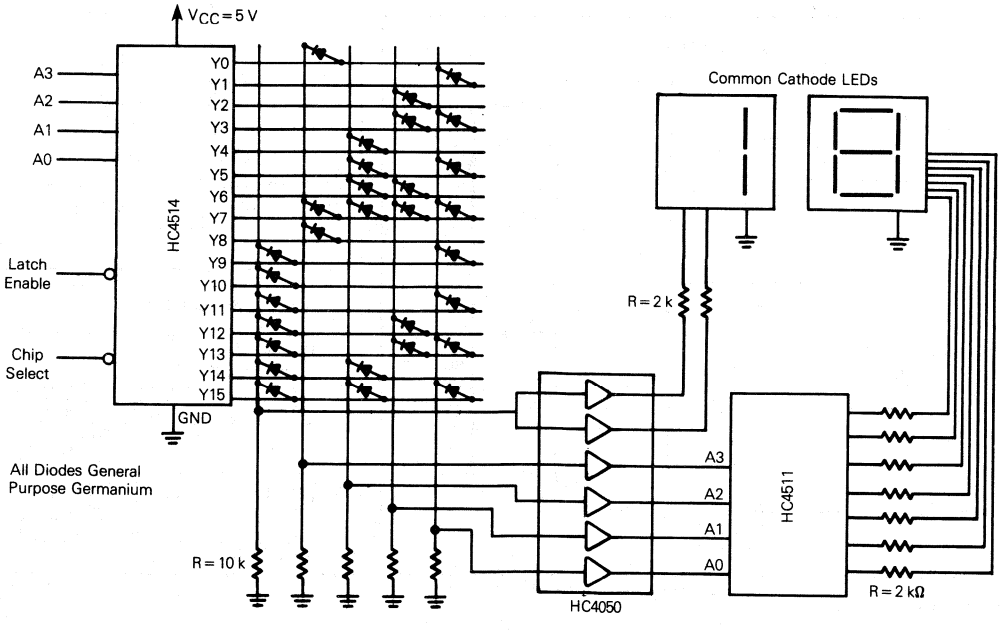
MICROPROCESSOR MEMORY DECODING



CODE TO CODE CONVERSION — HEXADECIMAL TO BCD



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MOTOROLA

MC54/74HC4518

Product Preview

DUAL BCD COUNTER

The MC54/74HC4518 is identical in pinout to the MC14518 metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC4518 consists of two independent, synchronous 4-stage counters. The counter stages are D-type flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be Reset by applying a high level on the Reset line. The HC4518 will count out of all undefined states within two clock periods. These up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition on Enable
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

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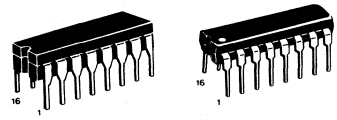
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

DUAL BCD COUNTER



J SUFFIX
CERAMIC PACKAGE
CASE 620

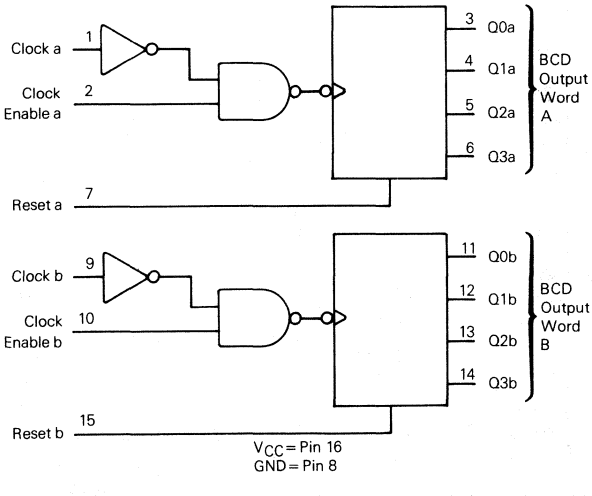
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

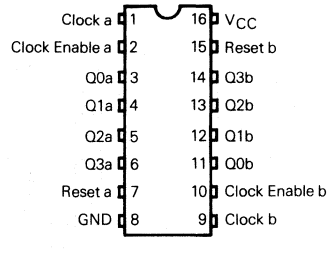
54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Clock	Clock Enable	Reset	Operation
↑	H	L	Increment Counter
L	↓	L	Increment Counter
↓	X	L	No Change
X	↑	L	No Change
↑	L	L	No Change
H	↓	L	No Change
X	X	H	Q0 thru Q3 = L

X = Don't Care

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MOTOROLA

MC54/74HC4520

Product Preview

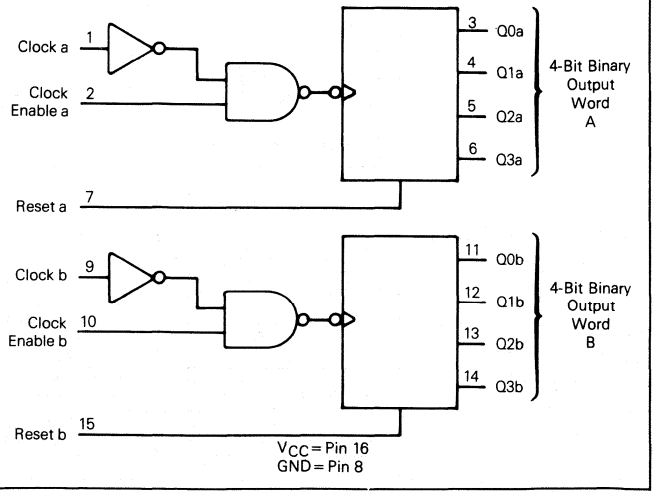
DUAL 4-BIT BINARY COUNTER

The MC54/74HC4520 is identical in pinout to the MC14520 metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC4520 consists of two independent, synchronous 4-stage counters. The counter stages are D-type flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be Reset by applying a high level on the Reset line. These up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design — Incremented on Positive Transition of Clock or Negative Transition on Enable
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM



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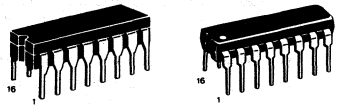
DUAL 4-BIT BINARY COUNTER



J SUFFIX
CERAMIC PACKAGE
CASE 620

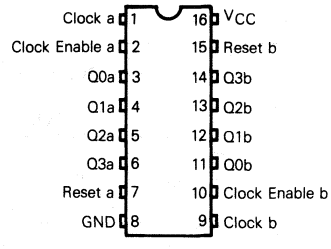
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Clock	Clock Enable	Reset	Operation
↑	H	L	Increment Counter
L	↓	L	Increment Counter
↓	X	L	No Change
X	↑	L	No Change
↑	L	L	No Change
H	↓	L	No Change
X	X	H	Q0 thru Q3 = L

X = Don't Care

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MOTOROLA

MC54/74HC4538

Advance Information

DUAL PRECISION MONOSTABLE MULTIVIBRATOR (RETRIGGERABLE, RESETTABLE)

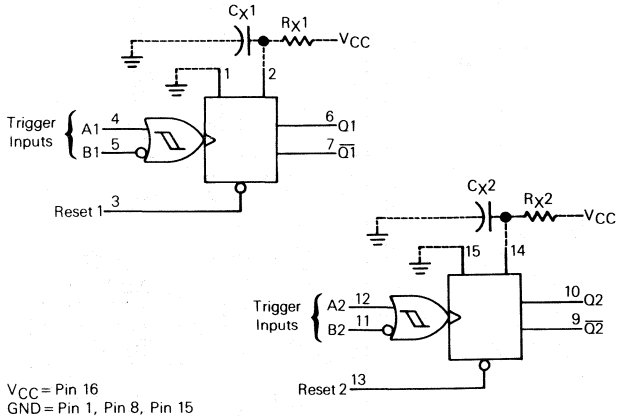
The MC54/74HC4538 is identical in pinout to the MC14538B and the MC14528B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This dual monostable multivibrator may be triggered by either the positive or the negative edge of an input pulse, and will produce a precision output pulse over a wide range of pulse widths. Because the device has conditioned trigger inputs, there are no trigger-input rise and fall time restrictions. The output pulse width is determined by the external timing components, R_X and C_X. The device has a reset function which forces the Q output low, regardless of the state of the output pulse circuitry.

The HC4538 is similar in function to the HC123, HC221, and HC423; however, the HC4538 is designed to have a more accurate pulse width.

- Unlimited Rise and Fall Times Allowed on the Trigger Inputs
- Output Pulse Width Is Independent of the Trigger Pulse Width
- ±7% Guaranteed Pulse Width Variation from Part to Part at 5 V, 25°C
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 220 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 1, Pin 8, Pin 15
R_X and C_X are external components

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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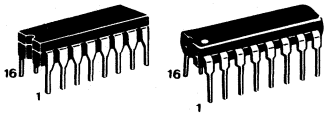
DUAL PRECISION MONOSTABLE MULTIVIBRATOR (RETRIGGERABLE, RESETTABLE)



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CERAMIC PACKAGE
CASE 620

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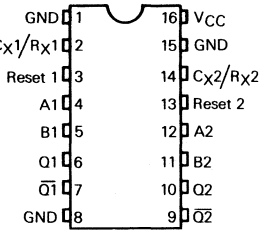
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs	
Reset	A	B	Q	$\overline{Q}$
H	↓	H	⊓	⊔
H	L	↑	⊓	⊔
H	X	L	Not Triggered	
H	H	X	Not Triggered	
H	L, H, ↑	H	Not Triggered	
H	L	L, H, ↓	Not Triggered	
L	X	X	L	H
↑, ↓	X	X	Not Triggered	

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin-A, B, Reset	±20	mA
I_{in}	DC Input Current, per Pin-C_X/R_X	±30	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \leq (V_{in}$ or $V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time-Reset (Figure 8)	—	500	ns
t_r, t_f	Input Rise and Fall Time-A or B (Figure 8)	—	no limit	ns
R_X	External Timing Resistor	1.0	*	kΩ
C_X	External Timing Capacitor	0	*	μF

*The maximum allowable values of R_X and C_X are a function of the leakage of capacitor C_X, the leakage of the HC4538, and leakage due to board layout and surface resistance. Values of R_X and C_X should be chosen so that the maximum current into pin 2 or pin 14 is 30 mA. Susceptibility to externally induced noise signals may occur for $R_X > 1$ MΩ.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current (A, B, Reset)	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{in}	Maximum Input Leakage Current (C_X/R_X)	V_{in}=V_{CC} or GND	6.0		±50	±500	±500	nA
I_{CC}	Maximum Quiescent Supply Current (Per Package) Standby State	V_{in}=V_{CC} or GND Q1 and Q2=Low I_{out}=0 μA	6.0	65	130	220	350	μA
I_{CC}	Maximum Supply Current (Per Package) Active State	V_{in}=V_{CC} or GND Q1 and Q2=High Pins 2 and 14=0.5 V_{CC}	6.0	90	130	220	350	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Q (Figures 7 and 9)	23	45	ns
t_{PHL}	Maximum Propagation Delay, Input A or B to $\overline{Q}$ (Figures 7 and 9)	26	50	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 8 and 9)	23	45	ns
t_{PLH}	Maximum Propagation Delay, Reset to $\overline{Q}$ (Figures 8 and 9)	26	50	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 8 and 9)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A or B to Q (Figures 7 and 9)	2.0 4.5 6.0	125 25 21	250 50 43	315 63 54	373 75 63	ns
t_{PHL}	Maximum Propagation Delay, Input A or B to $\overline{Q}$ (Figures 7 and 9)	2.0 4.5 6.0	138 28 23	275 55 47	347 69 59	410 82 70	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 8 and 9)	2.0 4.5 6.0	125 25 21	250 50 43	315 63 54	373 75 63	ns
t_{PLH}	Maximum Propagation Delay, Reset to $\overline{Q}$ (Figures 8 and 9)	2.0 4.5 6.0	138 28 23	275 55 47	347 69 59	410 82 70	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 8 and 9)	2.0 4.5 6.0	38 8 6	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance (A, B, Reset)		5	10	10	10	pF
C_{in}	Maximum Input Capacitance (C_X/R_X)		25	–	–	–	pF
C_{PD}	Power Dissipation Capacitance*		150	–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For system power consumption calculations, the power required to change the external timing capacitor should also be taken into consideration.

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TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{rr}	Minimum Retrigger Time, Input A or B (Figure 8)	2.0 4.5 6.0	* * *				ns
t_{rec}	Minimum Recovery Time, Reset Inactive to A or B (Figure 8)	2.0 4.5 6.0					ns
t_w	Minimum Pulse Width, Input A or B (Figure 7)	2.0 4.5 6.0	40 8 7	80 16 14	101 20 17	119 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 8)	2.0 4.5 6.0	40 8 7	80 16 14	101 20 17	119 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times, Reset (Figure 8)	–	1000	500	500	500	ns
t_r, t_f	Maximum Input Rise and Fall Times, A or B (Figure 8)	–	No Limit				ns

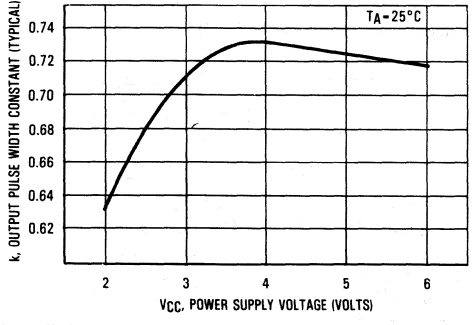
$$* t_{rr}(ns) \approx 72 + \left(\frac{V_{CC}\ (volts) \bullet C_X(pF)}{30.5} \right)$$

OUTPUT PULSE WIDTH CHARACTERISTICS (C_L = 15 pF, T_A = 25°C)

Symbol	Parameter	Conditions: Timing Components	Conditions: V_{CC}	Min	Typ	Max	Unit
τ	Output Pulse Width* (Figures 7 and 9)	R_X = 1 kΩ, C_X = 12 pF	3	190	283	400	ns
			5	120	147	185	
		R_X = 10 kΩ, C_X = 100 pF	3		1.2		μs
			5		1.0		
		R_X = 10 kΩ, C_X = 1000 pF	3	9.4	10.5	11.6	μs
			5	9.3	10.0	10.7	
–	Pulse Width Match Between Circuits in the Same Package	–			±1		%

* For output pulse widths greater than 100 μs, $\tau = kR_XC_X$, where the value of k may be found on Figure 1.

FIGURE 1 – OUTPUT PULSE WIDTH CONSTANT, k, versus SUPPLY VOLTAGE
(For output pulse widths ≥ 100 μs: $\tau = kR_XC_X$)



PIN DESCRIPTIONS

INPUTS

A1, A2 (PINS 4, 12) – Positive-edge trigger inputs. A rising-edge signal on either of these pins will trigger the corresponding multivibrator when there is a high voltage level on the B1 or B2 input.

B1, B2 (PINS 5, 11) – Negative-edge trigger inputs. A falling-edge signal on either of these pins will trigger the corresponding multivibrator when there is a low voltage level on the A1 or A2 input.

RESET 1, RESET 2 (PINS 3, 13) – Reset inputs (active low). When a low voltage is applied to one of these pins, the Q output of the corresponding multivibrator is reset to a low voltage and the $\overline{Q}$ output is set to a high voltage.

C_X1/R_X1 and C_X2/R_X2 (PINS 2 and 14) – External timing components. These pins are tied to the common points of the external timing resistors and capacitors (see the Block Diagram).

GND (PINS 1 and 15) – External ground. The external timing capacitors discharge to ground through these pins.

OUTPUTS

Q1, Q2 (PINS 6, 10) – Noninverted monostable outputs. These pins (normally low) pulse high when the multivibrator is triggered at either the A or the B input. The width of the pulse is determined by the external timing components, R_X and C_X.

$\overline{Q1}$, $\overline{Q2}$ (PINS 7, 9) – Inverted monostable outputs. These pins (normally high) pulse low when the multivibrator is triggered at either the A or the B input. These outputs are the inverse of Q1 and Q2.

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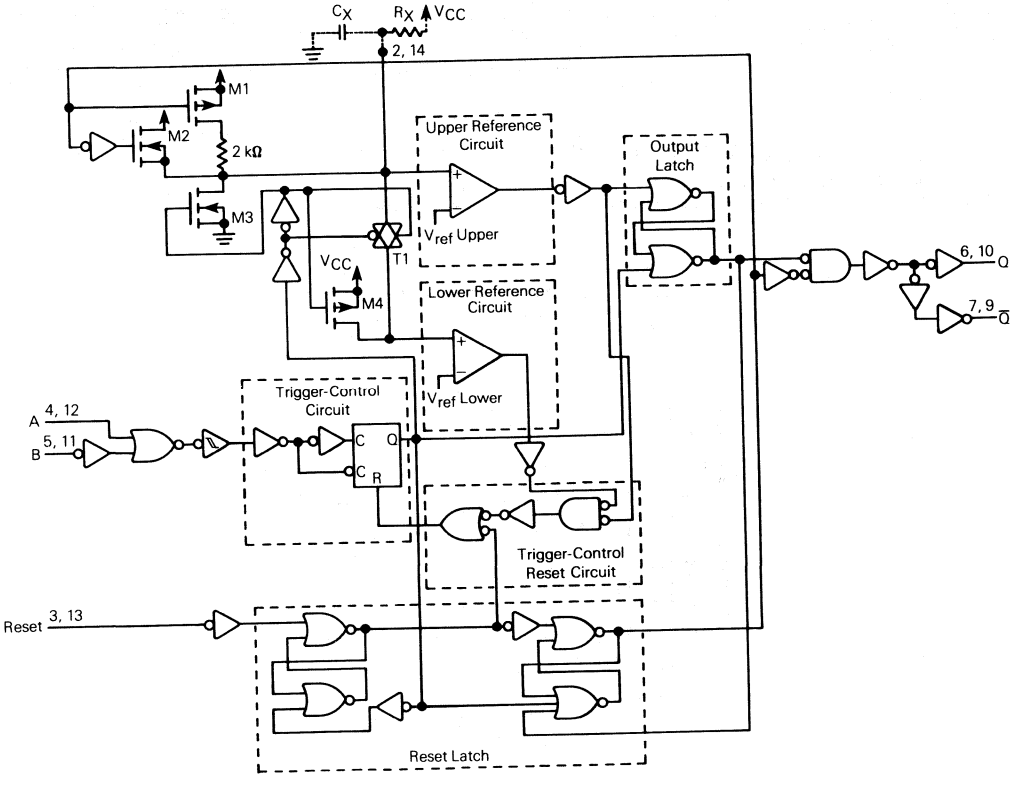
FIGURE 2 — FUNCTION DIAGRAM
(½ the device)



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CIRCUIT OPERATION

Figure 5 shows the HC4538 configured in the retriggerable mode. Briefly, the device operates as follows (refer to Figure 1): In the quiescent state, the external timing capacitor, C_X, is charged to V_{CC}. When a trigger occurs, the Q output goes high and C_X discharges quickly to the lower reference voltage (V_{ref} Lower ≈ 1/3 V_{CC}). C_X then charges, through R_X, back up to the upper reference voltage (V_{ref} Upper ≈ 2/3 V_{CC}), at which point the one-shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the function diagram (Figure 2) and the timing diagram (Figure 3).

QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in Figure 3). Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, Figure 3).

The output of the trigger-control circuit is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor, C_X, is charged to V_{CC} (#4), and the upper reference circuit has a low output (#5). Transistor M4 is turned on and transmission gate T1 is turned off. Thus the lower reference circuit has V_{CC} at the noninverting input and a resulting low output (#6).

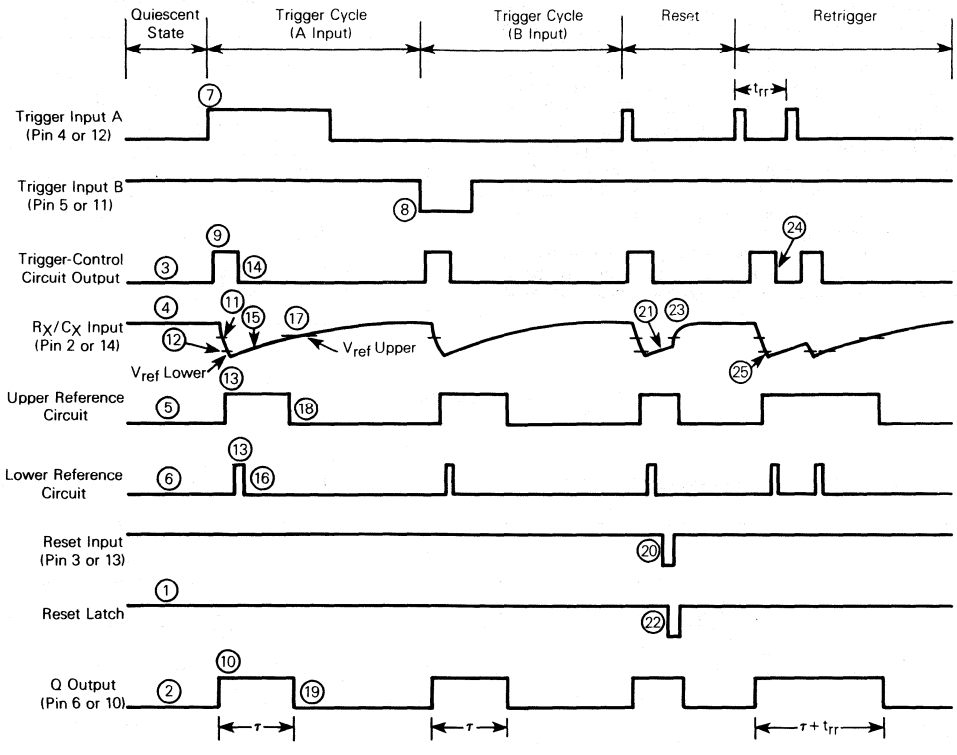
In addition, the output of the trigger-control reset circuit is low.

TRIGGER OPERATION

The HC4538 is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

The trigger-control circuit going high simultaneously initiates three events. First, the output latch goes low, thus

FIGURE 3 — TIMING DIAGRAM



taking the Q output of the HC4538 to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, C_X, to rapidly discharge toward ground (#11). (Note that the voltage across C_X appears at the input of the upper reference circuit comparator). Third, transistor M4 is turned off and transmission gate T1 is turned on, thus allowing the voltage across C_X to also appear at the input of the lower reference circuit comparator.

When C_X discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flip-flop to a low state (#14). This turns transistor M3 off again, allowing C_X to begin to charge back up toward V_{CC}, with a time constant $t = R_X C_X$ (#15). In addition, transistor M4 is turned on and transmission gate T1 is turned off. Thus a high voltage level is applied to the input of the lower reference circuit comparator, causing its output to go low (#16). The monostable multivibrator may be retriggered at any time after the trigger-control circuit goes low.

When C_X charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the HC4538 to a low state (#19), and completing the time-out cycle.

RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the HC4538 to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while C_X is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus C_X is allowed to quickly charge up to V_{CC} (#23) to await the next trigger signal.

RETRIGGER OPERATION

When used in the retriggerable mode (Figure 5), the HC4538 may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24). Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit (#25), the minimum retrigger time, t_{rr} (Figure 8) is a function of internal propagation delays and the discharge time of C_X:

$$t_{rr}(ns) \cong 72 + \frac{V_{CC}(volts) \bullet C_X(pF)}{30.5}, \text{ at room temperature}$$

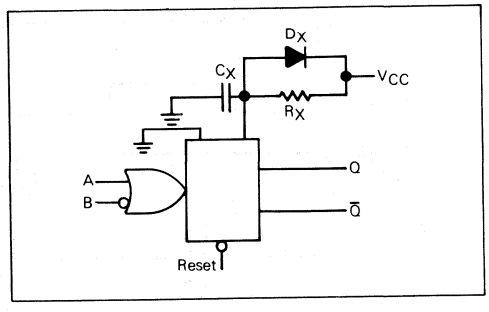
Figure 6 shows the device configured in the non-retriggerable mode.

POWER-DOWN CONSIDERATIONS

Large values of C_X may cause problems when powering down the HC4538 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{CC} through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \bullet C_X / (30\ mA)$. For example, if $V_{CC} = 5$ V and $C_X = 15\ \mu F$, the V_{CC} supply must turn off no faster than $t = (5\ V) \bullet (15\ \mu F)/30\ mA = 2.5$ ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{CC} to zero volts occurs, the HC4538 may sustain damage. To avoid this possibility, use an external clamping diode, D_X, connected as shown in Figure 4.

FIGURE 4 — LATCH-UP PROTECTION DURING POWER DOWN



TYPICAL APPLICATIONS

FIGURE 5 — RETRIGGERABLE MONOSTABLE CIRCUITRY

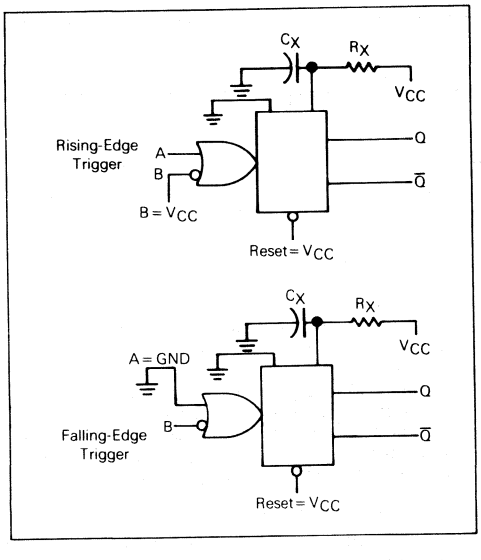
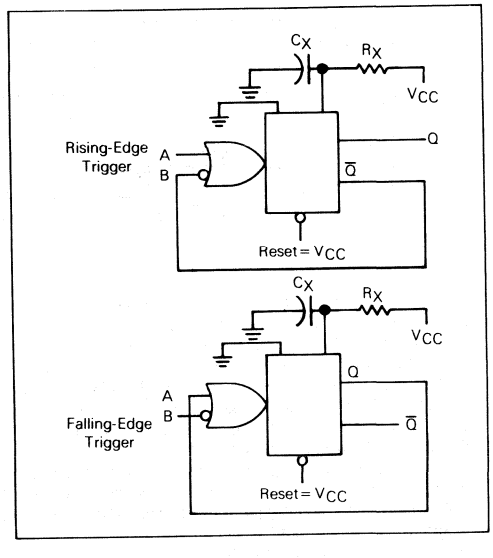


FIGURE 6 — NONRETRIGGERABLE MONOSTABLE CIRCUITRY



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SWITCHING WAVEFORMS

FIGURE 7

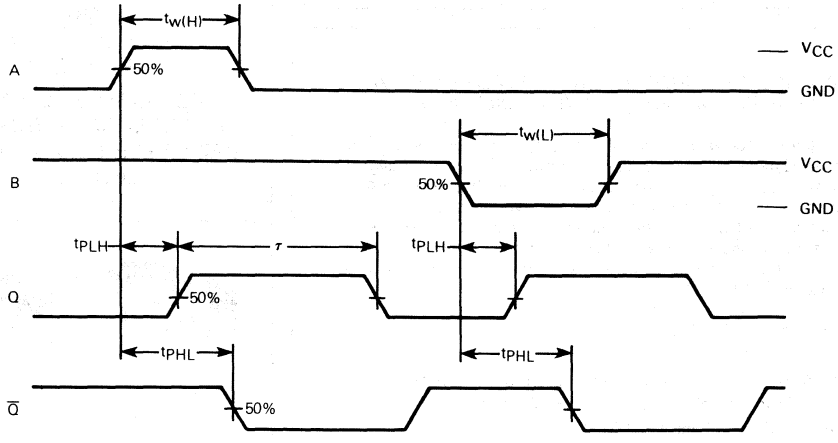


FIGURE 8

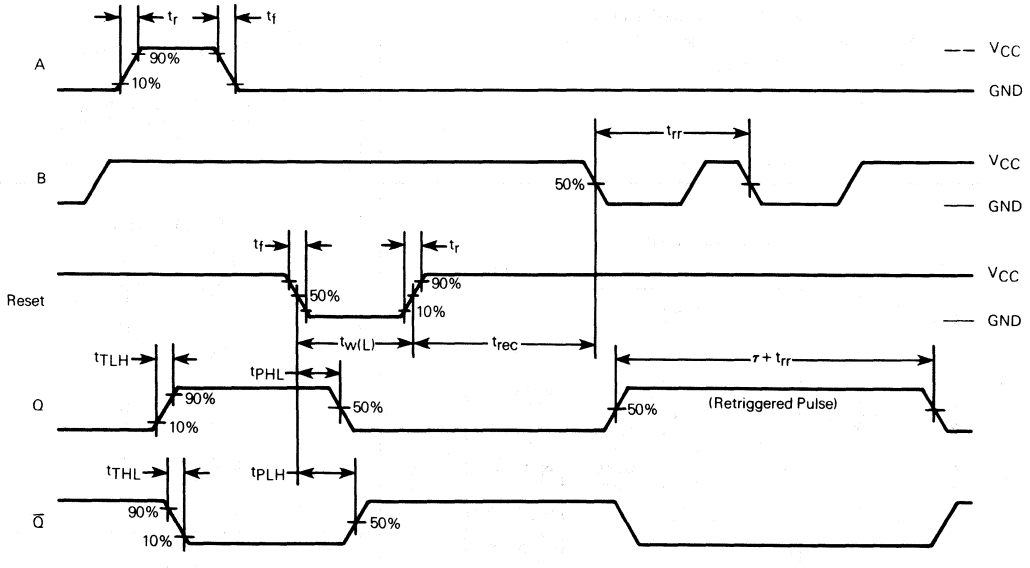
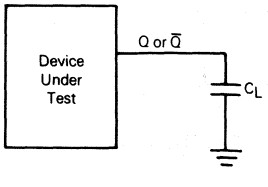


FIGURE 9 — TEST CIRCUIT



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MOTOROLA

MC54/74HC4543

Advance Information

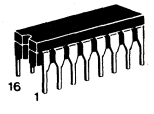
BCD-TO-SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER FOR LIQUID-CRYSTAL DISPLAYS

The MC54/74HC4543 is compatible in both function and pinout with the MC14543 metal-gate CMOS decoder/driver. This device is designed for use with liquid-crystal display (LCD) readouts. It provides a 4-bit storage latch, a BCD-to-seven segment decoder, and an LCD driver. The blanking input (BI) and latch enable (LE, active low) are used to blank the display and store the BCD code, respectively. A square wave is applied to the phase (Ph) input of the HC4543 and electrically common backplane of the LCD.

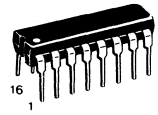
- Latch Storage of BCD Inputs
- Blanking Input
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 1 LSTTL Load Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

BCD-TO-SEVEN-SEGMENT LATCH/DECODER/DISPLAY DRIVER FOR LIQUID-CRYSTAL DISPLAYS



J SUFFIX
CERAMIC PACKAGE
CASE 620



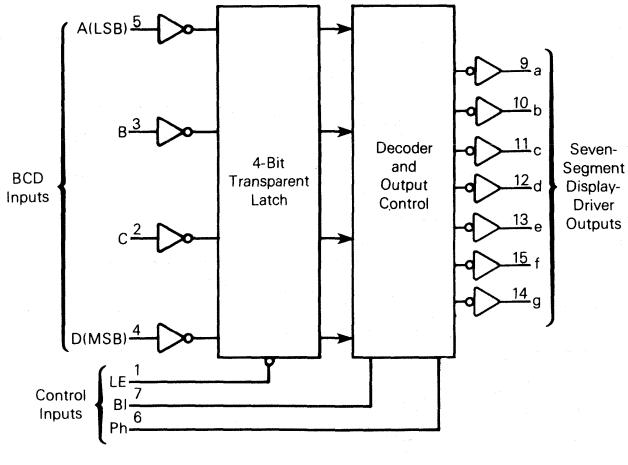
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

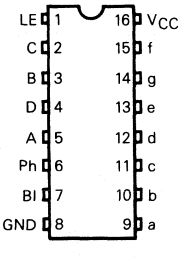
54 Series: −55°C to +125°C
MC54HCXXXXJ (Ceramic Package Only)

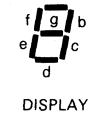
74 Series: −40°C to +85°C
MC74HCXXXXN (Plastic Package)
MC74HCXXXXJ (Ceramic Package)

BLOCK DIAGRAM

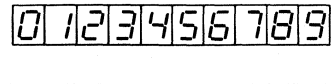


PIN ASSIGNMENT





DISPLAY



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 3)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed			
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.98 4.49 5.99	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−0.4 mA I_{out}=−0.5 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.02 0.01 0.01	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=0.4 mA I_{out}=0.5 mA	4.5 6.0	0.20 0.20	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A, B, C, or D to Output	45	100	ns
t_{PHL}	(Figures 1 and 5)	45	100	
t_{PLH}	Maximum Propagation Delay, LE to Output	45	100	ns
t_{PHL}	(Figures 2 and 5)	45	100	
t_{PLH}	Maximum Propagation Delay, BI or Ph to Output	27	100	ns
t_{PHL}	(Figures 3 and 5)	27	100	
t_{TLH},	Maximum Output Transition Time, Any Output	25	50	ns
t_{THL}	(Figures 3 and 5)			

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	25°C 54HC and 74HC Guaranteed Limit	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
t_{PLH}	Maximum Propagation Delay, Input A, B, C, or D to Output (Figures 1 and 5)	2.0	300	600	756	894	ns
		4.5	60	120	151	179	
		6.0	51	102	129	152	
t_{PHL}		2.0	300	600	756	894	ns
		4.5	60	120	151	179	
		6.0	51	102	129	152	
t_{PLH}	Maximum Propagation Delay, LE to Output (Figures 2 and 5)	2.0	300	600	756	894	ns
		4.5	60	120	151	179	
		6.0	51	102	129	152	
t_{PHL}		2.0	300	600	756	894	ns
		4.5	60	120	151	179	
		6.0	51	102	129	152	
t_{PLH}	Maximum Propagation Delay, BI or Ph to Output (Figures 3 and 5)	2.0	175	600	756	894	ns
		4.5	35	120	151	179	
		6.0	30	102	129	152	
t_{PHL}		2.0	175	600	756	894	ns
		4.5	35	120	151	179	
		6.0	30	102	129	152	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 5)	2.0	300	600	756	894	
		4.5	60	120	151	179	
		6.0	51	102	129	152	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*			–	–	–	pF

*C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

5

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
			Typical	Guaranteed Limit			
t_{su}	Minimum Setup Time, Input A, B, C, or D to LE (Figure 4)	2.0	50	100	126	149	ns
		4.5	10	20	25	30	
		6.0	9	17	21	25	
t_h	Minimum Hold Time, LE to Input A, B, C, or D (Figure 4)	2.0	25	50	63	75	ns
		4.5	5	10	13	15	
		6.0	4	9	11	13	
t_w	Minimum Pulse Width, LE (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)		1000	500	500	500	ns

SWITCHING WAVEFORMS

FIGURE 1

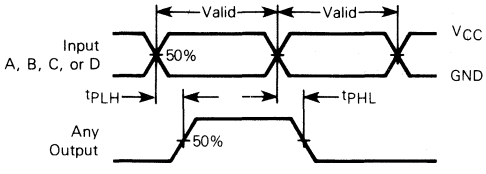


FIGURE 2

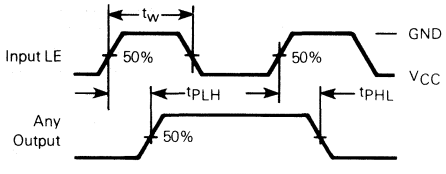


FIGURE 3

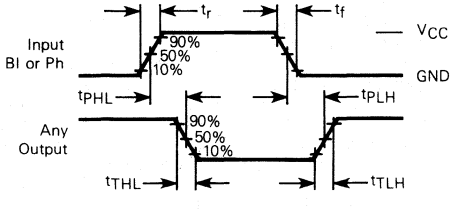


FIGURE 4

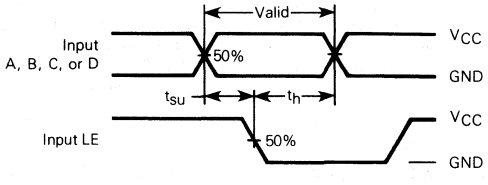
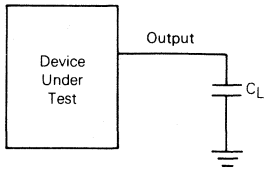


FIGURE 5 — TEST CIRCUIT



FUNCTION TABLE

Inputs							Outputs							
LE	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X	••							••
†	†	H	†				Inverse of Output Combinations Above							Display as above

X = Don't care

† = Above Combinations

* = For liquid crystal readouts, apply a square wave to Ph.

** = Depends upon the code previously applied when LE = H

PIN DESCRIPTIONS

INPUTS

A, B, C, D (Pins 5, 3, 2, 4) — BCD inputs. These are the inputs to be decoded. The data on these pins is decoded to a seven-segment output when the LE pin is high and is latched when LE is low. For inputs greater than hexadecimal 9 or for BI input high, the output is blanked. A (pin 5) is the least-significant data bit and D (pin 4) is the most-significant data bit.

OUTPUTS

a, b, c, d, e, f, g (Pins 9, 10, 11, 12, 13, 15, 14) — Decoded seven-segment display-driver outputs. For liquid-crystal displays (LCD's), these outputs are tied directly to the LCD segment pins. For other type displays, see Figure 6.

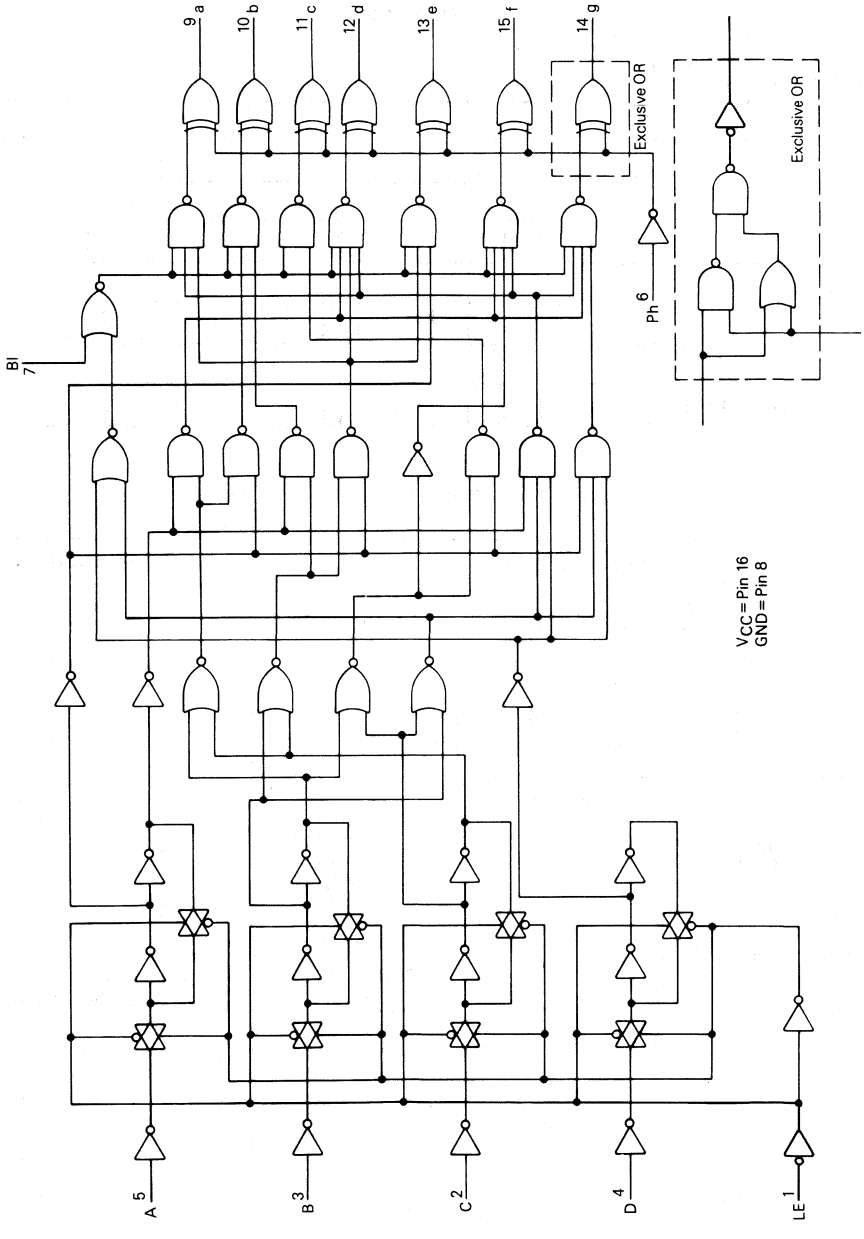
CONTROL INPUTS

LE (Pin 1) — Latch Enable input (active low). A falling-edge signal on this pin latches the code on the A, B, C, and D pins. The code remains latched until a rising-edge signal is applied to this pin. A high logic level on this pin allows the code to be transferred thru the latch to the decoder.

Ph (Pin 6) — Phase input. This input is used to invert the output logic level. For liquid-crystal displays (LCD), a square wave is applied to this input (typically 100Hz) and to the common backplane of the LCD. For light-emitting diode (LED), incandescent, or gas-discharge displays, the phase input is tied to the appropriate level as shown in Figure 6.

BI (Pin 7) — Blanking input pin. A high level on this pin causes the outputs to follow the phase input, thereby blanking the display (no voltage drop across LCD segments).

LOGIC DIAGRAM



TIMING DIAGRAM

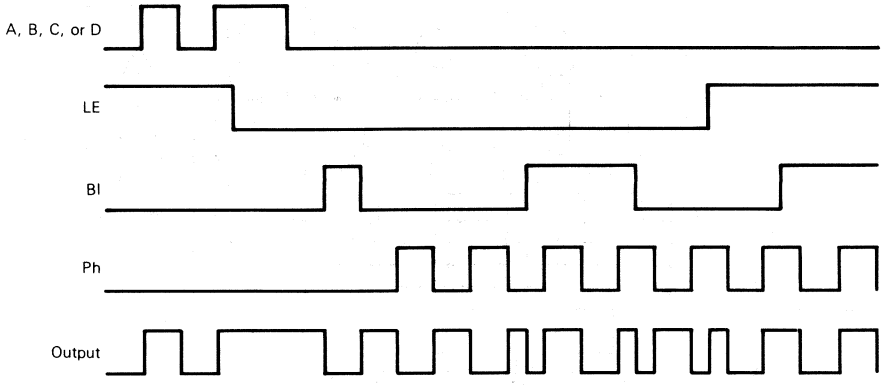
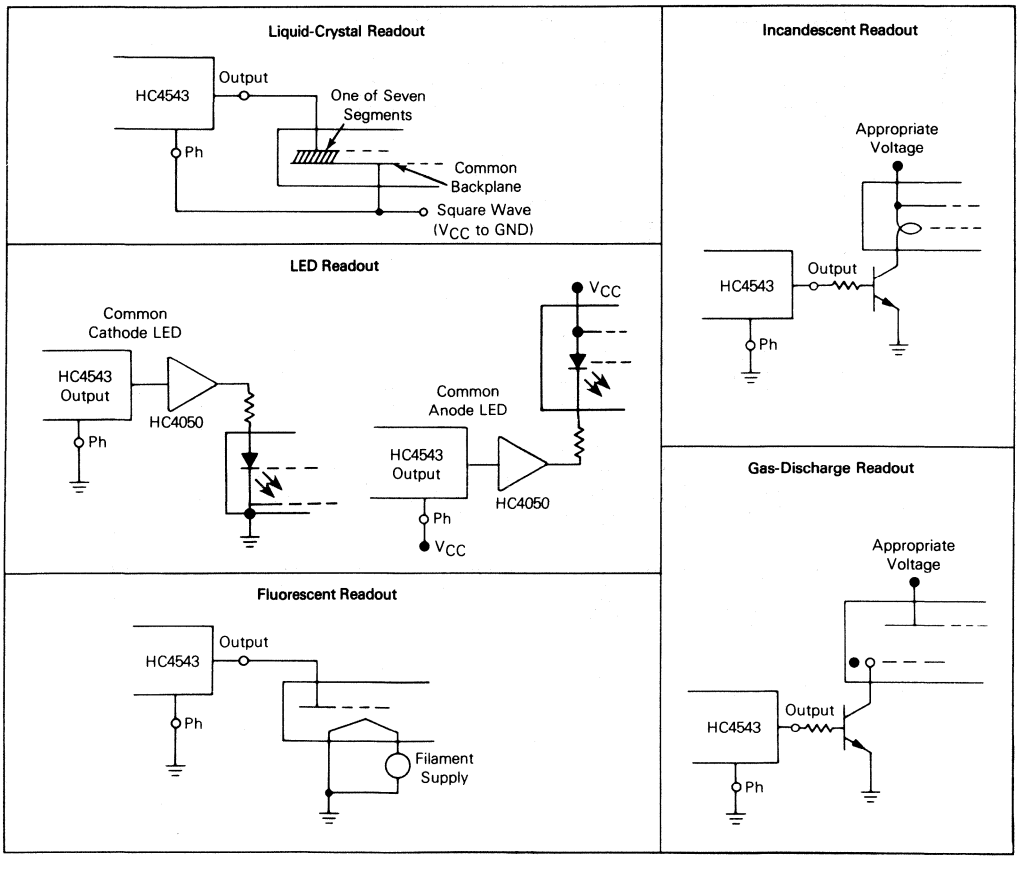


FIGURE 6 — CONNECTIONS TO VARIOUS DISPLAY READOUTS



5

Reliability

6

INTRODUCTION

Motorola has conducted a comprehensive reliability study of the High-Speed CMOS logic family to evaluate new devices and processes and to assess current performance levels. The 1982 High-Speed CMOS data base consists of results obtained from 6,796 devices representing 21 device types. The data presented here show that the manufacturing technique used in the production of this family, from superior designs, through the Silicon-Gate die fabrication process, and through assembly and testing, provides devices which equal or exceed standard Metal-Gate CMOS reliability.

Tests conducted in the evaluation include accelerated life, temperature humidity bias, autoclave, temperature cycle, thermal shock and mechanical series. The grouping of test results is consistent with the proposed JEDEC JC 40.2 device classifications for I_{CC} (quiescent current) limits. Since I_{CC} closely correlates with device complexity, this provides a logical, consistent, and unambiguous format for grouping of reliability data. This classification system includes SSI, Flip-Flops and Latches, and MSI. In addition, those devices in the MSI group which have the added advantage of bus drive capability are presented separately, since some customers will prefer these data separate. Thus, reliability data for the MSI category of device types also include the MSI Bus Compatible devices. Future reports will also follow this format.

ACCELERATED LIFE TEST

Accelerated life testing is used to simulate long-term operation and to gather data for failure rate predictions. The test is conducted at an ambient temperature of 125°C with devices biased at the nominal operating voltage of 5 volts. A complete functional and parametric test to data sheet specifications is performed at 0, 48, 168, 504, and 1008 hours. Devices which fail to meet all electrical specifications at each readout are removed from the test, datalogged to identify failure modes, and, when required, analyzed to determine the physical failure mechanisms.

Life testing was performed on both plastic and CERDIP package types. The twenty-eight lots which were included in the life test study are listed in Table 1 by device type and the quantity of each tested. A complete summary of acceierated life test data is presented in Tables 2 and 3.

Table 1.
Device Types Used In 125°C Accelerated Life Test

Device Classification	Plastic Device Type	Quantity	Ceramic Device Type	Quantity
SSI	MC74HC00N	300	MC54HC00J	365
	MC74HC02N	104	MC74HC86J	104
	MC74HC10N	104		
	MC74HC20N	100		
	MC74HC86N	104		
	MC74HC132N	100		
	MC74HC266N	104		
	MC74HC4075N	100		
Flip-Flops And Latches	MC74HC74N	180		
	MC74HC109N	100		
MSI	MC74HC138N	178	MC74HC373J	95
	MC74HC139N	100	MC74HC533J	95
	MC74HC160N	104		
	MC74HC161N	159		
	MC74HC175N	100		
	MC74HC242N	95		
	MC74HC257N	100		
	MC74HC280N	100		
MSI – Bus Compatible	MC74HC242N	95	MC74HC373J	95
	MC74HC257N	100	MC74HC533J	95

Table 2.
Summary of 1982 Life Test Data — Plastic

Device Classification	# of Lots	# of Devices	# of Failures	Actual Device Hours	85°C Equivalent Device Hours	85°C Failure Rate %/1000 Hours (60% Confidence Limit)
SSI	9	1016	1	1.02×10^6	2.65×10^7	0.0074
Flip-Flops And Latches	3	280	1	2.75×10^5	7.14×10^6	0.027
MSI	10	936	2	9.4×10^5	2.44×10^7	0.018
MSI — Bus* Compatible	2	195	0	1.97×10^5	5.10×10^6	0.017
Totals	22	2232	4	2.24×10^6	5.80×10^7	0.0086

*Note: Data generated on the Bus Compatible MSI devices are included with the MSI group as well.

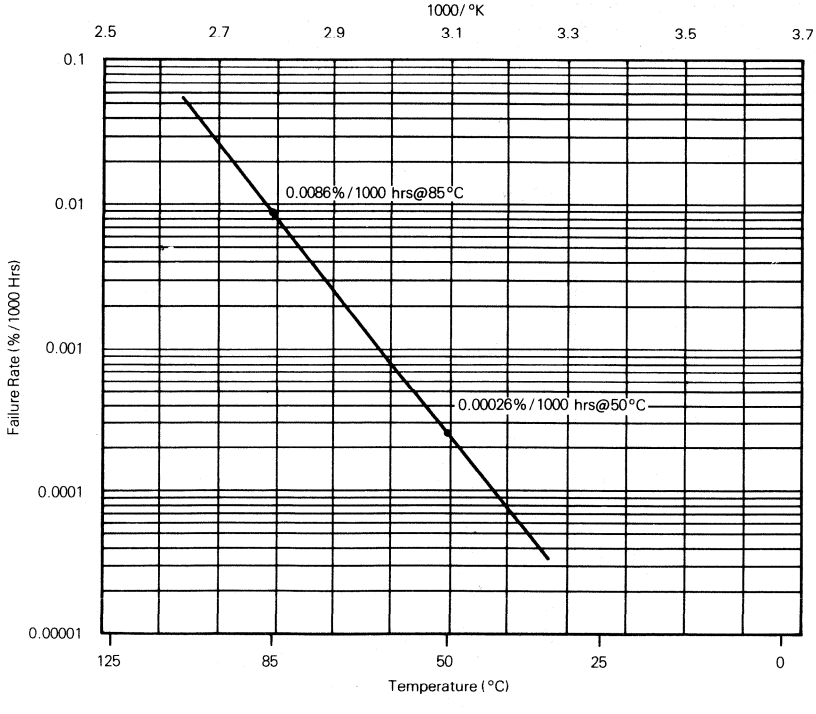


Figure 1. Failure Rate versus Temperature — Plastic

Table 3.
Summary of 1982 Life Test Data — Ceramic

Device Classification	# of Lots	# of Devices	# of Failures	Actual Device Hours	85°C Equivalent Device Hours	85°C Failure Rate %/1000 Hours (60% Confidence Limit)
SSI	4	469	0	4.73×10^5	1.23×10^7	0.0072
Flip-Flops And Latches	X	X	X	X	X	X
MSI – Bus Compatible	2	193	0	1.93×10^5	5.0×10^6	0.018
Totals	6	662	0	6.66×10^5	1.73×10^7	0.005

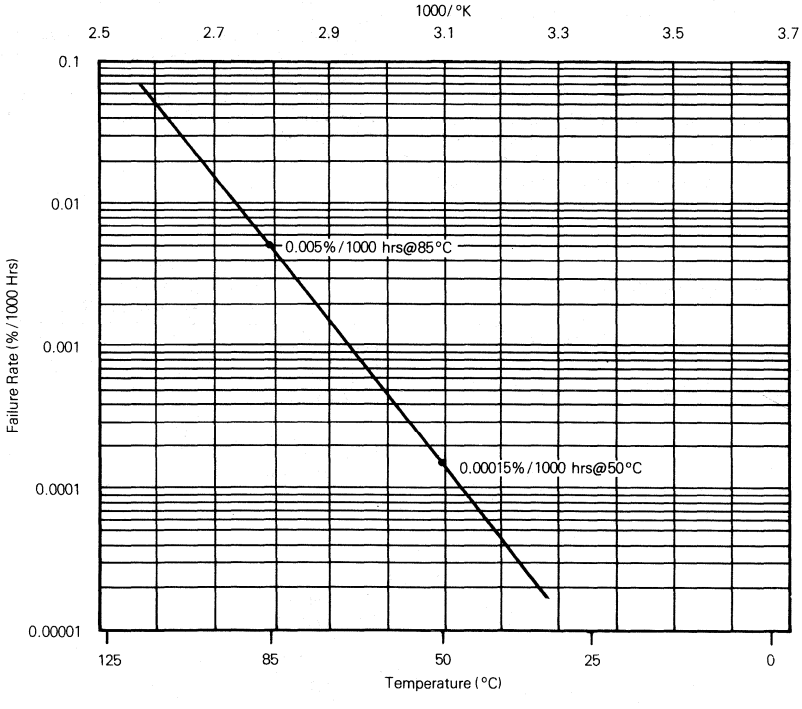


Figure 2. Failure Rate versus Temperature — Ceramic

6

LIFE TEST FAILURE SUMMARY

An in-depth analysis was performed on all four failures from the life test experiments. The single failure in the SSI group was due to a field oxide defect causing a small polysilicon shunt to the p-well, resulting in 5 μA I_{CC} leakage at the 48 hour electrical test. The single failure in the Flip-Flops and Latches group was due to a photo-resist flaw causing an open gate, resulting in 4.4 μA I_{CC} leakage at the 48 hour electrical test. Of the two failures from the MSI group, one was a functional failure at the 504 hour electrical test which fully recovered after being subjected to a bake at 175°C for 24 hours; the other failure was a short from an undetermined cause at the 504 hour electrical test. Note that these results were obtained on product without a preconditioning burn-in, and no attempt has been made to exclude infant mortality failures from the data.

CMOS failure rates are calculated for an 85°C operating environment and, for comparisons to the data base, calculations are based on 1008 hour life test data. The Arrhenius relationship is employed to compute the equivalent 85°C device hours using 1.0 eV activation energy and the accelerated life test device hours at 125°C.

PROTRACTED LIFE TESTING

The following additional stresses were applied with the purpose of thoroughly examining this product line for any problems which would occur in stresses of extreme duration and temperature. Further studies at these extreme levels of stress will probably not be repeated in future reliability evaluations.

EXTENDED LIFE TEST

Twenty-two of the above twenty-eight lots, a total of 2,181 devices, were subjected to an additional 504 hours of 125°C life test. Two additional failures were generated. Eleven lots, a total of 1,133 devices, were continued to 2016 hours and six lots, 634 devices, were continued to 4536 hours; no additional failures occurred. See Table 4 for a summary of results.

140°C AND 150°C ACCELERATED LIFE TEST

An additional 1,053 devices were subjected to greater temperature extremes and longer test times than standard operating life test to evaluate device performance under additional stress.

A group of 784 plastic and ceramic packaged devices were stressed at 140°C with a 5 volt static bias for 3528 hours and a group of 269 ceramic devices were stressed at 150°C and 5 volts for a total of 3696 hours. No failures were detected for either group. For a list of all devices tested at 140°C or 150°C refer to Table 5.

Table 4.
125°C Extended Life Test Summary

Device Classification	Cumulative Test Time (Hours) 1512	2016	4536
SSI	1/1180	0/1078	0/579
Flip-Flops And Latches	1/173	–	–
MSI	0/828	0/55	0/55
Totals	2/2181	0/1133	0/634

Table 5.
Device Types Used In 140°C And 150°C Accelerated Life Test

140°C	Quantity	150°C	Quantity
MC54HC00J	165	MC54HC00J	165
MC74HC02N	104	MC54HC10J	104
MC74HC10N	96		
MC54HC10J	104		
MC74HC74N	80		
MC74HC138N	180		
MC74HC161N	55		

Table 6.
140°C Accelerated Life Test Summary
Plastic and Ceramic 5 Volt Static Bias

Lots	Devices	Hours 24	72	192	528	1584	3528	Total % Failures
7	784	0	0	0	0	0	0	0.00

Table 7.
150°C Accelerated Life Test Summary
Ceramic 5 Volt Static Bias

Lots	Devices	Hours 30	96	264	816	1848	3696	Total % Failures
2	269	0	0	0	0	0	0	0.00

TEMPERATURE HUMIDITY BIAS

The plastic encapsulated device has been popular due to a considerable cost advantage over hermetically sealed units. Although most plastic package applications are relatively benign, a degree of moisture resistance is required by most users. Temperature Humidity Bias (THB) is a test designed to evaluate the moisture-related performance of the package-die combination and is performed under a 5 volt bias at 85°C and 85% relative humidity. Electrical measurements are conducted at 168, 504, 1008 and 1512 hours to full data sheet specifications.

THB testing was performed on 869 plastic devices which were assembled with copper leadframes, conductive epoxy die attach and thermosonic gold ball bonding. Test results for the various device groupings are found in Table 8.

All four THB failures in the SSI and Flip-Flops and Latches groups resulted from corrosion. The single failure in the MSI group was a leakage reject resulting from an oxide defect. The data accumulated under the severe THB conditions demonstrate excellent moisture resistance. This performance can be attributed to the silicon-gate process, the good thermal expansion match between the copper leadframe material and molding compound, and excellent passivation.

Table 8.
Temperature Humidity Bias
85°C 85% R.H. 5 Volts

Device Classification	Cumulative Test Time (Hours) 168	504	1008	1512
SSI	0/440	1/430	1/428	0/88
Flip-Flops And Latches	0/88	0/88	1/88	1/87
MSI	1/341	0/340	0/340	0/170
MSI Bus* Compatible	0/85	0/85	0/85	0/85
Cumulative % Failure	0.12	0.23	0.47	0.76

AUTOCLAVE

Autoclave is a storage test employing the environmental conditions of $T_A = 121°C$, 100% relative humidity, and 15 psig. This test is employed as an additional stringent test to measure the moisture resistance of the packaging system and susceptibility of the die to corrosion. As with THB testing, both package integrity and actual die construction play a major role in the results. Autoclave test results are found in Table 9.

The three failures generated during autoclave testing were due to corrosion.

Table 9.
Autoclave
121°C 100% R.H. 15psig

Device Classification	Cumulative Test Time (Hours) 24	48	144
SSI	0/100	0/100	–
Flip-Flops And Latches	–	0/98	0/98
MSI	0/265	2/265	1/265
MSI Bus* Compatible	–	2/115	1/65
Cumulative % Failure	0.0	0.43	0.71

***Note:** Data generated on the Bus Compatible MSI devices are included with the MSI group as well.

THERMAL CYCLING

The compatibility of materials used in the fabrication of any device is essential to its reliability. Any appreciable mismatch in physical properties, such as thermal expansion coefficients, can cause long-term device failures. These concerns were investigated by performing temperature cycling and thermal shock testing.

TEMPERATURE CYCLE

The test procedure for temperature cycle employs the parameters specified in MIL-STD-883B, method 1010.4, condition C. Devices are subjected to temperature extremes of −65°C to +150°C in nitrogen filled chambers. One test cycle consists of a ten minute dwell at each temperature extreme plus a transition time of approximately five minutes. The gradual change of temperature and relatively long dwell times in an air ambient tend to uncover problems related to expansion rate differentials. Devices are electrically tested after 100, 500, and 1000 cycles. Results of temperature cycle tests for all plastic encapsulated device groups and for SSI ceramic encapsulated devices are found in Tables 10 and 11, respectively.

THERMAL SHOCK

Thermal shock is an environmental test performed in accordance with MIL-STD-883B, method 1011.3, condition C. The objective of the test is the same as that for temperature cycle — to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides a more severe stress than temperature cycle in that the device is exposed to a sudden change in temperature due to the high thermal conductivity and capacity of the liquid ambient.

Devices are placed in a fluorocarbon bath cooled to −65°C. After being held in the cold chamber for at least five minutes, the sample is transferred to an adjacent chamber filled with fluorocarbon at 150°C, and held for an equivalent time. Thermal shock end point testing is performed after 100, 500, and 1000 cycles. Results of thermal shock tests for all plastic device groups and for the SSI ceramic device group are found in Tables 12 and 13, respectively.

The results of thermal cycling tests on High-Speed CMOS devices were excellent with only 2 hermeticity failures generated during thermal shock testing.

Table 10.
Temperature Cycle
−65°C to +150°C

Device Classification	Cumulative Test Cycles 100	500	1000	Cumulative % Failures
SSI	0/339	0/339	0/339	0.00
Flip-Flops And Latches	0/40	0/40	0/40	0.00
MSI	0/179	0/179	0/179	0.00
MSI Bus* Compatible	0/39	0/39	0/39	0.00
Total	0/558	0/558	0/558	0.00

Table 11.
Temperature Cycle
(Ceramic SSI)
−65°C to +150°C

Test	Cumulative Test Cycles 100	500	1000	Cumulative % Failures
Electrical	0/158	0/158	0/158	0.00
Hermeticity	0/158	0/158	0/158	0.00

Table 12.
Thermal Shock
−65°C to +150°C

Device Classification	Cumulative Test Cycles 100	500	1000	Cumulative % Failures
SSI	0/337	0/329	0/329	0.00
Flip-Flops And Latches	0/40	0/40	0/40	0.00
MSI	0/180	0/180	0/180	0.00
MSI Bus* Compatible	0/40	0/40	0/40	0.00
Total	0/557	0/549	0/549	0.00

Table 13.
Thermal Shock
(Ceramic SSI)
−65°C to +150°C

Test	Cumulative Test Cycles 100	500	1000	Cumulative % Failures
Electrical	0/176	0/176	0/176	0.00
Hermeticity	0/176	0/176	2/176	1.10

*Note: Data generated on the Bus Compatible MSI devices are included with the MSI group as well.

MECHANICAL SERIES

A group of 99 CERDIP SSI devices were stressed using a cumulative sequence of physical tests including, in order of their application, mechanical shock (1), variable frequency vibration (2) and, constant acceleration (3). Mechanical shock determines the ability of the device to withstand moderately severe impacts which could occur in the field; variable frequency vibration tests device resistance to vibration and resonances; and constant acceleration detects mechanical weakness at higher force levels. Two hermeticity failures were detected by these tests.

Table 14.
Mechanical Series
Mechanical Shock — 1,500 g 0.5 msec Y1 axis
Variable Frequency Vibration — 20 g 20 kHz 4 min Y1 axis
Constant Acceleration — 30,000 g 1 min Y1 axis

Test	Failures/Sample	
	Electrical	Hermeticity
1) Mechanical Shock	0/98	0/99
2) Variable Frequency Vibration	0/98	0/98
3) Constant Acceleration	0/96	2/98

CONCLUSIONS

Thorough reliability testing has been performed on an extensive cross section of the High Speed CMOS logic family. The evaluations included accelerated life tests and a series of environmental stresses designed to assess package integrity, moisture resistance, and thermal compatibility. Through these tests, Motorola's High Speed CMOS has proven to be an exceptionally reliable family of devices across the board, from SSI to our highest complexity functions. Reliability testing will continue and these comprehensive reports will be issued on an annual basis. Reports will be made available upon customer request.

For additional information, contact CMOS Logic & Special Functions Reliability Engineering at (512) 928-6640 or write to:

CMOS Logic & Special Functions Reliability Engineering
Motorola Incorporated
3501 Ed Bluestein Boulevard
Austin, Texas 78721

Mechanical Data

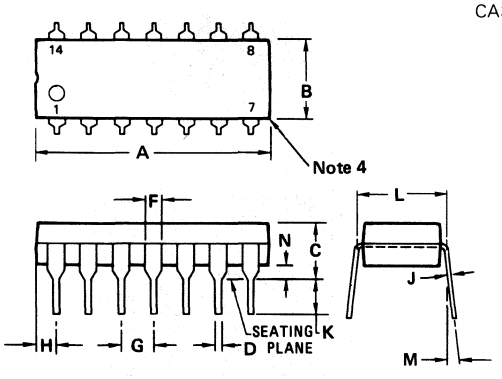
7

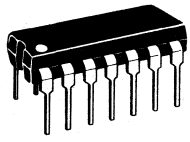
MECHANICAL DATA

The packaging availability for each device is indicated on the individual data sheets. Dimensions for the packages are given in this section.

14-PIN PACKAGES

PLASTIC PACKAGE
CASE 646

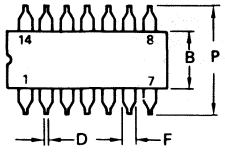


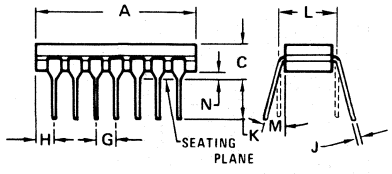


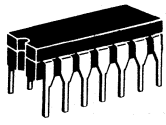
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

CERDIP PACKAGE
CASE 632





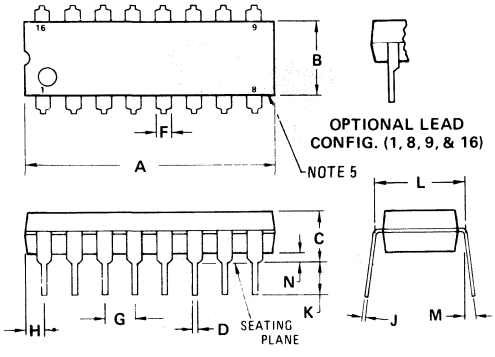


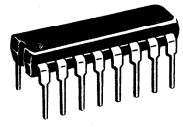
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "A" AND "B" (632-07) DO NOT INCLUDE GLASS RUN-OUT.
4. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

16-PIN PACKAGES

PLASTIC PACKAGE
CASE 648

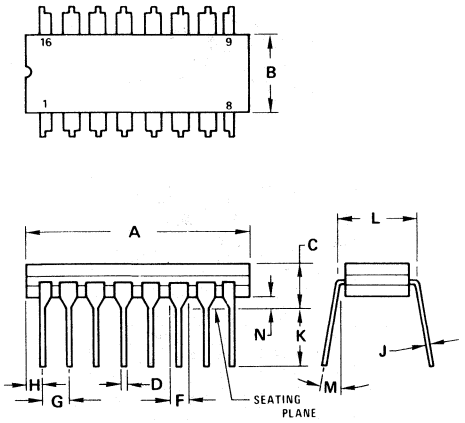


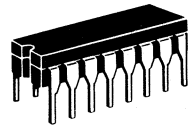


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

CERDIP PACKAGE
CASE 620



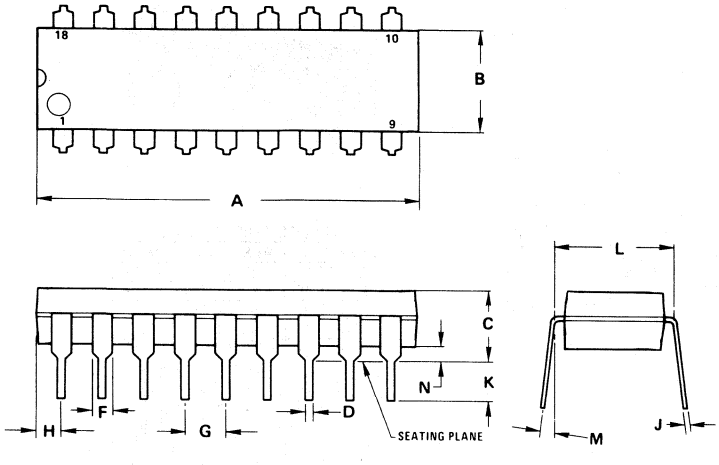


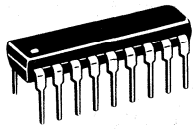
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	–	15^0	–	15^0
N	0.51	1.02	0.020	0.040

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
5. DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

18-PIN PACKAGES

PLASTIC PACKAGE
CASE 707



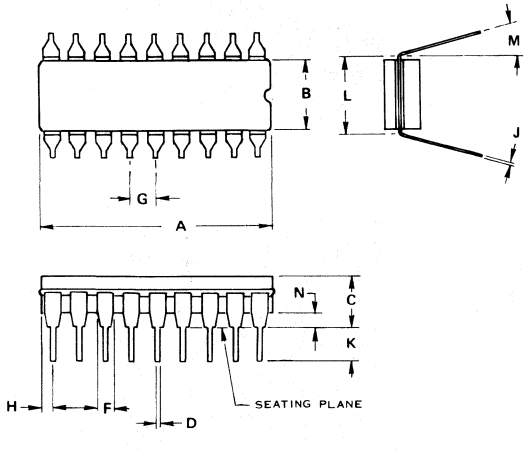


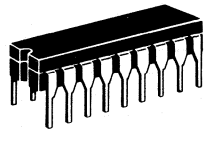
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

CERDIP PACKAGE
CASE 726





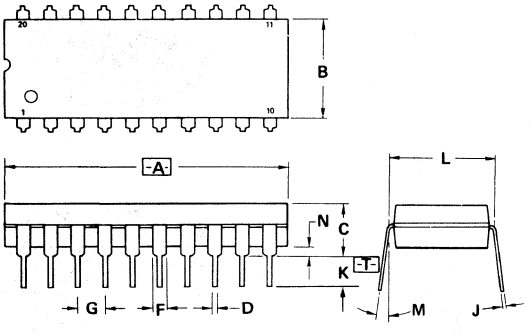
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

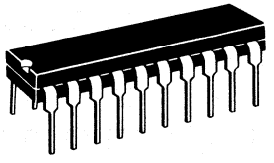
NOTES:

1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.

20-PIN PACKAGES

PLASTIC PACKAGE
CASE 738

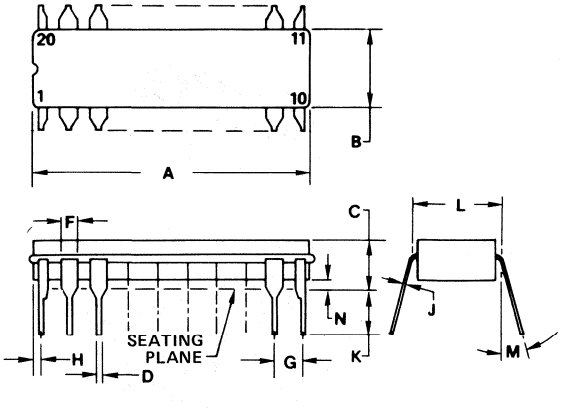


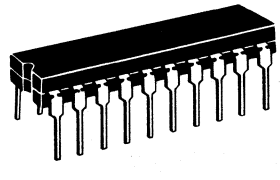


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS;
   ⌖ Ø 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

CERDIP PACKAGE
CASE 732



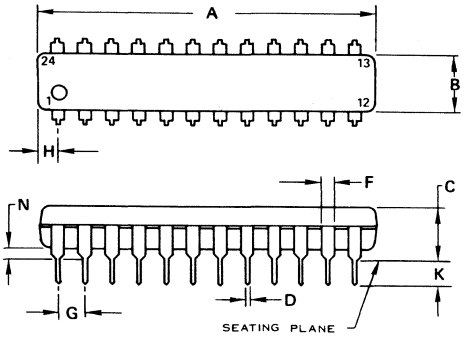


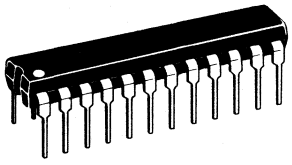
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

24-PIN PACKAGES

PLASTIC PACKAGE
CASE 724

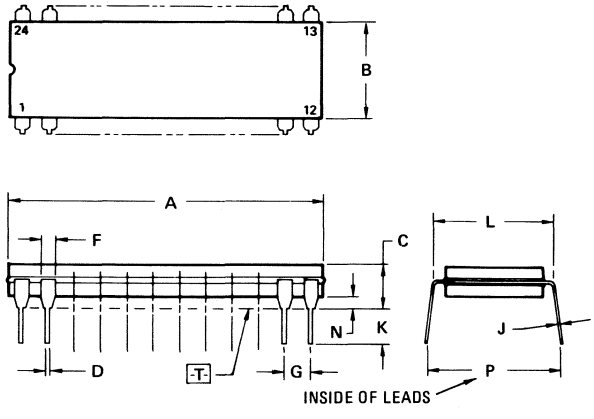


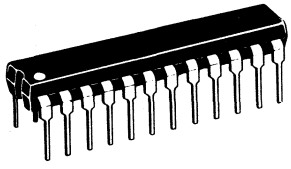


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.13	1.230	1.265
B	6.35	6.86	0.250	0.270
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040

NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM D).

CERDIP PACKAGE
CASE 758





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.64	1.240	1.285
B	7.24	7.75	0.285	0.305
C	3.68	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.14	1.57	0.045	0.062
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	7.62	7.87	0.300	0.310
N	0.51	1.27	0.020	0.050
P	9.14	10.16	0.360	0.400

NOTES:
1. DIMENSION A IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: 24 PLACES
   ⌖ 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.